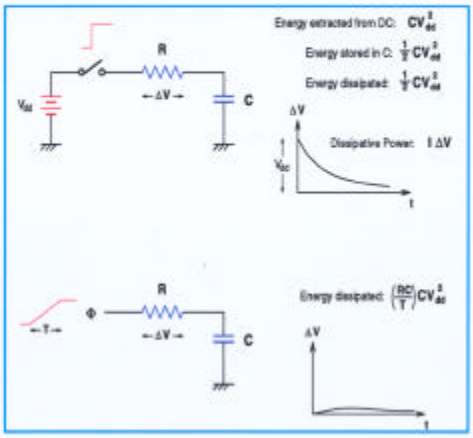
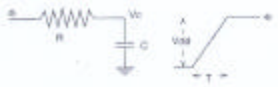
Adiabatic Switching Concept



3c)



$$RC\left(\frac{dV_c}{dt}\right) + V_c = \Phi$$

$$\Phi = \begin{cases} 0 & t < 0 \\ \left(\frac{V_{dd}}{T}\right)t & 0 \le t < T \\ V_{dd} & t \ge T \end{cases}$$

The solution of the above equation is given by

$$V_c = \begin{cases} 0 & t < 0 \\ \Phi - \left(\frac{RC}{T}\right)V_{dd}(1 - e^{-t/RC}), & 0 \le t < T \\ \Phi - \left(\frac{RC}{T}\right)V_{dd}(1 - e^{-T/RC})e^{-(t-T)/RC} & t \ge T \end{cases} \quad (7.2)$$

The energy dissipation in the above charging process can be calculated as follows:

$$E_{\text{linear}} = \int_0^\infty iV_R\,dt = \int_0^T iV_R\,dt + \int_T^\infty iV_R\,dt \quad (7.3)$$

The first term of Eq. (7.4) can be written as

$$\int_0^T i V_R\,dt = \int_0^T \frac{(\Phi - V_c)^2}{R}\,dt$$

$$= \int_0^T \frac{\left[(V_{dd}/T)RC(1 - e^{-t/RC})\right]^2}{R\,dt}$$

$$= \frac{R^2C^2}{T^2} CV_{dd}^2 \int_0^{T/RC} (1 - e^{-t/RC})^2 d\left(\frac{t}{RC}\right)$$

$$= \left(\frac{RC}{T}\right) CV_{dd}^2 \left[1 - \frac{3}{2}\left(\frac{RC}{T}\right) + 2\left(\frac{RC}{T}\right) e^{-T/RC} - \frac{1}{2}\left(\frac{RC}{T}\right) e^{-2T/RC}\right]$$

And the second term can be written as

$$\int_T^\infty i V_R\,dt = \int_T^\infty \frac{(\Phi - V_c)^2}{R}\,dt$$

$$= \frac{RC}{T^2} CV_{dd}^2 (1 - e^{-T/RC})^2 \int_T^\infty e^{-2(t-T)/RC}\,dt$$

$$= \left(\frac{RC}{T}\right)^2 CV_{dd}^2 \left[\frac{1}{2}(1 - e^{-T/RC})^2\right]$$

Finally we have

$$E_{losses} = \left(\frac{RC}{T}\right) CV_{dd}^2 \left(1 - \frac{RC}{T} + \frac{RC}{T} e^{-T/RC}\right) \qquad (7.4)$$

Let us consider the two extreme cases. When $T \gg RC$,

$$E_{losses} = \left(\frac{RC}{T}\right) CV_{dd}^2 \qquad (7.5)$$

and when $T \ll RC$

$$E_{losses} = \left(\frac{RC}{T}\right) CV_{dd}^2 \left\{1 - \frac{RC}{T} + \frac{RC}{T}\left[1 - \frac{T}{RC} + \frac{1}{2}\left(\frac{T}{RC}\right)^2\right]\right\}$$

$$= \frac{1}{2} CV_{dd}^2 \qquad (7.6)$$

Similarly,

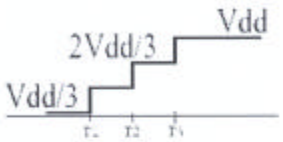
$$E_C = \int_0^\infty i_{VDD}(t) V_{out}\,dt = \int_0^{T_1} i_{VDD}(t) V_{out}\,dt + \int_{T_1}^{T_2} i_{VDD}(t) V_{out}\,dt + \int_{T_2}^\infty i_{VDD}(t) V_{out}\,dt$$

$$= C\int_0^{\frac{V_{DD}}{3}} V_{out}\,dV_{out} + C\int_{\frac{V_{DD}}{3}}^{\frac{2V_{DD}}{3}} V_{out}\,dV_{out} + C\int_{\frac{2V_{DD}}{3}}^{V_{DD}} V_{out}\,dV_{out}$$

$$= \frac{1}{2} CV_{DD}^{\ 2}$$

$$E_d = \frac{2}{3} V_{DD}^{\ 2} - \frac{1}{2} CV_{DD}^{\ 2} = \frac{1}{6} CV_{DD}^{\ 2}$$

3b)



$$E_{VDD} = \int_0^{T_1} i_{VDD}(t)\frac{V_{DD}}{3}dt + \int_{T_1}^{T_2} i_{VDD}(t)\frac{2V_{DD}}{3}dt + \int_{T_2}^{\infty} i_{VDD}(t)V_{DD}dt$$

$$= \int_0^{T_1} C\frac{dV_{out}}{dt}\frac{V_{DD}}{3}dt + \int_{T_1}^{T_2} C\frac{dV_{out}}{dt}\frac{2V_{DD}}{3}dt + \int_{T_2}^{\infty} C\frac{dV_{out}}{dt}V_{DD}dt$$

$$= C\frac{V_{DD}}{3}\int_0^{\frac{V_{DD}}{3}} dV_{out} + C\frac{2V_{DD}}{3}\int_{\frac{V_{DD}}{3}}^{\frac{2V_{DD}}{3}} dV_{out} + CV_{DD}\int_{\frac{2V_{DD}}{3}}^{V_{DD}} dV_{out}$$

$$= \frac{2}{3}CV_{DD}^2$$

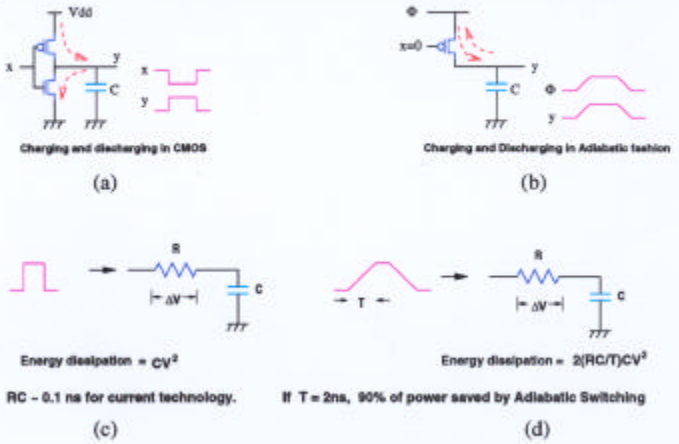
3a)

$$E_{VDD} = \int_0^{\infty} i_{VDD}(t)V_{DD}dt = \int_0^{\infty} V_{DD}C\frac{dV_{out}}{dt}dt = CV_{DD}\int_0^{\infty} dV_{out} = CV_{DD}^2$$

$$E_C = \int_0^{\infty} i_{VDD}(t)V_{out}dt = \int_0^{\infty} C\frac{dV_{out}}{dt}V_{out}dt = C\int_0^{\infty} V_{out}dV_{out} = \frac{1}{2}CV_{DD}^2$$

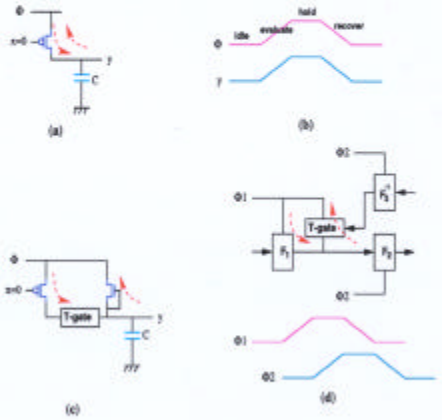
$$E_d = CV_{DD}^2 - \frac{1}{2}CV_{DD}^2 = \frac{1}{2}CV_{DD}^2$$

Adiabatic Switching Concept (continued)

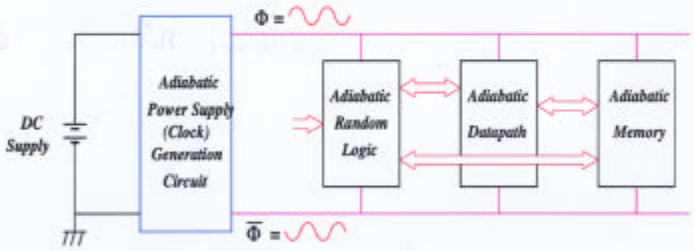


Basic Operations in an Adiabatic Logic Gate

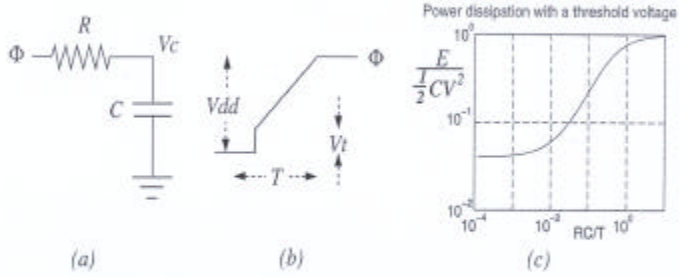
- Output follows clock signal
- 4-phase in a clock
  - evaluate
  - hold
  - recover
  - idle
- Need input isolation and output recovery scheme



Adiabatic Digital System

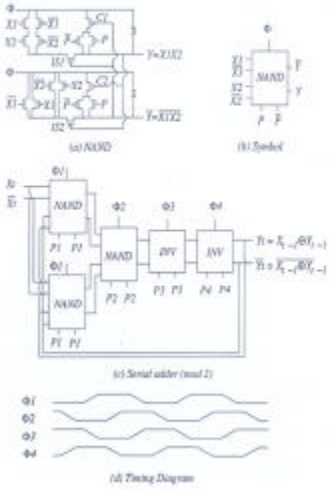


Energy Dissipation Model with Threshold Voltage



- Resistance Loss: $(RC/T)CV^2_{dd}$
- Threshold Loss: $(1/2)CV^2_{th}$
  - Dominate at low frequency

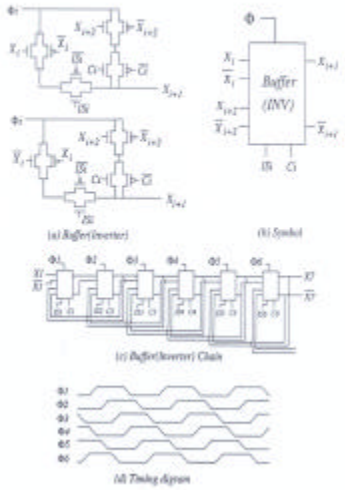
A Bit-Serial Adder using Partially Reversible Logic



- 4 phases of clock required
- Using local signal to control the recovery path. Hence, inverse function is not required
- Differential signaling is used

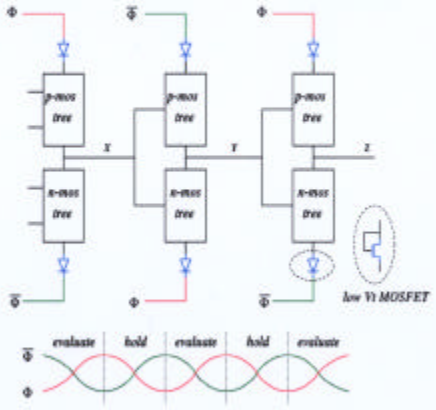
A Buffer (Inverter) Chain using Reversible Logic

- 6 phases of clock required
- Inverse logic naturally available
- Charge recovery path can be controlled by inverse function (next stage gate in buffer chain)
- In general, reversibility is not available



Quasi-Static Energy Recovery Logic (QSERL)

- Two phase clocks
- Comparable complexity with static CMOS
- Low threshold voltage MOSFET as the diode
- Lower switching activity than dynamic adiabatic logic

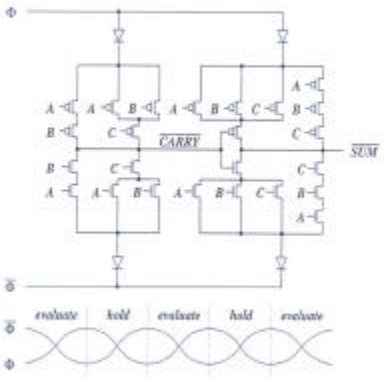


Advantages of Quasi-Static Energy Recovery Logic

- Limitations of Previous Adiabatic Logic
  - Dynamic
  - Complex Power Supply/Clock Schemes
  - Major Transistor & Wiring Overheads
  - Careful Transistor Ratioing
- Advantages of Quasi-Static Energy Recovery Logic (QSERL)
  - Simple dual-rail power supply/clock
  - Modest overhead in transistor counts & wiring
  - Convertibility from CMOS designs

A Full Adder Using QSERL

- A quasi-CMOS adiabatic adder
- Works in both static CMOS and adiabatic mode
- A 2x2 adiabatic multiplier using this adder implemented

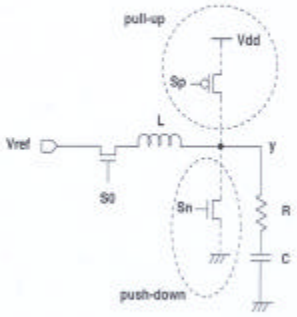


Summary of Simulation Results of Adiabatic Logic Blocks

- A buffer chain using reversible logic
  - At 1 MHz, 94% of energy recovered
  - At 111 MHz, 68% of energy recovered
- A bit-serial adder using partially reversible logic
  - At 1 MHz, 90% of energy recovered
  - At 111 MHz, 61% of energy recovered
- A 2x2 multiplier using QSERL logic
  - At 20 MHz, 60% of energy saved
  - At 100 MHz, 35% of energy saved

A Generic Resonant Scheme for Energy Recovery

- Ideally, the circuit oscillates between ***0*** and $2V_{ref}$
- Pull-up and pull-down paths to replenish the energy to keep oscillation going
- Extra circuits to generate control signal ***Sp*** and ***Sn***
- External control signals ***Sp*** and ***Sn*** are ***180*** degree out of phase



A Generic Resonant Scheme (continued)

- Serial connected control transistor ***S0*** limits the energy recovery efficiency
- Extra circuitry to generate ***Sp*** and ***Sn***
- Energy in charging the gate capacitances of ***Sp*** and ***Sn*** are dissipated
- It requires an additional reference voltage source
- Single phase clock is generated. More than one resonant circuit is required