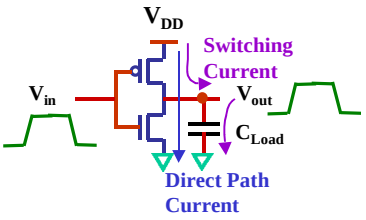
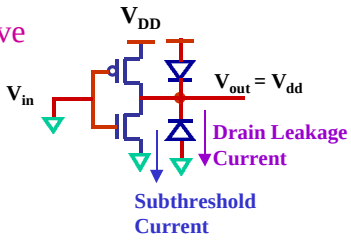
Power Estimation

Power Dissipation in CMOS

- Dynamic
  - -- Switching Power
  - -- Short Circuit
- Leakage
  - -- Diode leakage
  - -- Sub-threshold leakage



Lowering supply voltage is an effective way to reduce power

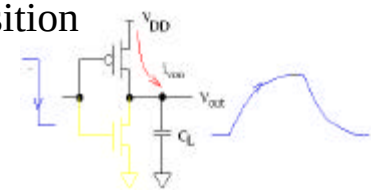


Switching Power

- Signal properties
  - Signal probability, P_i, - probability of a signal being logic ONE
  - Signal activity, a_i, - probability of signal switching(0->1, or 1->0)
- Energy dissipated per transition

$$E_{VDD} = \int_0^\infty i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^\infty C_L \frac{dv_{out}}{dt} dt$$

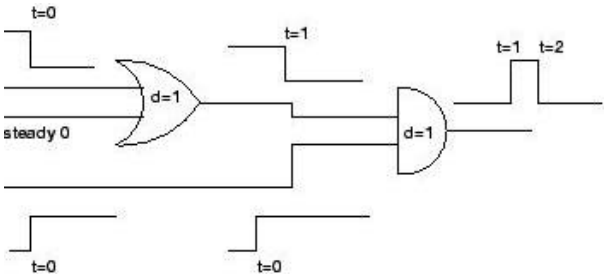
$$= C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$



$$E_C = \int_0^\infty i_{VDD}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out} = C_L V_{DD}^2 / 2$$

Energy dissipated for 1->0 or 0->1 transition: $C_L V_{DD}^2 / 2$

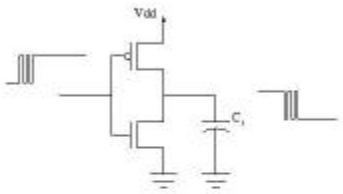
Spurious Transition at a Node



Hazardous transition occurs at the output of AND gate due to different delays through two different paths converging at the inputs to the AND gate.

- Assume each gate has unit delay
- Width of the glitch depends on the delays through the logic gates and interconnects.

Dynamic Power



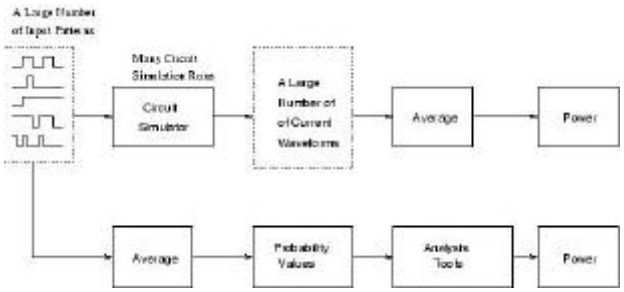
$P_{ave} = \frac{1}{2} \sum_i Vdd^2 C_i \, A_i.$

If no delays (no glitches), $a_i \equiv A_i / f \;\; (A_i * T_c)$

and $P_{ave} = \frac{1}{2} \sum_i Vdd^2 C_i \, (a_i / T_c).$

$\Rightarrow$ Estimate A_i or a_i.

Average Number of Transitions



Switching at internal nodes depends on input signals.

Model input signals as stochastic process. Each signal having some properties:

- Signal probability

- Signal activity

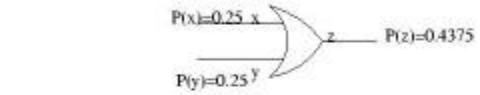
Modeling of the Input Signals

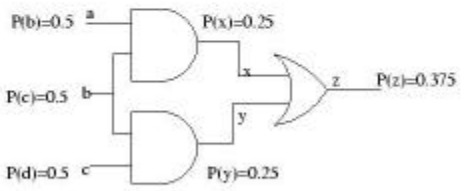
- Run simulation for a long time and take the average.
  - Straight-forward and simple
  - Computationally expensive
  - Specific information about the inputs required and sometimes not available
- Input signals are modeled by its probabilistic behavior – weakly pattern-dependent:
  - Signal Probability (P)
  - Activity (A) or Normalized Activity (a, or Transition Probability)

Review of Power Estimation Techniques

- Two major weakly pattern-dependent techniques have been proposed.
  - Probabilistic Approach
    - Temporal correlation of primary inputs
    - Spatial correlation of internal nodes
    - Partitioning – divide and conquer
    - Delay models
  - Statistical Approach
    - Delay models

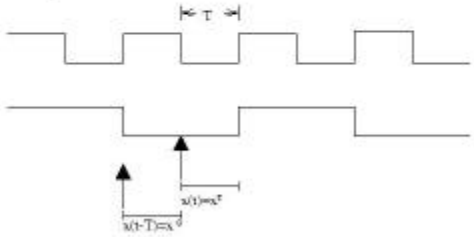
Spatial Correlation



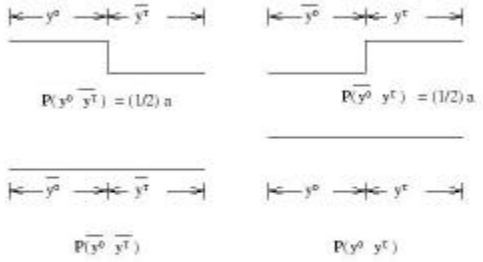


Temporal Correlation of Signals

- $x(t-T)$ (x^0) and $x(t)$ (x^T) are not independent.
  These two signals have the same probability but different activity values.



Closer Look at the Normalized Activity



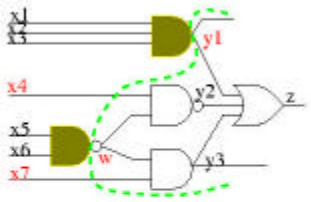
An Efficient Algorithm for computing Activity

- $P(\overline{y^0}y^T) + P(y^0y^T)$
  $= P(\overline{y^0}y^T + y^0y^T)$
  $= P(y^T) = P(y)$.
  Therefore, we have $P(y^0y^T) = P(y) - \frac{1}{2}a(y)$.
- $a(y) = 2[P(y) - P(y^0y^T)]$.
- If the symbolic representation of $P(y)$ is available, we can derive $P(y^0y^T)$.

Why Partition the Circuit?

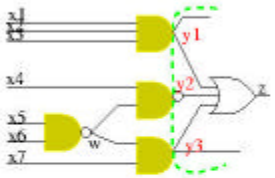
- Only minimum independent inputs are required.
  $\Rightarrow$ speed up the computation without sacrificing accuracy.
- The exact calculation of signal probability and activity is NP-hard.
  - The number of product terms may grow exponentially with respect to the number of independent inputs.
  $\Rightarrow$ Less correlated signals are chosen as independent inputs.

Partitioning Circuits



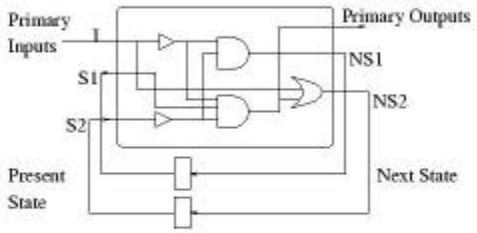
- Before partitioning, $a(z)$ is expressed in terms of: probability and activity of nodes x_1, $x_2 \cdots x_7$.
- After partitioning, $a(z)$ is expressed in terms of: probability and activity of nodes y_1, x_4, w, and x_7.

Further Partitioning Circuits



- After further partitioning, $a(z)$ is expressed in terms of: probability and activity of nodes y_1, $y2$, and y_3.
- Inaccuracy comes from reconvergent fanout w.
- Trade-off accuracy for computation time.

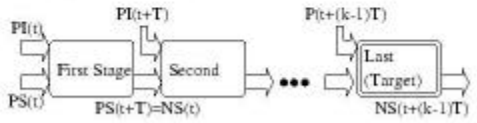
Probabilistic Approaches for Sequential Circuits



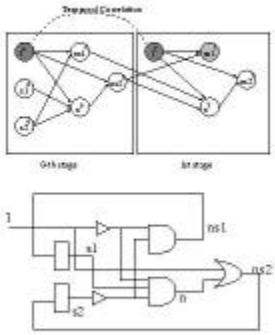
- How to model the correlation among state bits?
- What is the probability and activity of the state bits?

A Solution to Correlated State Bits

- How to model the correlation among state bits?
  Unroll the circuit k times.
- What are the probability and activity of the state bits?
  Assign initial values in the first stage and update them.
- Notice that Primary inputs are temporally correlated.
  $\Rightarrow PI(t)$ is NOT independent of $PI(t+T)$.

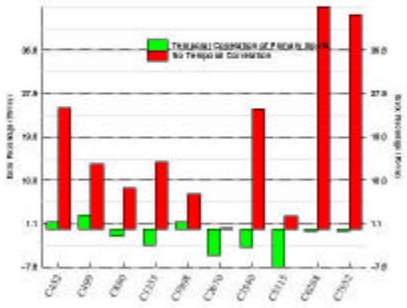


An example of unrolled circuits



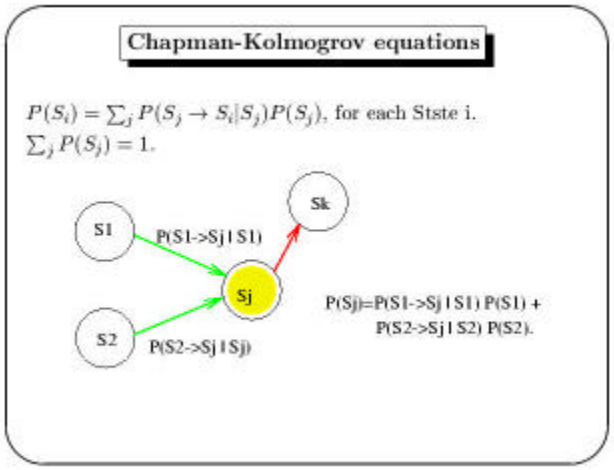
Results of Unrolling Method (Twice)

$P = 0.5$ and $a = 0.3$.



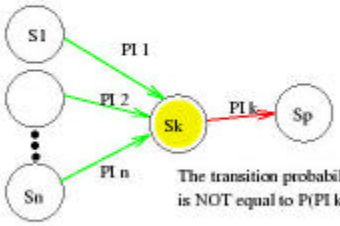
State Transition Graph

- If STG is available, one can determine the state probabilities using the Chapman-Kolomogorov equations.
- However, STG's do not consider temporal correlations among signals
  - Solution: Extended State Transition Graphs
    - High complexity



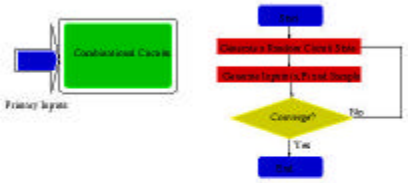
Why ESTG Instead of STG?

- Since primary inputs are temporally correlated, STG is not Markov.



The transition probability P(Sk->Sp | Sk) is NOT equal to P(PI k).

Statistical Approach in Combinational Circuits

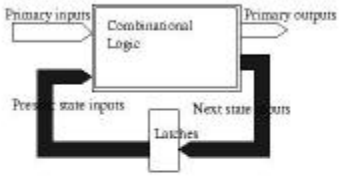


- Partitioning can also be used in this approach.
- Spatial and temporal correlations are taken care of automatically.

Stopping Criterion

- If the number of samples N is large, by CLT
  $\Rightarrow$ Sample mean $\bar{a}$: a random variable with normal distribution.
- Make inferences about the quality of each sample.
  With $(1-\alpha)$ confidence, $|\bar{a}-a| \leq z_{\alpha/2}\sigma$.
- Given $(1-\alpha)$ confidence and ϵ percentage error,
  $N \geq \left(\frac{z_{\alpha/2}s}{a\epsilon_1}\right)^2$
- If $\bar{a} \leq a_{min}$ (defined by users),
  $N \geq \left(\frac{z_{\alpha/2}s}{a_{min}\epsilon_1}\right)^2$

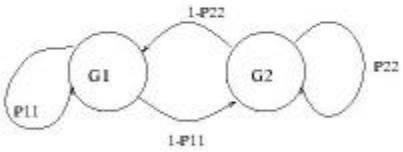
Problems with the Statistical Approach



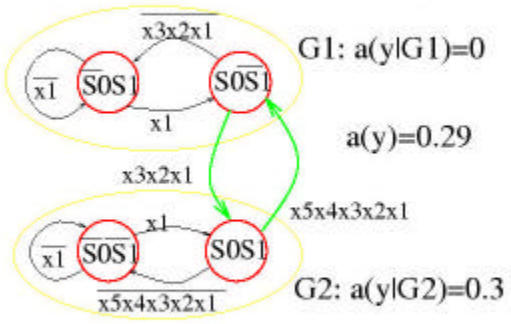
- Randomly generate an initial state with uniform distribution.
  $\Rightarrow$ Samples are biased.
- Start from the same initial state.
  $\Rightarrow$ If near-closed sets exist, data may be sampled from a particular near-closed set.

Near-Closed Sets in Sequential Circuits

- Closed set: No way out.
- Near-closed set: Probabilistically speaking, almost no way in and out.



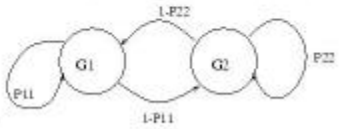
An Example of Near Closed Sets



$y = (s1 \oplus s0)x1.$

A Solution to the problems

- Randomly generate an initial state according to its state probability and sample data.
- Example: $P(G_1) = 0.7$, $P(G_2) = 0.3$, 100 samples a_i, $i = 1 \ldots 100$.
  70 samples from G_1 and 30 samples from G_2 and
  $\Rightarrow a(y) = \frac{\sum_{i=1}^{100} a_i}{100} = a(y|G_1)P(G_1) + a(y|G_2)P(G_2)$.



How to Generate Initial States?

If no state probability information is given,

- Step 1: Randomly generate an initial state with uniform distribution.
- Step 2: Run a *warmup period* of simulation. At the end of the warmup period, the probability of reaching state S_i is very close to the state probability $P(S_i)$. That is, the new initial state is in fact generated according to state probabilities. Then sample data.

How to Generate Initial States?

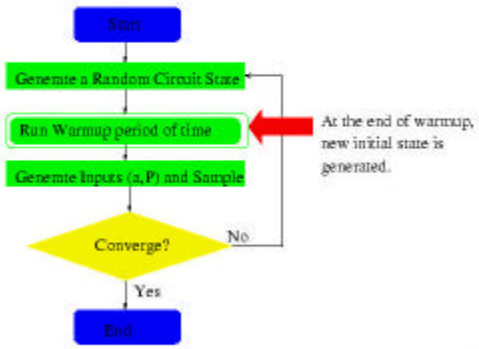
Say, $P(G_1) = 0.7$, $P(G_2) = 0.3$ and 100 samples.

After step 1, ≈ 50 initial states in G_1 and ≈ 50 in G_2.

After step 2, ≈ 70 new initial states in G_1 and ≈ 30 in G_2.

Therefore, 70 samples from G_1 and 30 from G_2.

Solution to the problems

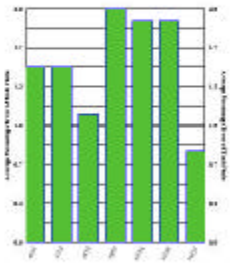


How to Determine the Warmup Period

- Assume the input signals are Markov.
- Transform STG into ESTG, since STG is NOT Markov but ESTG IS.
- Apply Markov chain theory to ESTG to determine the warmup period.

Results of Sequential Circuits with Warmup

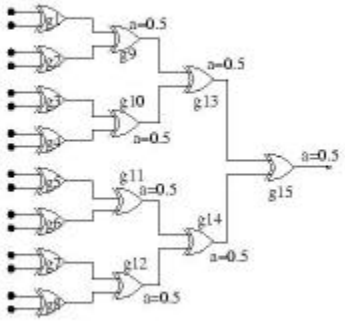
$P = 0.5$ and $a = 0.3$.



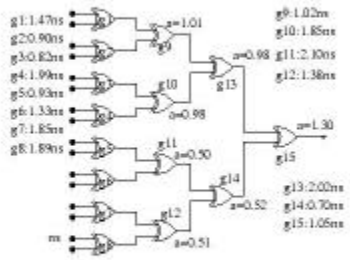
Sources of Uncertainty

- Systematic
  - approximation made to simplify models
  - approximation made to estimate device and interconnect parasitics prior to layout
- Random
  - uncontrolled variations in photolithography
  - die to die, wafer to wafer variations

Perfectly Balanced Tree with Nominal Delays

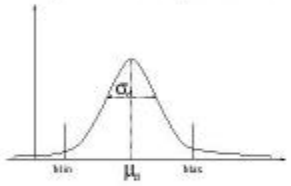


Perfectly Balanced Tree with Probabilistic Delays



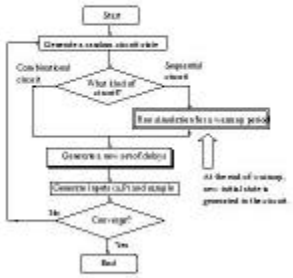
Probabilistic Delay Models

Use probabilistic delay models to capture the uncertainty.



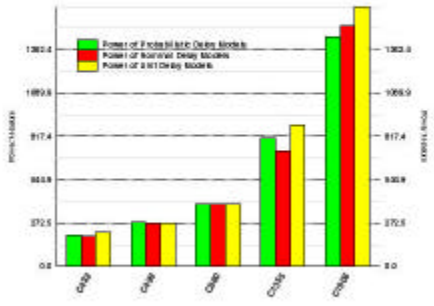
Statistical Estimation with Probabilistic Delays

$\mathbf{a} = F(\mathbf{PI}, D)$, where D is a reandom vector, which is equal to $(d_1, d_2, \ldots, d_n)$, and n is the number of gates in the circuit.



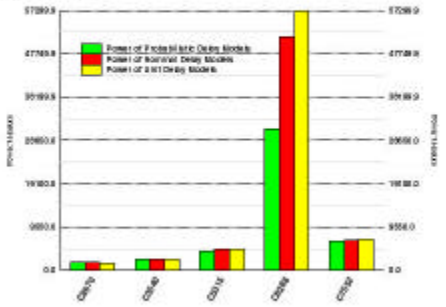
Power under Different Delay Models

$P = 0.5$ and $a = 0.5$.



Power under Different Delay Models

$P = 0.5$ and $a = 0.5$.



Power under Different Delay Models

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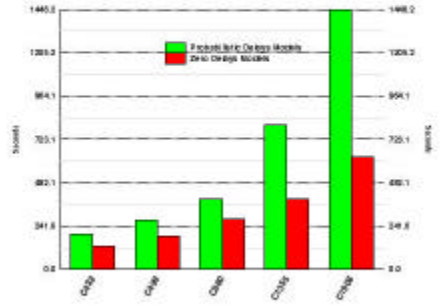

Power under Different Delay Models

$P = 0.5$ and $a = 0.5$.