Combinational Logic Gates in CMOS

References:
Adapted from: *Digital Integrated Circuits: A Design Perspective*, J. Rabaey, Prentice Hall © UCB
*Principles of CMOS VLSI Design: A Systems Perspective*, N. H. E. Weste, K. Eshraghian, Addison Wesley
Adapted from: EE216A Lecture Notes by Prof. K. Bult © UCLA
Combinational vs. Sequential Logic

**Combinational**

Out = f(In)

**Sequential**

Out = f(In, State)

State is related to previous inputs
Stored in registers, memory etc
Overview

• **Static CMOS**
  – Complementary CMOS
  – Ratioed Logic
  – Pass Transistor/Transmission Gate Logic

• **Dynamic CMOS Logic**
  – Domino
  – np-CMOS
Static CMOS Circuit

- At every point in time (except during the switching transients) each gate output is connected to either $V_{DD}$ or $V_{SS}$ via a low-resistive path.
- The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit.
- In contrast, a dynamic circuit relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.
Digital Gates
Fundamental Parameters

• Area and Complexity
• Performance
• Power Consumption
• Robustness and Reliability
What Can Go Wrong in CMOS Logic?

- Incorrect or insufficient power supplies
- Power supply noise
- Noise on gate input
- Faulty connections between transistors
- Clock frequency too high or circuit too slow

Complementary CMOS is pretty safe against these
How about Ratioed or Dynamic Logic?

- All the previous and
- Incorrect ratios in ratioed logic
- Charge sharing in dynamic logic
- Incorrect clocking in dynamic logic
Complementary CMOS

PUN and PDN are dual networks

V_{DD}

in_1 \hspace{1cm} in_2 \hspace{1cm} in_3

PMOS only

F = \overline{G}

V_{SS}

in_1 \hspace{1cm} in_2 \hspace{1cm} in_3

NMOS only
NMOS Transistors in Series/Parallel Connection

- Transistors can be thought as a switch controlled by its gate signal
- NMOS switch closes when switch control input is high

\[ X = Y \text{ if } A = 1 \text{ and } B = 1, \text{ i.e., } AB = 1 \]

\[ X = Y \text{ if } A = 1 \text{ or } B = 1, \text{ i.e., } A + B = 1 \]

- NMOS passes a strong 0 but a weak 1
NMOS Transistors in Series/Parallel Connection

• Connect Y to GND

X = 0 if A = 1 and B = 1, i.e., A.B = 1
X = A.B

X = 0 if A = 1 or B = 1, i.e., A + B = 1
X = A + B

• Implement the complement of PDN
PMOS Transistors in Series/Parallel Connection

• PMOS switch closes when switch control input is low

\[
X = Y \text{ if } A = 0 \text{ and } B = 0 \\
\text{or } A + B = 1 \\
\text{or } A.B = 1
\]

• PMOS passes a strong 1 but a weak 0

\[
X = Y \text{ if } A = 0 \text{ or } B = 0 \\
\overline{A.B} = 1 \\
\overline{A} + \overline{B} = 1
\]
PMOS Transistors in Series/Parallel Connection

- Connect Y to VDD

\[ X = 1 \text{ if } A = 0 \text{ and } B = 0 \]
\[ X = A + B = \overline{A}.\overline{B} \]

- Combine series PDN and parallel PUN or parallel PDN and series PUN to complete the logic design to output good 1 and 0

\[ X = 1 \text{ if } A = 0 \text{ or } B = 0 \]
\[ X = \overline{A}.B = \overline{A} + \overline{B} \]
Complementary CMOS Logic Style Construction

- PUN is the DUAL of PDN (can be shown using DeMorgan’s Theorems)

\[ A + B = \overline{A \overline{B}} \]
\[ \overline{A \overline{B}} = A + B \]
\[ \overline{AB} = \overline{A} + \overline{B} \]
\[ G(in_1, in_2, in_3, \ldots) \equiv F(\overline{in_1}, \overline{in_2}, \overline{in_3}, \ldots) \]

- The complementary gate is inverting
  - Implements NAND, NOR, …
  - Non-inverting boolean function needs an inverter
The NAND Circuit

PDN connected to GND: $\overline{G} = \overline{A} \cdot \overline{B}$
PUN connected to $V_{DD}$: $F = \overline{A} + \overline{B} = \overline{A+B}$

$G(in_1, in_2, in_3, \ldots) \equiv F(in_1, in_2, in_3, \ldots)$
The NOR Circuit

\[ \overline{A \cdot B} = A + B \]

Output table:

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

A + B

\[ \text{Output} = \overline{A \cdot B} \]
Example Gate: COMPLEX CMOS GATE

\[ \text{OUT} = \overline{D + A \cdot (B+C)} \]
\[ F = ((A \cdot B) + C \cdot (A + B)) = \text{carry} \]

Symmetrical!

Remove redundancy
\[ F = (ABC + ABC + ABC + ABC) = \text{sum} \]
Full Adder Circuit
4-input NAND Gate
Standard Cell Layout Methodology

- VDD
- VSS
- Well
- polsilsicon
- Routing Channel
- metal1
- signals
Two Versions of \((a+b).c\)

(a) Input order \(\{a \ c \ b\}\)

(b) Input order \(\{a \ b \ c\}\)
Consistent Euler Path

\{a \ b \ c\}
Example: $x = ab + cd$

(a) Logic graphs for $(ab+cd)$

(b) Euler Paths \{a b c d\}

(c) stick diagram for ordering \{a b c d\}
Properties of Complementary CMOS Gates

• High noise margin
  – $V_{OH}$ and $V_{OL}$ are at $V_{DD}$ and $G_{ND}$, respectively

• No static power consumption
  – In steady state, no direct path between $V_{DD}$ and $V_{SS}$

• Comparable rise and fall times under appropriate scaling of PMOS and NMOS transistors
Transistor Sizing

- For symmetrical response (dc, ac)
- For performance
- Input dependent
- Focus on worst-case
Propagation Delay Analysis - The Switch Model

(a) Inverter

(b) Two-input NAND

(c) Two-input NOR
Analysis of Propagation Delay

- Assume $C_L$ dominates
- Assume $R_n = R_p =$ resistance of minimum sized NMOS inverter
- For $t_{PLH}$
  - Worst case when only one PMOS pulls up the output node
  - $t_{PLH} \propto R_p C_L$
- For $t_{PHL}$
  - Worst case when two NMOS in series
  - $t_{PHL} \propto 2R_n C_L$
3-Input NAND Gate

rise-time: 1 transistor (simple)

fall-time: 3 transistor in series

for linear approximation: take $3 \times R_{on}$
If $\mu_n = 3\mu_p$
for equal fall and rise time:
Take $W_n = W_p$

If $\mu_n = 2\mu_p$
for equal fall and rise time:
Take $W_n = (3/2)W_p$
Design for Worst Case
3-input NAND Gate with Parasitic Capacitors
Worst Case Approximation
Using Lumped RC Model

(We ignore the constant term 0.69 or 1.22)

\[ t_{df} = \sum R_{\text{pulldown}} \times \sum C_{\text{pulldown}} \]

\[ = (R_{N1} + R_{N2} + R_{N3}) \times (C_a + C_b + (C_c + C_{p+load})) \]
Penfield-Rubenstein Model
(Elmore Delay Model)

\[ t_d = \sum R_i C_i \]

with:  \( C_i = \) capacitance at node \( i \)
\( R_i = \) total resistance between \( C_i \) and supply

\[ t_{df} = [R_{N1}C_a] + [(R_{N1} + R_{N2})C_b] + \\
[(R_{N1} + R_{N2} + R_{N3})(C_c + C_{p+load})] \]
Distributed RC Effects

\[ t_n = \frac{RC \times n(n+1)}{2} \approx \frac{nR\cdot nC}{2} \]

Worst case under lumped model: \( t_n = nR\cdot nC \)
Comparison

**RP-Model**

\[
 t_{df} = [R_{N1}C_a] + [(R_{N1} + R_{N2})C_b] + [(R_{N1} + R_{N2} + R_{N3})C_c] + \\
 n \text{ transistors in series} + [(R_{N1} + R_{N2} + R_{N3})C_{p+load}] \\
\]

\[
 R_N C \frac{n(n+1)}{2} + [(R_{N1} + R_{N2} + R_{N3})C_{p+load}] \\
\]

With \( R_{N1} = R_{N2} = R_{N3} = R_N \)

and \( C_a = C_b = C_c = C \)

**Lumped-Model**

\[
 R_N C n^2 + [(R_{N1} + R_{N2} + R_{N3})C_{p+load}] 
\]
Macro Modeling

\[ t_d = [R_{N1}C_a] + [(R_{N1}+R_{N2})C_b] + [(R_{N1} + R_{N2} + R_{N3})C_c] + \\
\quad [(R_{N1} + R_{N2} + R_{N3})C_p + [(R_{N1} + R_{N2} + R_{N3})C_{load}]] \]

- Internal delay
- External load

\[ t_d = T_{d, \text{internal}} + \lambda \times C_{load} \]
Effect of Loading

\[ t_d = t_{d,\text{internal}} + \lambda \times C_{\text{load}} \]
Effect of Fan-In and Fan-Out on Delay

\[ t_d = a_1 FI + a_2 FI^2 + a_3 FO \]

- **Fan-out**: number of gates connected
  - 2 gate capacitance per fan-out

- **Fan-in**: number of inputs to a gate
  - Quadratic effect due to increasing resistance and capacitance
$t_p$ as a function of Fan-In

$AVOID \ LARGE \ FAN-IN \ GATES! \ (Typically \ not \ more \ than \ FI < 4)$
Example
3-Input NAND gate with Parasitic Capacitors

$R_n = 0.5R_p = \frac{1}{2 \times 10^{-4}}$

$C_a = C_b = C_c = C_j = 0.05\text{pF}$

$C_p = 3C_j = 0.15\text{pF}$

$C_{load} = 2C_g = 0.20\text{pF}$
Worst Case Approximation by Lumped Model

\[ t_{dr} = R_p \times (C_c + C_{p+load}) = 10000 \times 0.4 \times 10^{-12} = 4.0 \text{ns} \]

\[ t_{df} = \sum R_{\text{pulldown}} \times \sum C_{\text{pulldown}} \]

\[ = (R_{N1} + R_{N2} + R_{N3}) \times (C_a + C_b + (C_c + C_{p+load})) \]

\[ = (3 \times 5000) \times (3 \times 0.05 + 0.15 + 0.20) \times 10^{-12} \]

\[ = 7.5 \text{ns} \]
Penfield-Rubenstein Model

\[ t_{dr} = R_p \times (C_c + C_{p+load}) = 10000 \times 0.4 \times 10^{-12} = 4.0\text{ns} \]

\[ t_{df} = [R_{N1}C_a] + [(R_{N1} + R_{N2})C_b] + [(R_{N1} + R_{N2} + R_{N3})(C_c + C_{p+load})] \]

\[ = 10000 \times 0.05\text{pF} + 10000 \times 0.05\text{pF} + 15000 \times 0.4\text{pF} = 6.75\text{ns} \]
Worst Case Approximation by Lumped Model

Make \( W_n = 2W_p \)

\[
\begin{align*}
\text{\( t_{dr} = R_p \times (C_c + C_{p+load}) = 10000 \times 0.45 \times 10^{-12} = 4.5\text{ns} \)}
\end{align*}
\]

\[
\begin{align*}
\text{\( t_{df} = \sum R_{\text{pulldown}} \times \sum C_{\text{pulldown}} \)}
\end{align*}
\]

\[
\begin{align*}
&= (R_{N1} + R_{N2} + R_{N3}) \times (C_a + C_b + (C_c + C_{p+load})) \\
&= (3 \times 2500) \times (3 \times 0.10 + 0.15 + 0.20) \times 10^{-12} \\
&= 4.875\text{ns}
\end{align*}
\]
Penfield-Rubenstein Model

Make $W_n = 2W_p$

$t_{dr} = R_p \times (C_c + C_{p+load}) = 10000 \times 0.45 \times 10^{-12} = 4.5\text{ns}$

$t_{df} = [R_{N1}C_a] + [(R_{N1} + R_{N2})C_b] + [(R_{N1} + R_{N2} + R_{N3})(C_c + C_{p+load})]$

$= 2500 \times 0.10\text{pF} + 5000 \times 0.10\text{pF} + 7500 \times 0.45\text{pF} = 4.125\text{ns}$
Rewriting Penfield-Rubenstein Equation

\[ t_d = [R_{N1}C_a] + [(R_{N1} + R_{N2})C_b] + \\
[ (R_{N1} + R_{N2} + R_{N3})(C_c + C_{p+load})] \]

\[ t_d = [R_{N1}(C_a + C_b + C_c + C_{p+load})] + \\
[ R_{N2} (C_b + C_c + C_{p+load})] + \\
[ R_{N3}(C_c + C_{p+load})] \]

\[ t_d = \sum R_{ii}C_{\text{downstream-}i} \]

with:  \( C_{\text{downstream-}i} = \) downstream capacitance at node \( i \)
\( R_{ii} = \) resistance at node \( i \)
Progressive Sizing

- When parasitic capacitance is significant (e.g., when fan-in is large), needs to consider distributed RC effect
- Increasing the size of M1 has the largest impact in terms of delay reduction
- $M_1 > M_2 > M_3 > \ldots > M_N$
Delay Optimization by Transistor Ordering

Critical signal next to supply

Critical signal next to output