EE456: Digital Integrated Circuit Design and Analysis

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or by appointments

Grading Policy

- 2 Mid-terms + quizzes will account for 60% of the grade. Final will account for 40%. Exams are mandatory and have to be taken on the scheduled day of the exam.
- You are guaranteed an A if your weighted average score over exams, quizzes, is 90 or above.
- Any form of cheating will be heavily penalized and reported to the Dean of students and may result in a failing grade.

Text and References

- Text:
  - *Digital Integrated Circuits: A Design Perspective*,
    J. Rabaey et. al., Prentice Hall, Second edition
- References:
  - *Principles of CMOS VLSI Design: A Systems Perspective*,
    2nd Ed.,
    N. H. E. Weste and K. Eshraghian, Addison Wesley
  - *Circuits, Interconnects, and Packaging for VLSI*,
    H. Bakoglu, Addison Wesley
- Class Notes:

Conferences & Journals

- IEEE Transactions on VLSI Systems
- IEEE Transactions on CAD of IC's
- IEEE Journal of Solid State Circuits
- IEEE VLSI Circuits Symposium
- Journal of Electronic Testing
- ACM Design Automation Conference
- IEEE International Conference on CAD
- IEEE Solid State Circuits Conference
- International symposium on Low-Power Electronics & Design
- IEEE Conference on Computer Design
- IEEE International Test Conference

Course Outline

- Introduction: Historical perspective and Future Trend
- CMOS Process
- CMOS Logic, Layout techniques
- MOS devices, SPICE models
- Inverters: transfer characteristics, static and dynamic behavior, power and energy consumption of static MOS inverters
- Designing combinational logic gates in CMOS
  - Static CMOS design: Complementary CMOS, ratioed logic, pass-transistor logic
  - Dynamic CMOS logic

Course Outline (Cont'd)

- Designing combinational logic gates (Cont'd)
  - Power consumption in CMOS gates
  - Low-power design
- Designing sequential circuits
- Interconnect and timing issues
- Designing memory and array structures
- Designing arithmetic building blocks

Introduction:
A Historical Perspective and Future Trends

References:

Adapted from*: Digital Integrated Circuits: A Design Perspective*,
J. Rabaey © UCB

Principles of CMOS VLSI Design: A Systems Perspective,
2nd Ed., N. H. E. Weste and K. Eshraghian

Electronics Market

United States Sales (1987)

(Billions of Dollars)

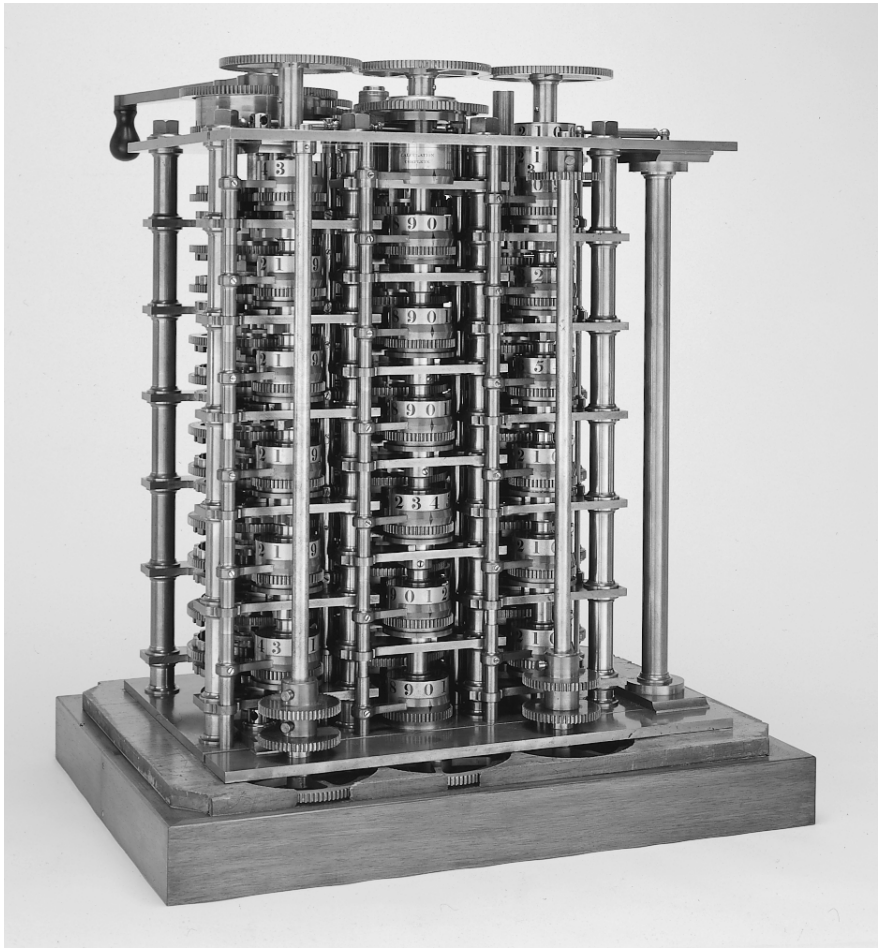
Chemicals	215
Electronics	235
Automobiles	201
Machinery	156
Petroleum	130

Worldwide Electronics Market

(Billions of Dollars)

	1988	1992
Europe	139	182
Japan	246	360
USA	246	332
Other	127	200
	770	1074

The First Computer



- The Babbage Differential Engine (1834)
- 25,000 mechanical parts
- Cost £17,470

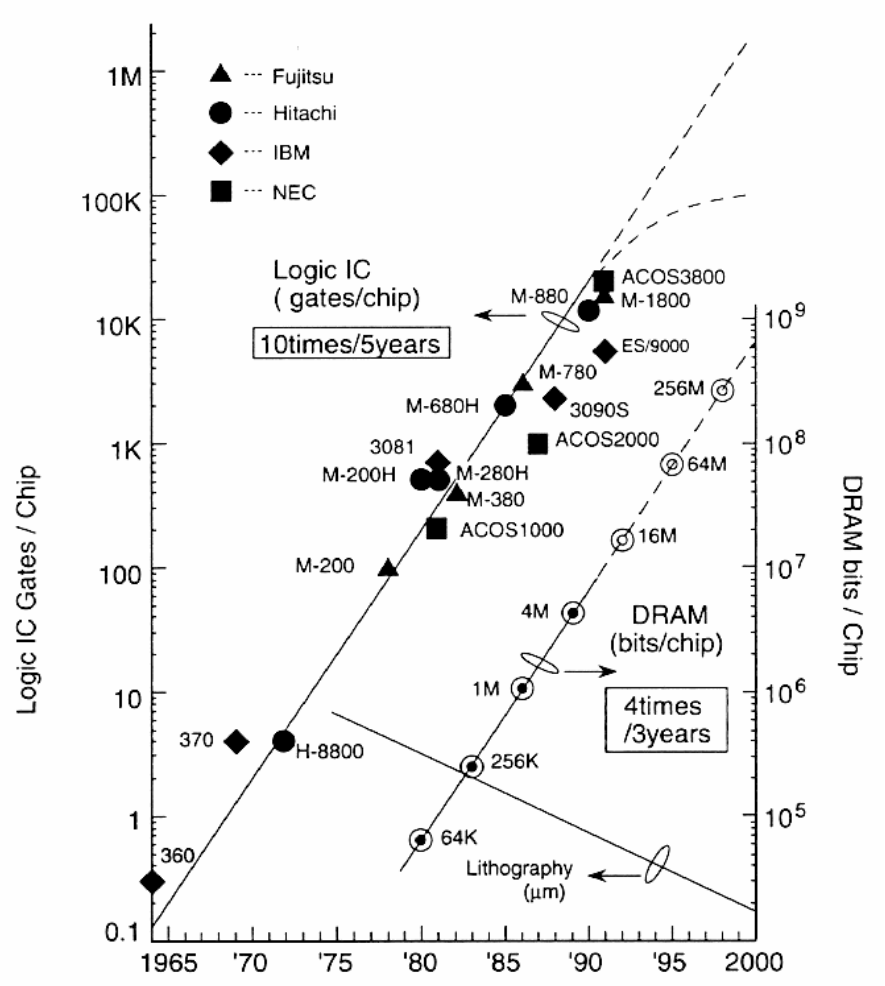
Digital Electronic Computing

- Started with the introduction of vacuum tube
- ENIAC for computing artillery firing tables in 1946
- Integration density
  - 80 feet long, 8.5 feet high, and several feet wide
  - 18,000 vacuum tubes
- Reliability issues and excessive power consumption
- Did not go far until the invention of the transistor at Bell Lab in 1947

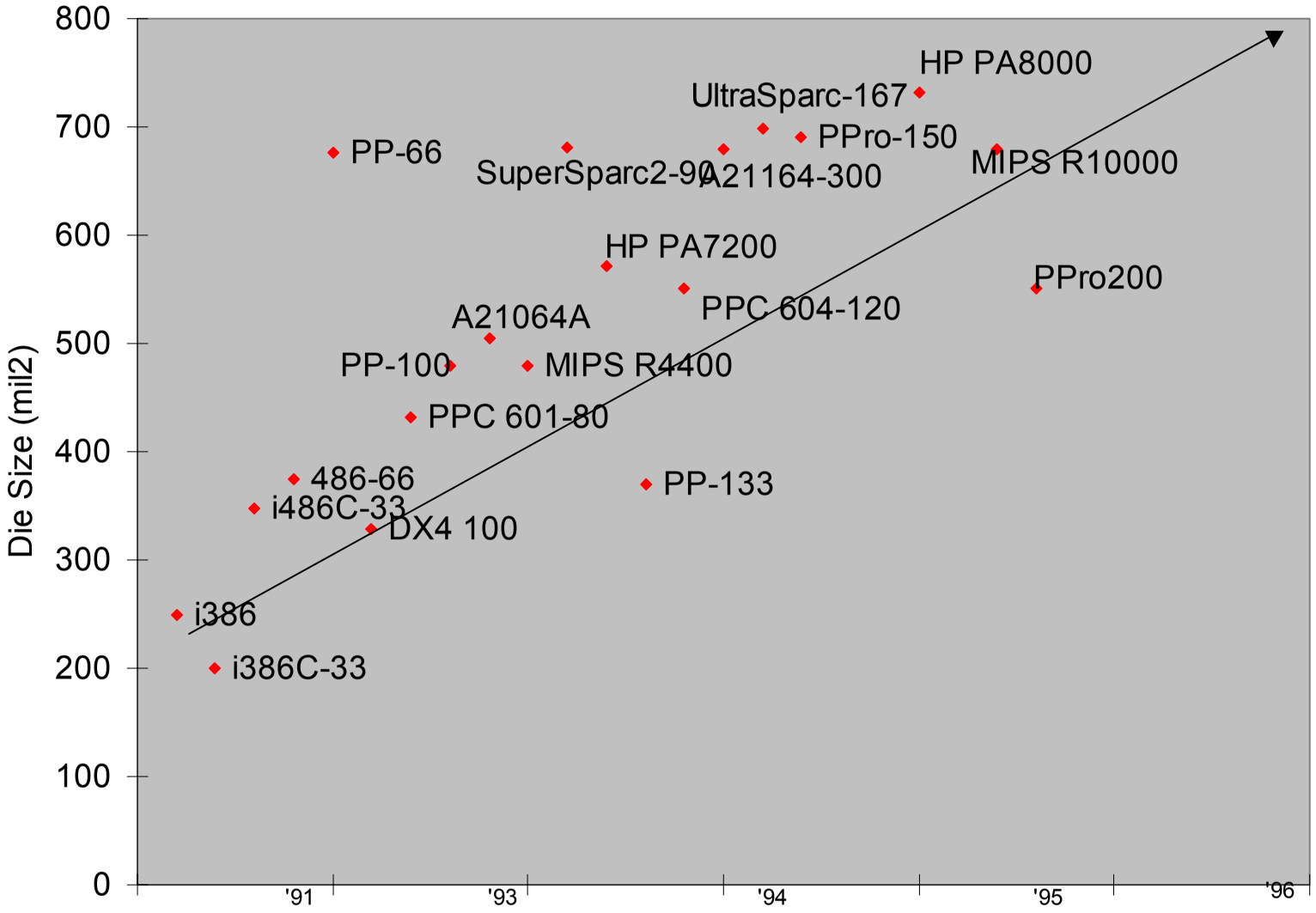
HISTORY

- MOS field-effect transistor: Lilienfeld (1925), Heil (1935)
- Bipolar transistors: Bardeen (1947), Schockley (1949)
- First Bipolar digital logic: Harris (1956)
  - IC Logic family:
    - Transistor-Transistor Logic (TTL) (1962)
    - Emitter-Coupled Logic (ECL) (1971)
    - Integrated Injection Logic (I^2L) (1972)
- PMOS and NMOS transistors on the same substrate: Weimer (1962), Wanlass (1965)
- PMOS-only logic until 1971 when NMOS technology emerged
- NMOS-only logic until late 1970s, when CMOS technology took over
- Later developments: BiCMOS, GaAs, low-temperator CMOS, super-conducting technologies, Nano-electronic

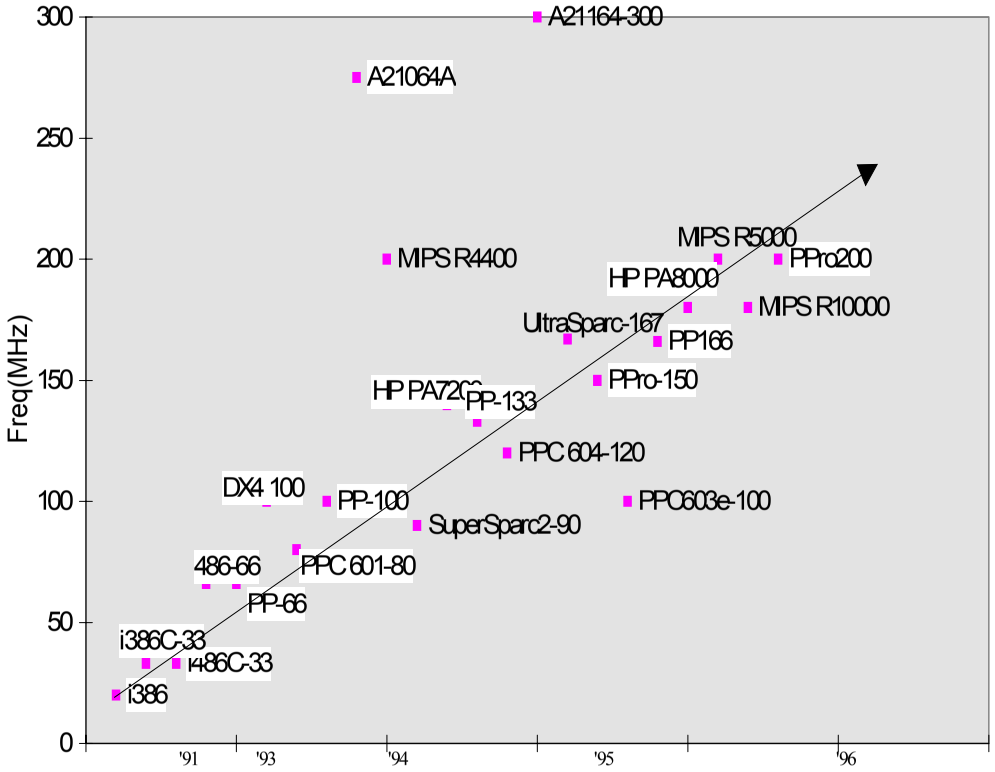
Evolution in Complexity



Processor Trends



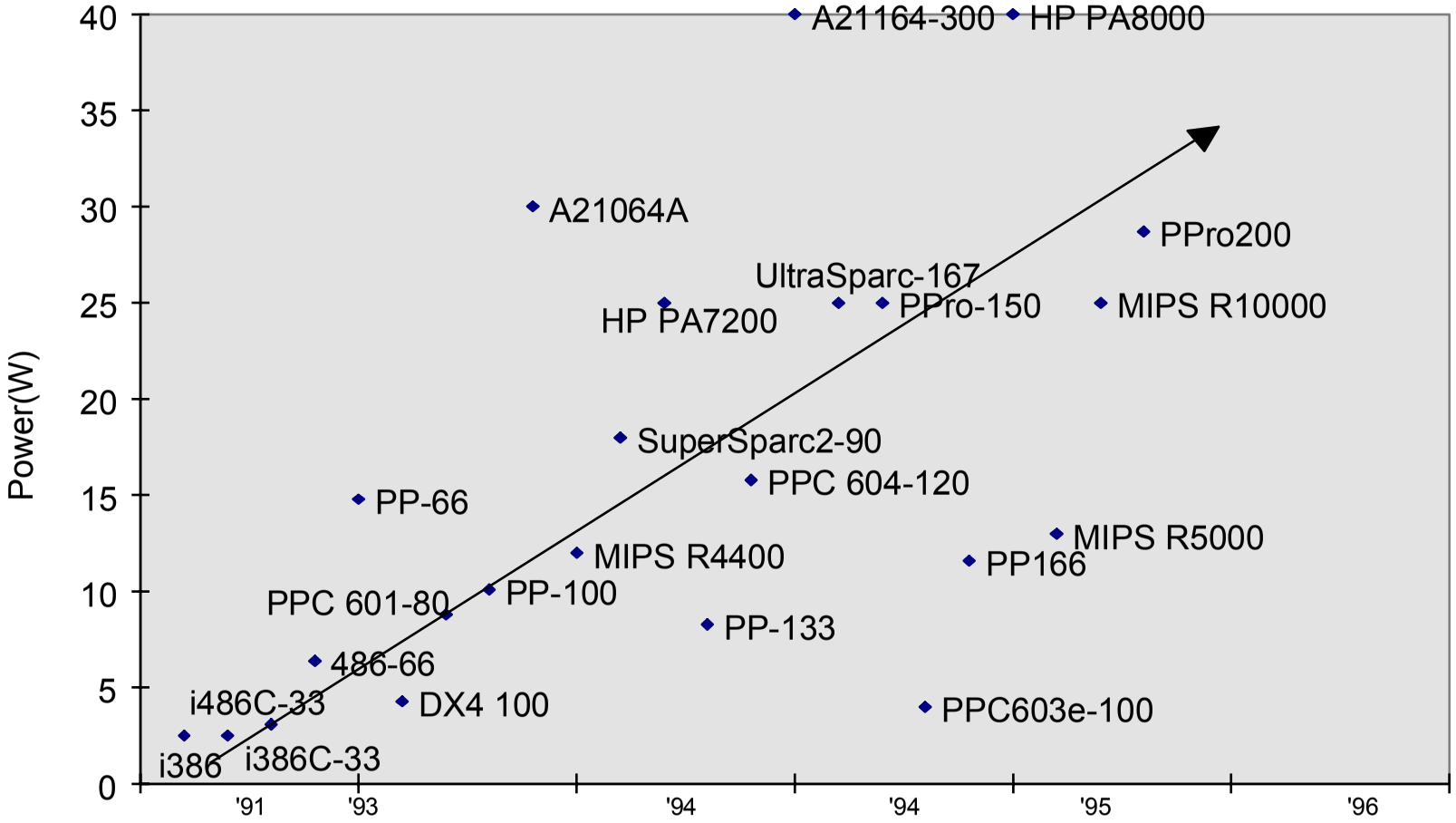
Processor Trends (cont'd)



Higher Performance:

- Higher Frequencies (2x/Generation)
- Higher Device counts (2x /Generation)

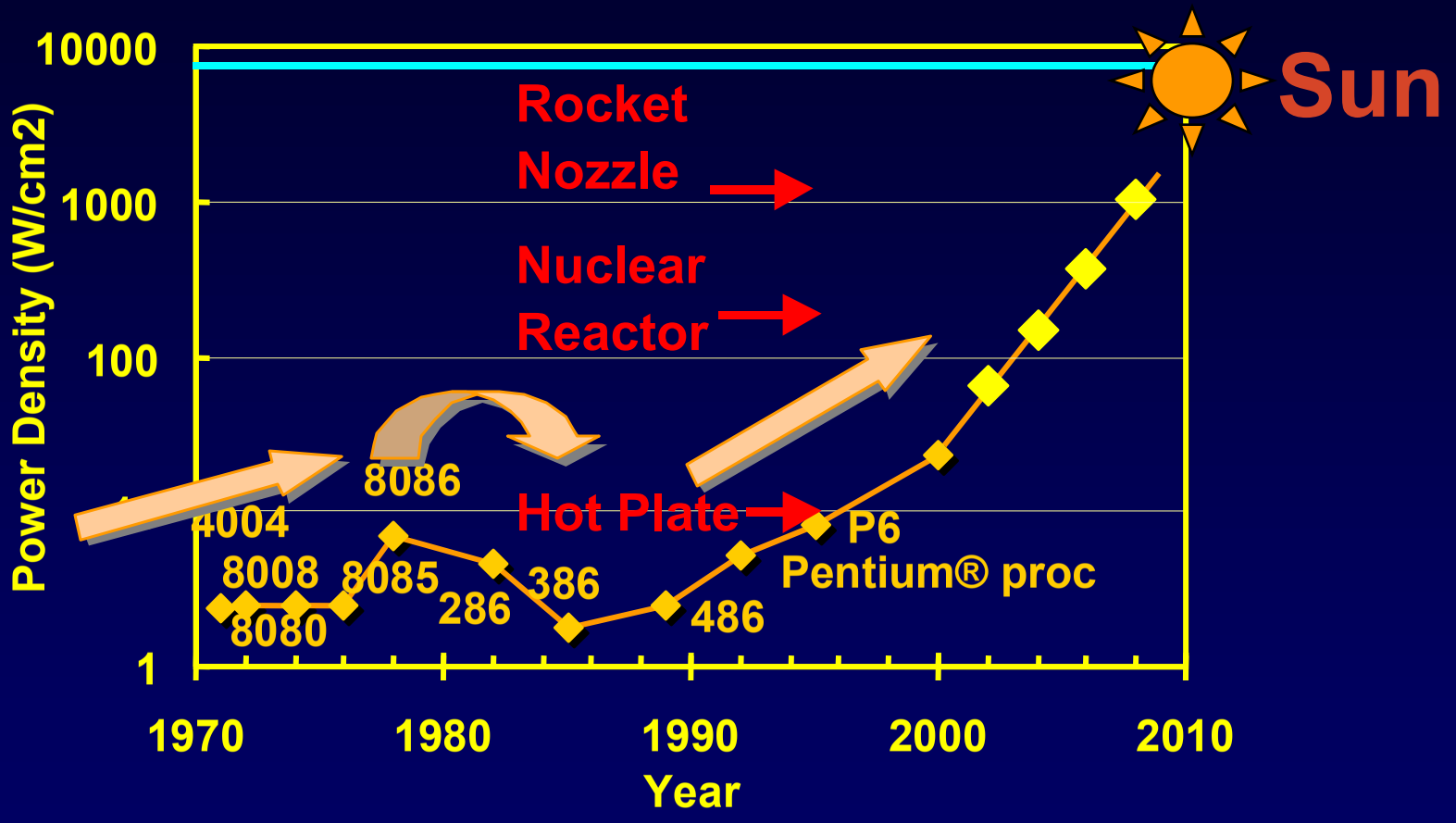
Power Trends



[Source: Microprocessor Report]

2x Performance Increase ==> 2x power increase

Power density will increase



Power density too high to keep junctions at low temp

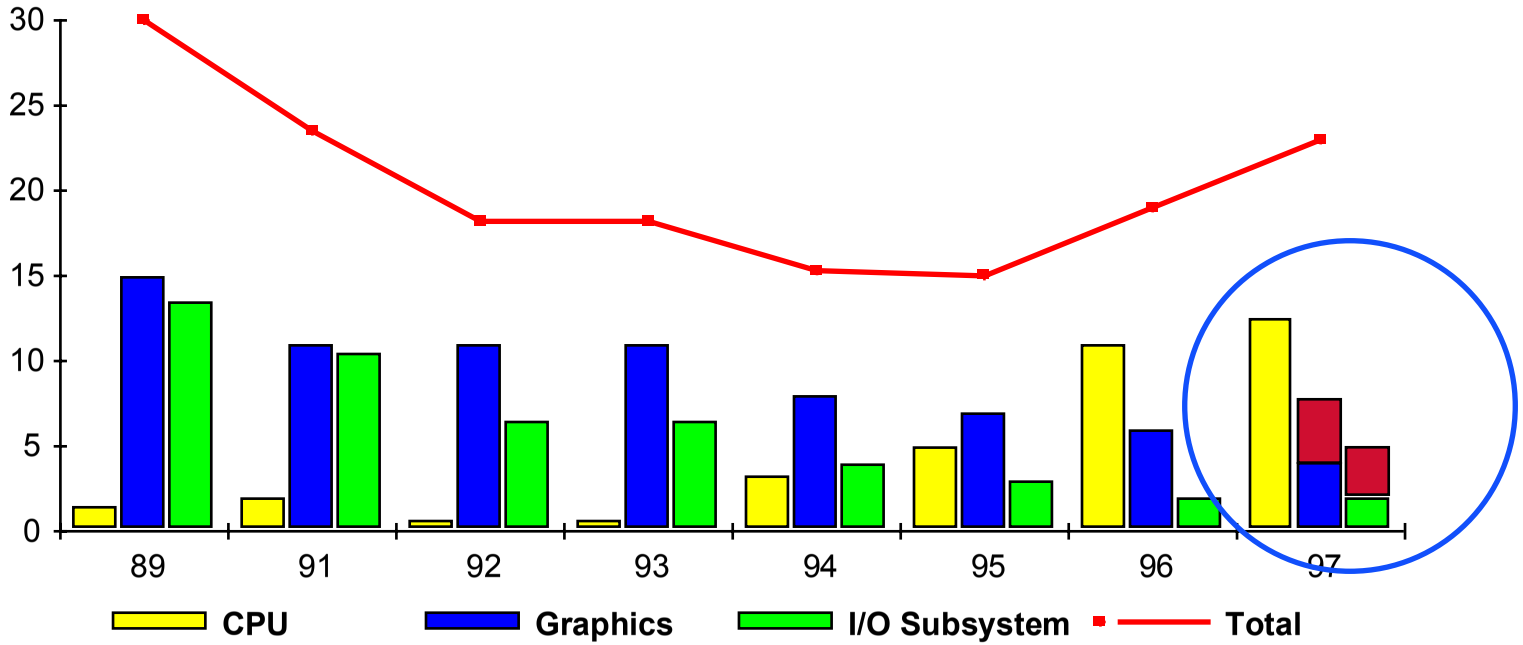
Heat Dissipation

- Chips fail when they get hot
- Need compact and cost-effective cooling solns

CPU	Thermal Soln Cost
486/33mhz	HeatSink $0.50
486DX2 66mhz	Heatsink $1.00
Pentium 66mhz	Larger Heatsink $2.00 System Fan $4.00

- Cooling Solns will become more exotic/expensive
  - Extruded Heatsinks, Heatpipes, Blowers, Noise....
- Every Watt impacts System Cost, esp. for HVM

Where is the Power Going? (Mobile PC)

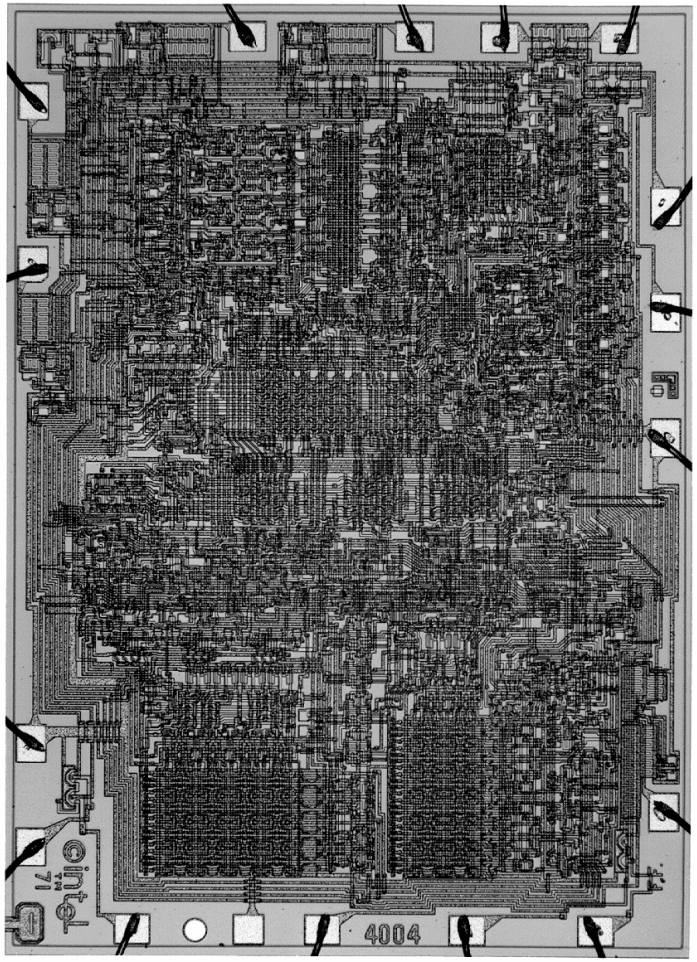


CPU Power: predicted from average device count/area growth

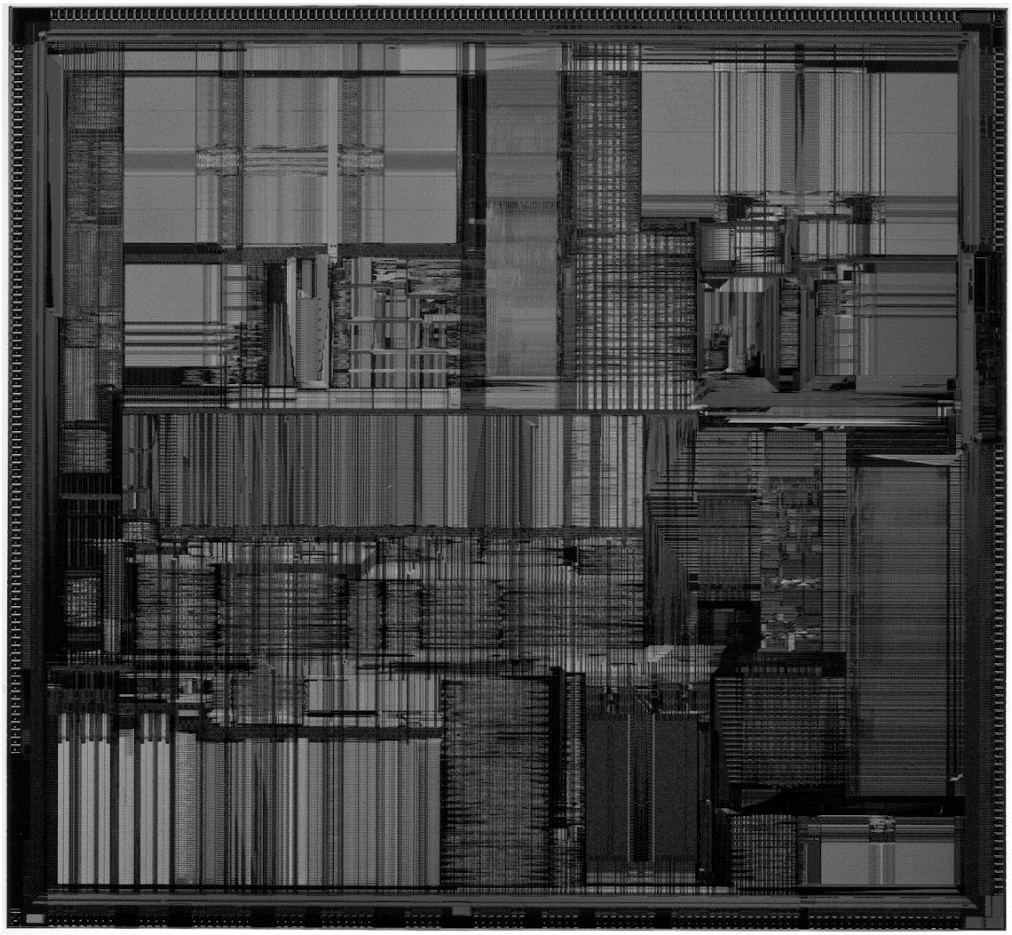
- CPU Power increasing (Predicted in 1994 Low power workshop)
- Graphics & Chipset Power increasing faster than predicted

Power reduction is not only a CPU problem

Intel 4004 Microprocessor



Intel Pentium (II) Microprocessor



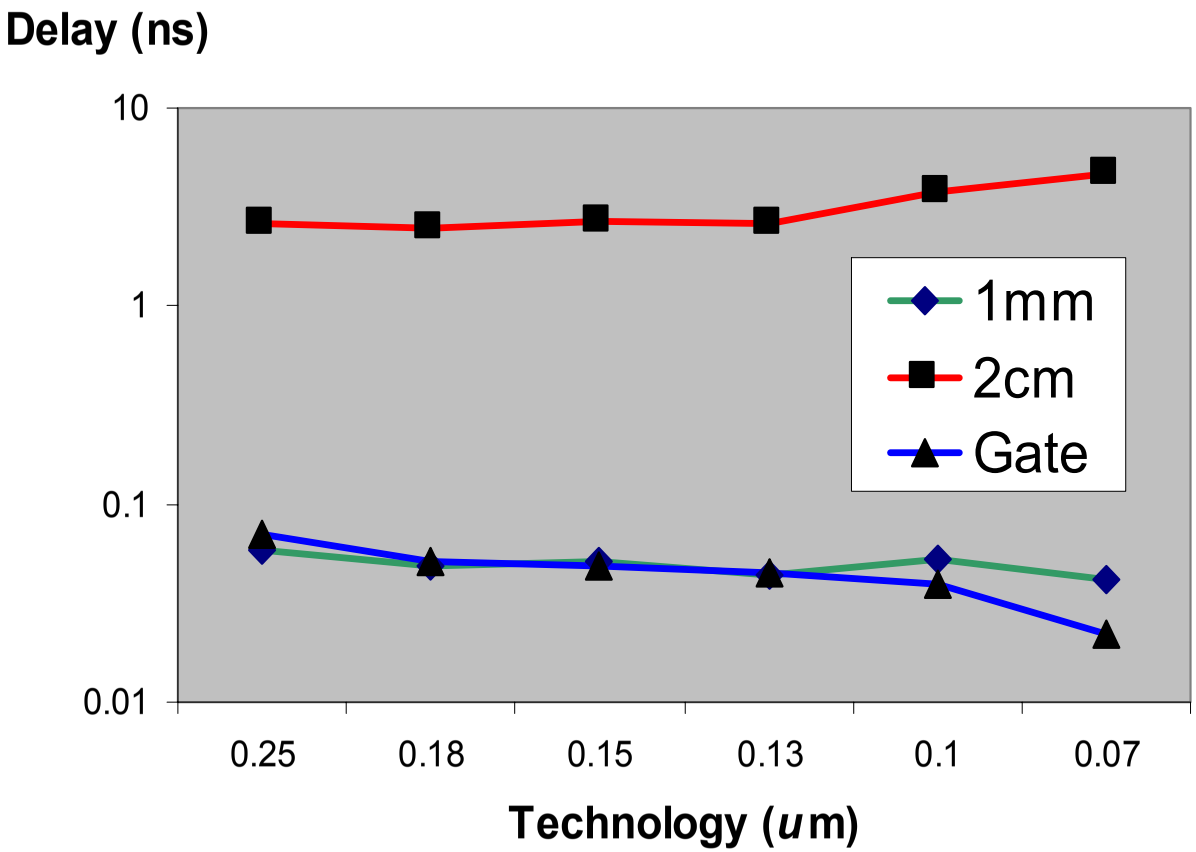
National Technology Roadmap for Semiconductor (NTRS)

Technology (um)	***0.25***	***0.18***	***0.13***	***0.10***	***0.07***
Year	1998	2001	2004	2007	2010
# transistors	28M	64M	150M	350M	800M
On-Chip Clock (MHz)	450	600	800	1000	1100
Area (mm^2)	300	360	430	520	620
Wiring Levels	5	5-6	6	6-7	7-8

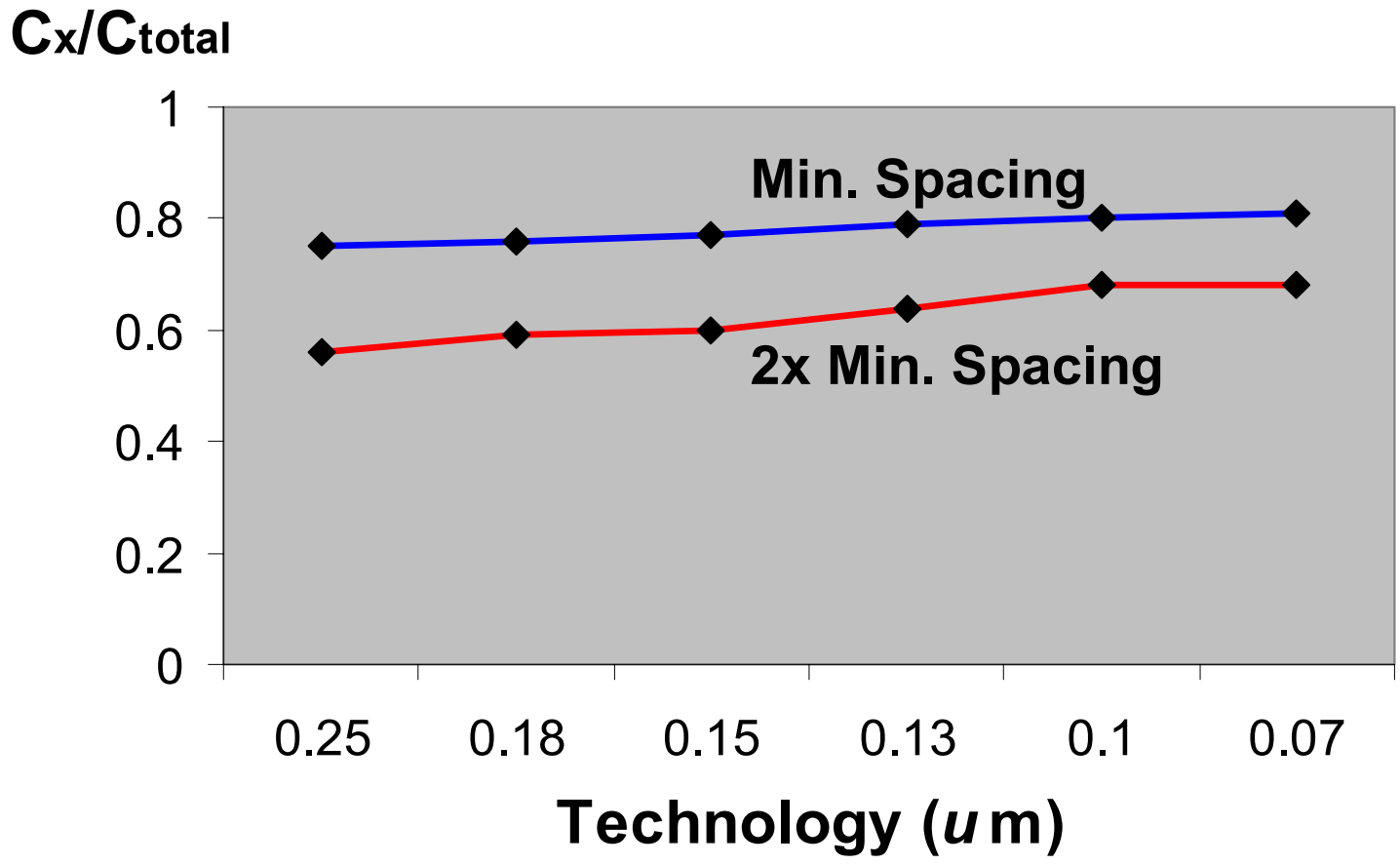
Interconnect Performance Trend

Technology (um)	***0.25***	***0.18***	***0.15***	***0.13***	***0.10***	***0.07***
2cm line delay (ns)	2.589	2.480	2.650	2.620	3.730	4.670
1mm line delay (ns)	0.059	0.049	0.051	0.044	0.052	0.042
Intrinsic gate delay (ns)	0.071	0.051	0.049	0.045	0.039	0.022

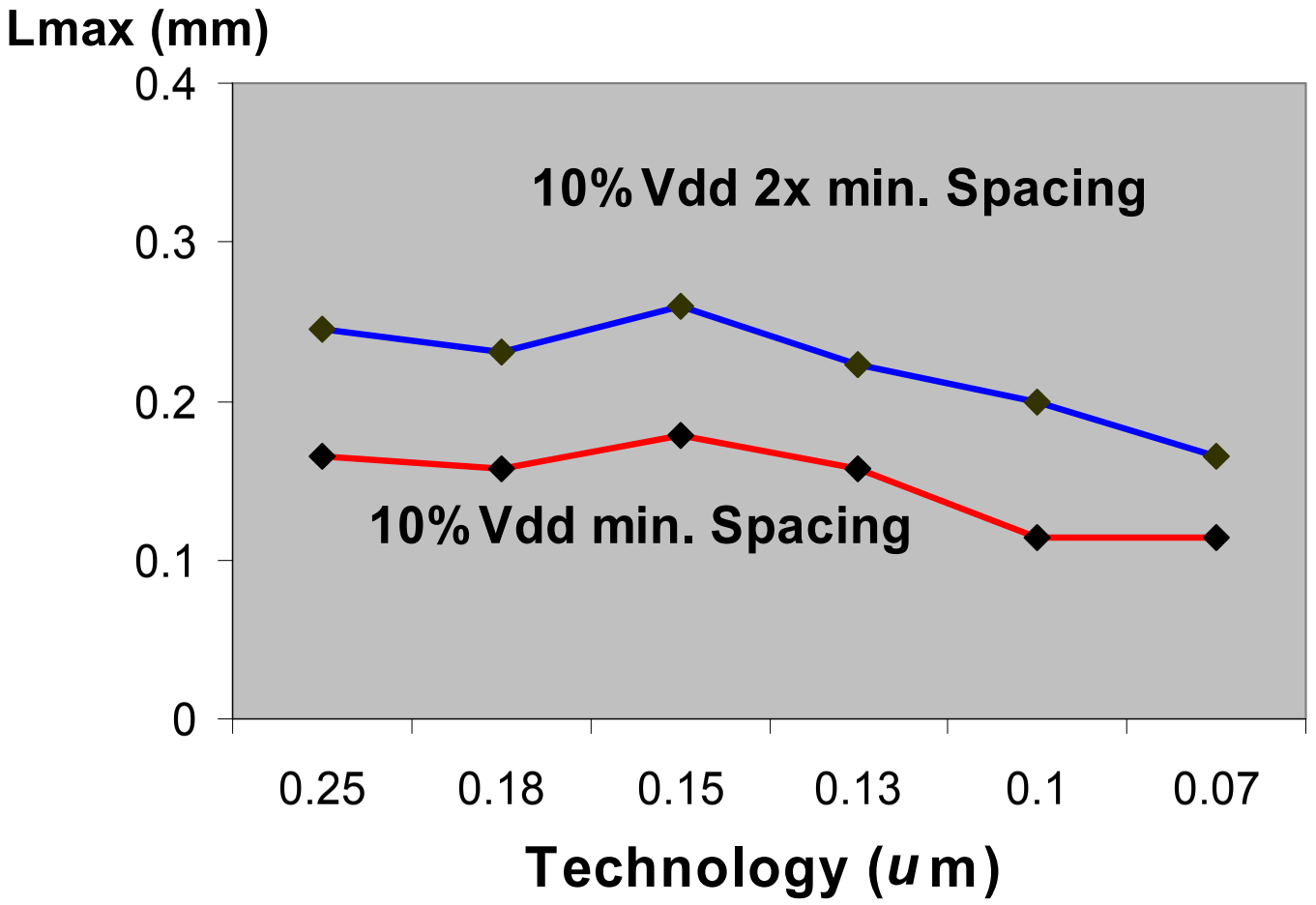
Interconnect Performance Trend



Significance of Coupling Capacitance



Coupling Noise

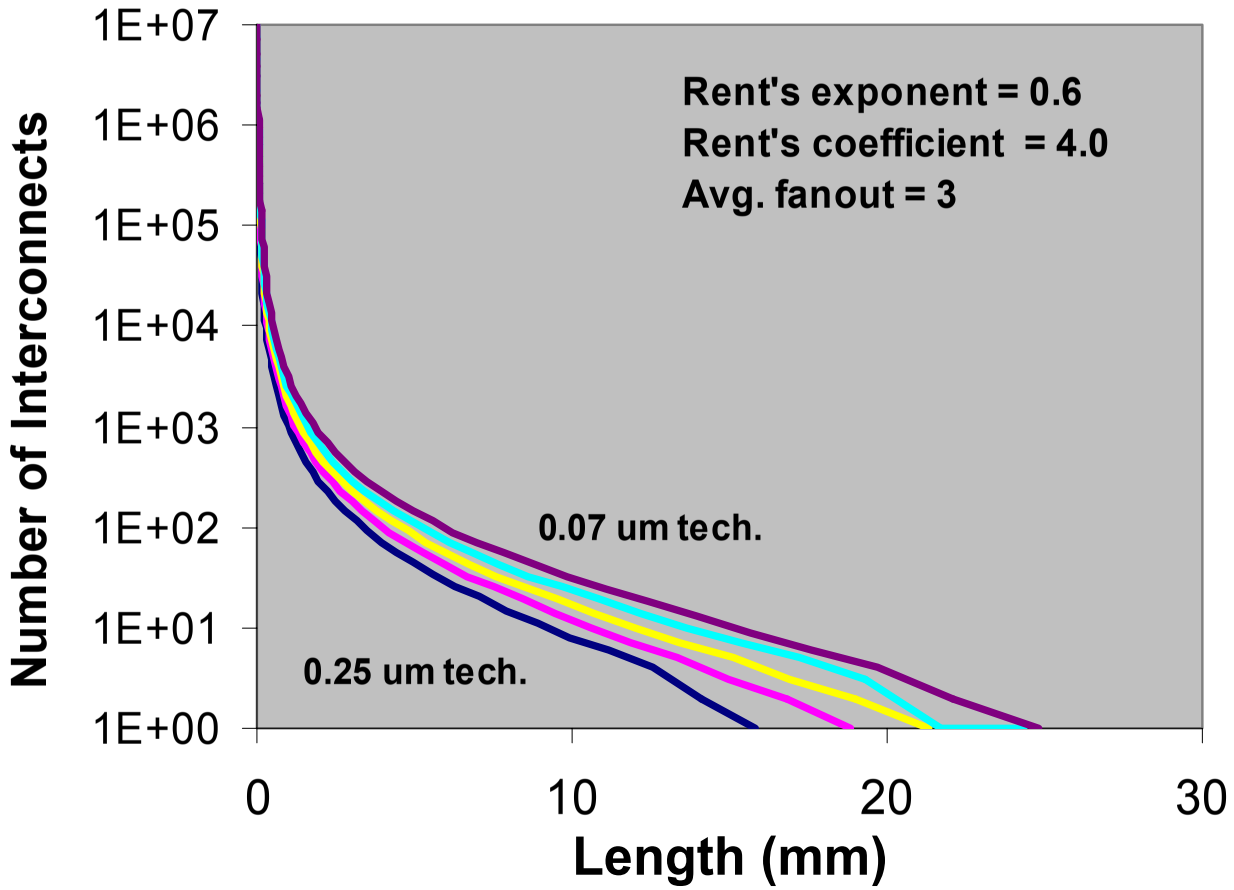


Interconnect Complexity

Technology (um)	*0.25*	*0.18*	*0.13*	*0.10*	*0.07*
Length (m)	820	1,480	2,840	5,140	10,000
Wiring Levels	6	6-7	7	7-8	8-9
Opt. # buffers per net	few	→	→	→	many
Opt. # wiresizes per net	few	→	→	→	many
Opt. # buffers per chip	5K	25K	54K	230K	797K

- Performance
- Signal reliability
- Electromigration

Distributions of Wire lengths

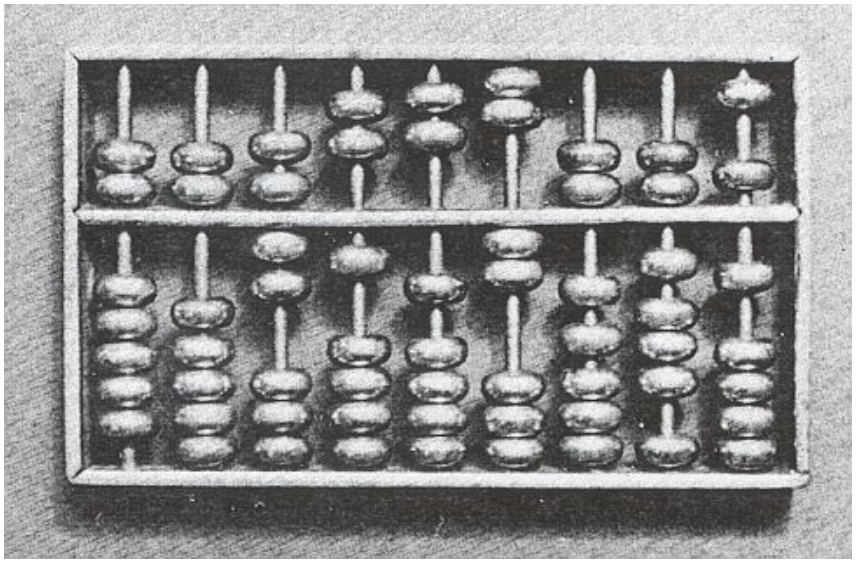


Constituents of the Information Theory

- Constituents of the Information Theory
  - Sender and recipient
  - Symbols (microstates) as elementary units of information
- Information carriers

Information is physical!

The Abacus, an ancient digital calculating device



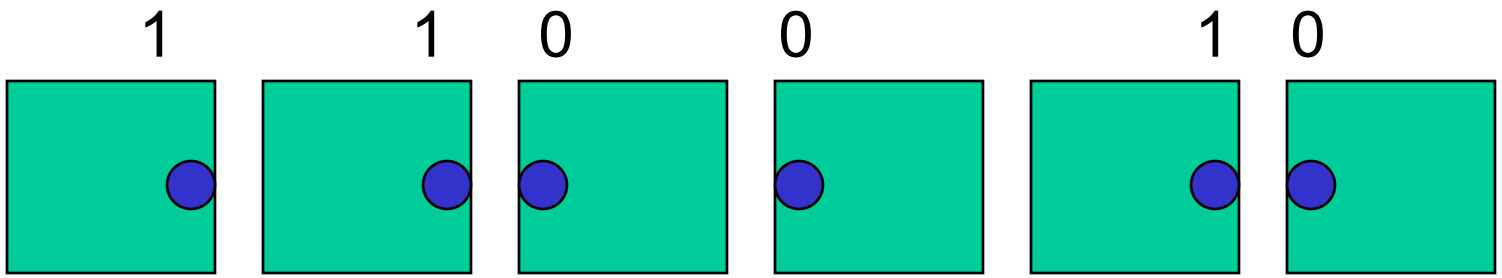
Information is represented in digital form

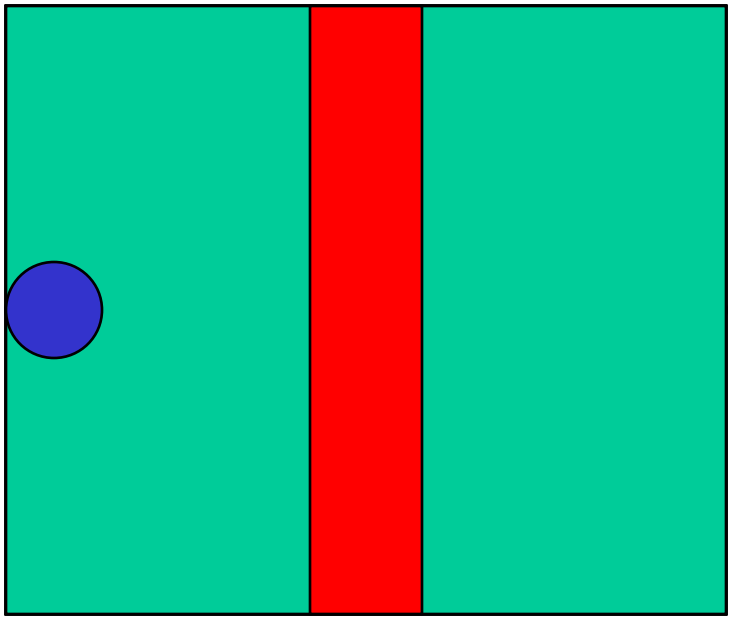
Each column denotes a decimal digit

Binary representation: two possible positions for each bead

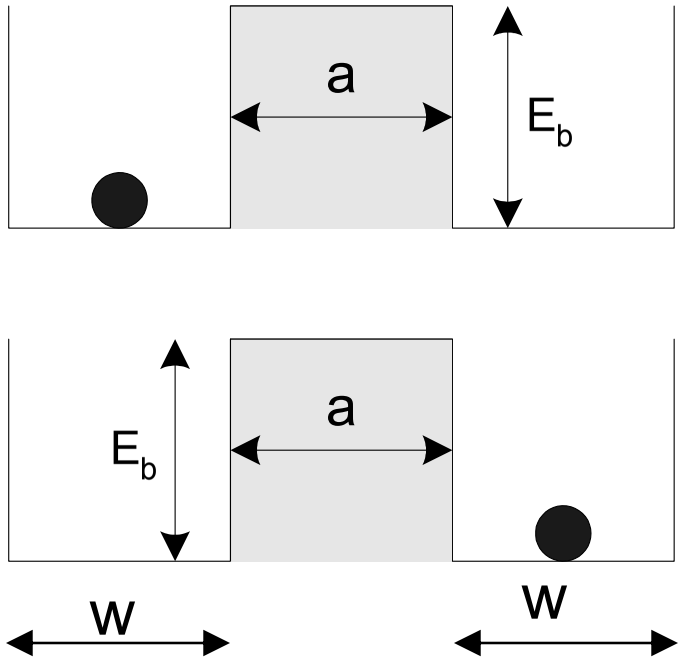
A bead in the abacus is a memory device, not a logic gate

Particle Location is an Indicator of State





Two-well bit



A physical system as a computing medium

- We need to create a bit first. Information processing always requires physical carrier, which are material particles.

- *First* requirement to physical realization of a bit implies creating *distinguishable* states within a system of such material particles.

- *The second* requirement is *conditional* change of state.

- The properties of *distinguishability* and *conditional change of state* are two fundamental properties of a material subsystem to represent information. These properties can be obtained by creating *energy barriers* in a material system.

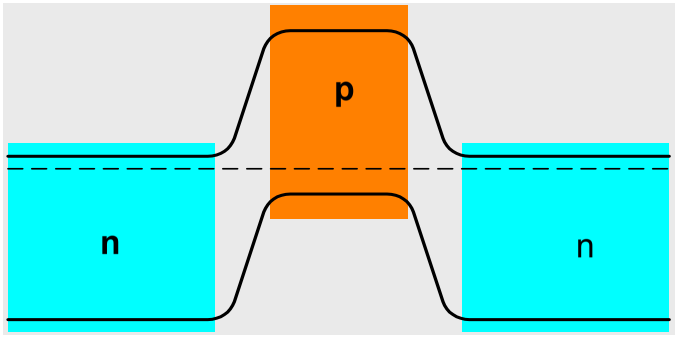
Kroemer's Lemma of Proven Ignorance

- If in discussing a semiconductor problem, you cannot draw an Energy-Band-Diagram, this shows that *you don't know what are you talking about*

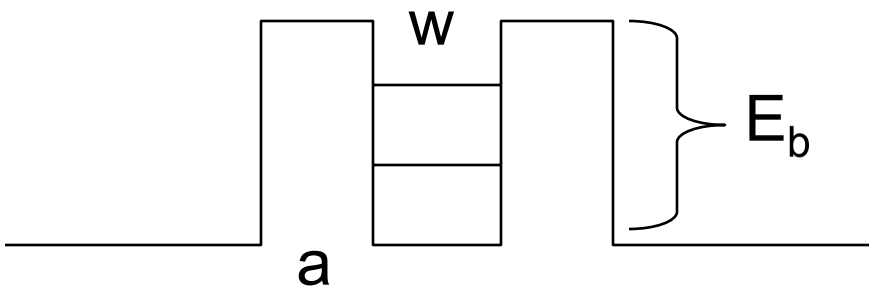
- If you can draw one, but don't, then *your audience won't know what are you talking about*

Barrier engineering in semiconductors

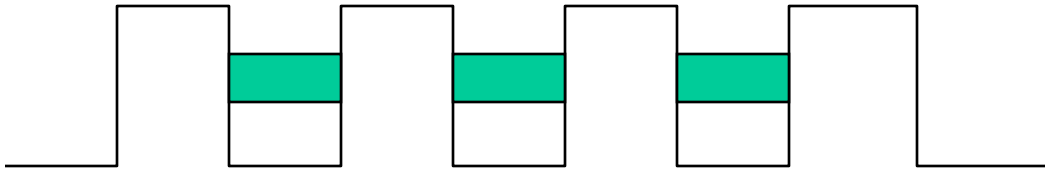
By doping, it is possible to create a built-in field and energy barriers of controllable height and length within semiconductor. It allows one to achieve conditional complex electron transport between different energy states inside semiconductors that is needed in the physical realization of devices for information processing.



Heterojunction barriers



Double barrier



Superlattice

Ideal von Neumann's Computer

Designers and Users want:

- Highest possible integration density (*n*)
  - *To keep chips size small and increase yields*
  - *To increase functionality*
- Highest possible speed (*f=1/t*)
  - *Speed sells!*
- Lowest possible power consumption (*P*)
  - *Decrease demands for energy*
  - *The generation of too much heat means costly cooling systems*

Binary Information Throughput (BIT)

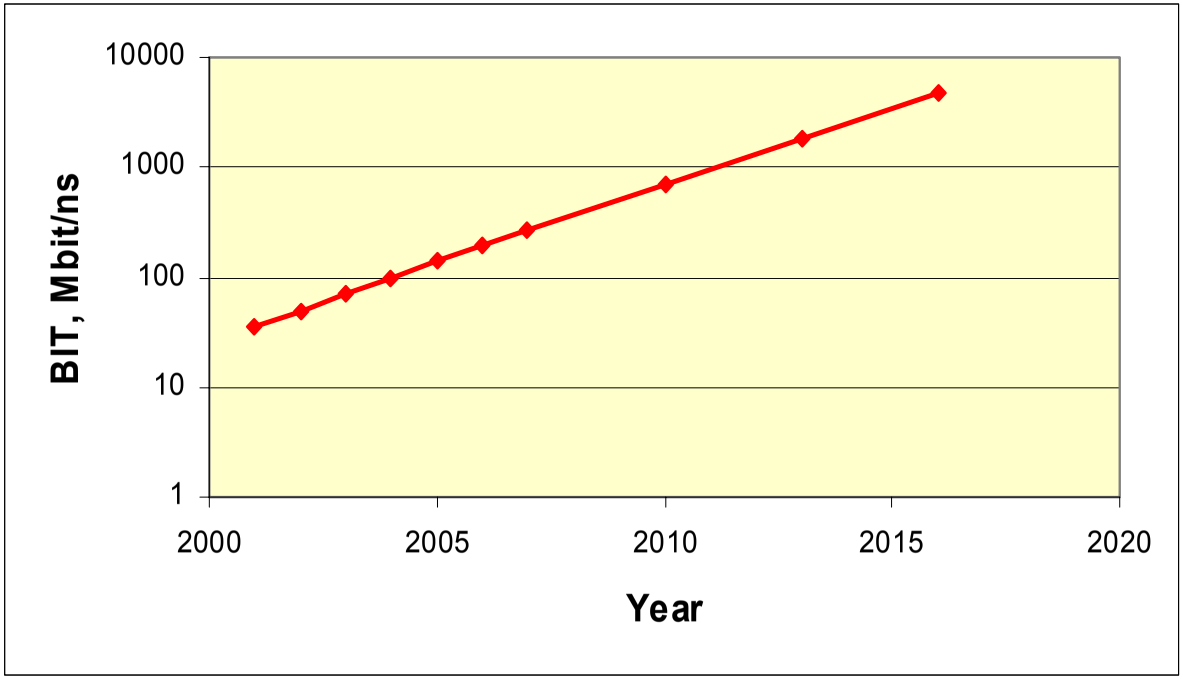
BIT is the maximum number of binary transition per unit time

$$BIT = n_{bit} f$$

- one measure of computational capability

n_{bit} – the number of binary states (e.g. transistors)

f-switching frequency



Energetics of Computation

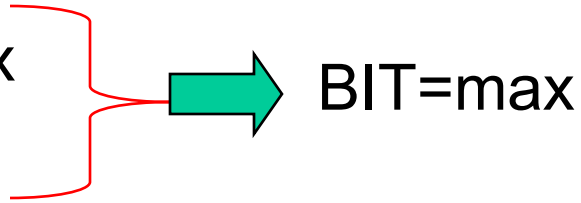
$$P = E_{bit} n f$$

Requirements for an ideal computer:

(integration density) n=max

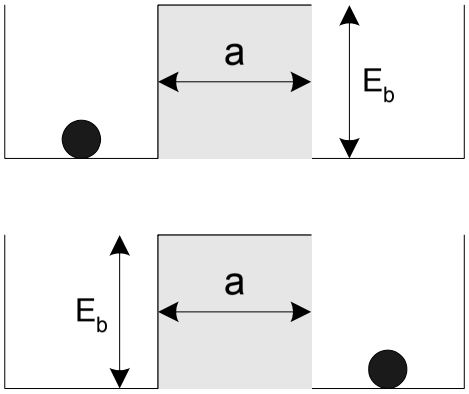
(switching frequency) f=max

(power) P=min



Lowest Barrier: Distinguishability Barrier

Distinguishability ***D*** implies low probability Π of spontaneous transitions between two wells (error probability)



***D=max*, Π=0** ***D=0*, Π=0.5 (50%)**

Classic distinguishability:

$$\Pi_{classic} = \exp(-\frac{E_b}{k_B T})$$

Minimum distinguishable barrier: Π=0.5

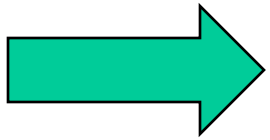
$$\frac{1}{2} = \exp(-\frac{E_b}{k_B T}) \Rightarrow E_b = kT\ln 2$$

Shannon - von Neumann - Landauer limit

Smallest Size:
The Heisenberg Barrier

$$\Delta x \Delta p \geq \hbar$$

$$\Delta E \Delta t \geq \hbar$$



$$a_{crit} = \frac{\hbar}{\sqrt{2mE_b}}$$

$$t_{\min} = \frac{\hbar}{E_b}$$

$$E_b = kT\ln 2$$

Classic and Quantum Distinguishability @ Π=0.5

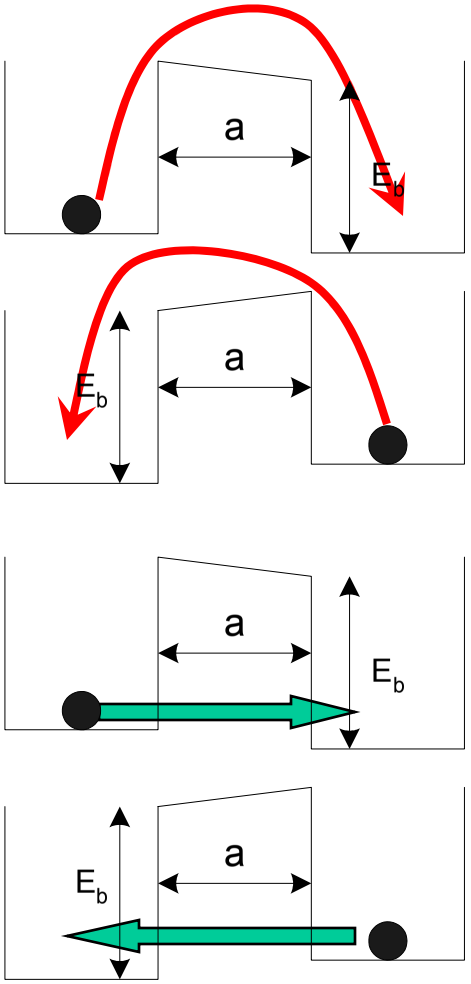
$$\Pi_{classic} = \exp(-\frac{E_b}{k_B T})$$

$$E_b^{\min} = k_B T \ln 2$$

WKB: (Tunneling)

$$\Pi_{quantum} = \exp(-\frac{2\sqrt{2m}}{\hbar} a\sqrt{E_b})$$

$$E_b^{\min} = \frac{\hbar^2 \ln^2 2}{8ma^2}$$



Technology Scaling

Technology scaling improves:

- **Transistor & interconnect performance**
- **Transistor density**
- **Energy consumed per switching transition**

0.7X scaling factor (30% scaling) results in:

- **30% gate delay reduction (43% freq. ↑)**
- **2X transistor density increase (49% area ↓)**
- **Energy per transition reduction**

Technology Scaling

- Speed & Performance
  - High drive current and low parasitics
  - Low gate delay and high frequency
- Density & Area
  - Small feature size
- Power & Reliability
  - Low power supply voltage
  - Low off-state leakage

Technology Generation Scaling

$$Dimensions \xrightarrow{scale} 0.7,\ V_{dd} \xrightarrow{scales} \beta,\ V_t \xrightarrow{scales} \beta$$

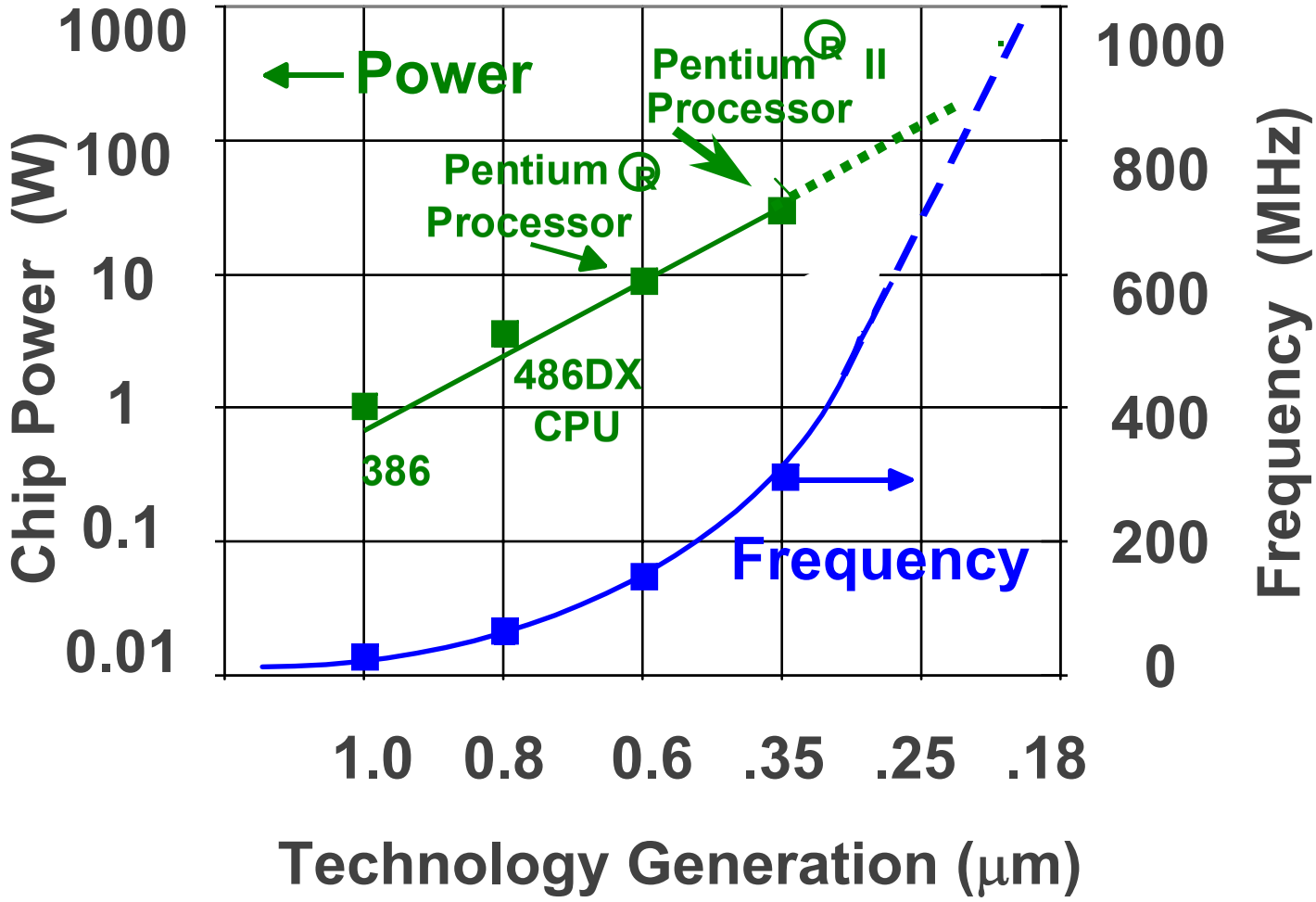
$$I = \frac{kW}{T_{ox}}(V_{dd} - V_t) \xrightarrow{scales} \frac{0.7}{0.7} \times \beta = \beta$$

$$D = \frac{CV_{dd}}{I} \xrightarrow{scales} \frac{0.7 \times \beta}{\beta} = 0.7 \quad \text{(30\% delay reduction)}$$

$$E = CV_{dd}^{\ 2} \xrightarrow{scales} 0.7\beta^{\ 2}$$

IC Frequency & Power Trends

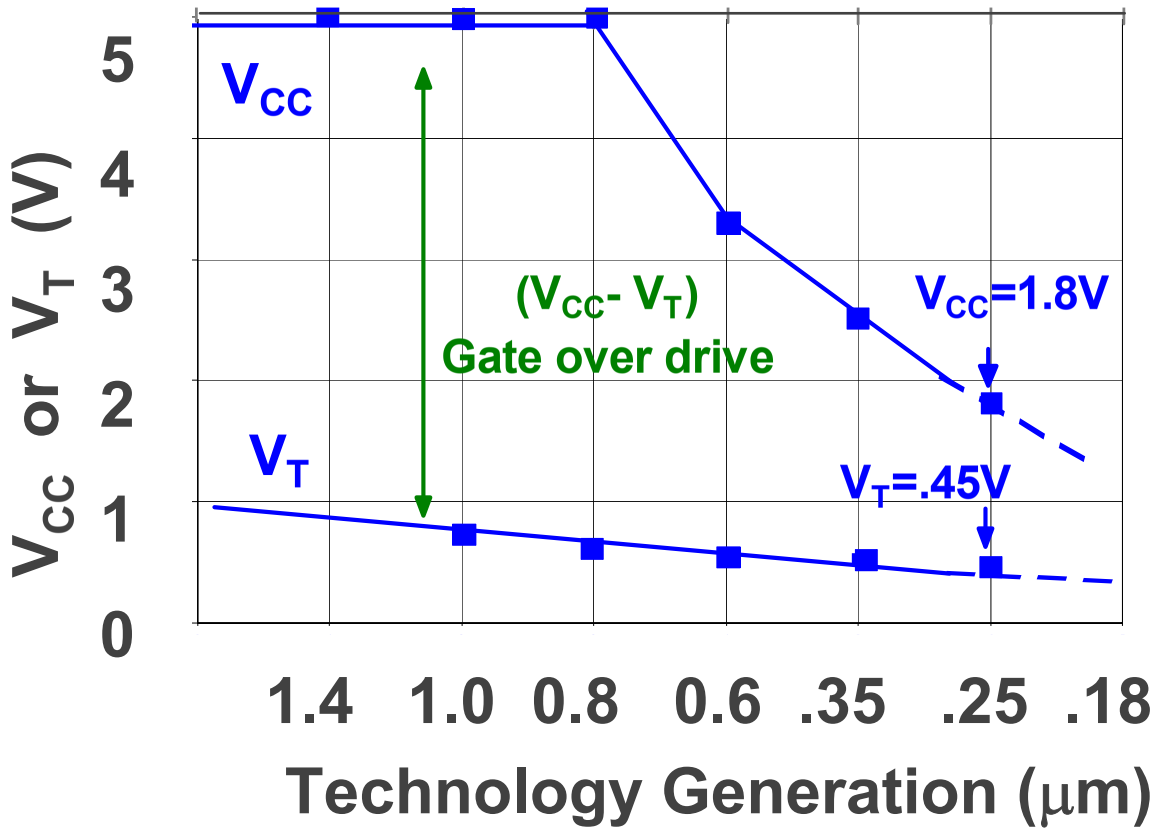
- Clock frequency improves 50%
- Gate delay improves ~30%
- Power increases 50%
- Power = $C_L V^2 f$



↑ Active switched capacitance "C_L" is increasing.

Constant Voltage vs Field Scaling

- Recently: constant e-field scaling, aka voltage scaling
- V_{CC} ⌫ 1V
- V_{CC} & modest V_T scaling
- Loss in gate overdrive (V_{CC}-V_T)



Voltage scaling is good for controlling IC's active power, but it requires aggressive V_T scaling for high performance

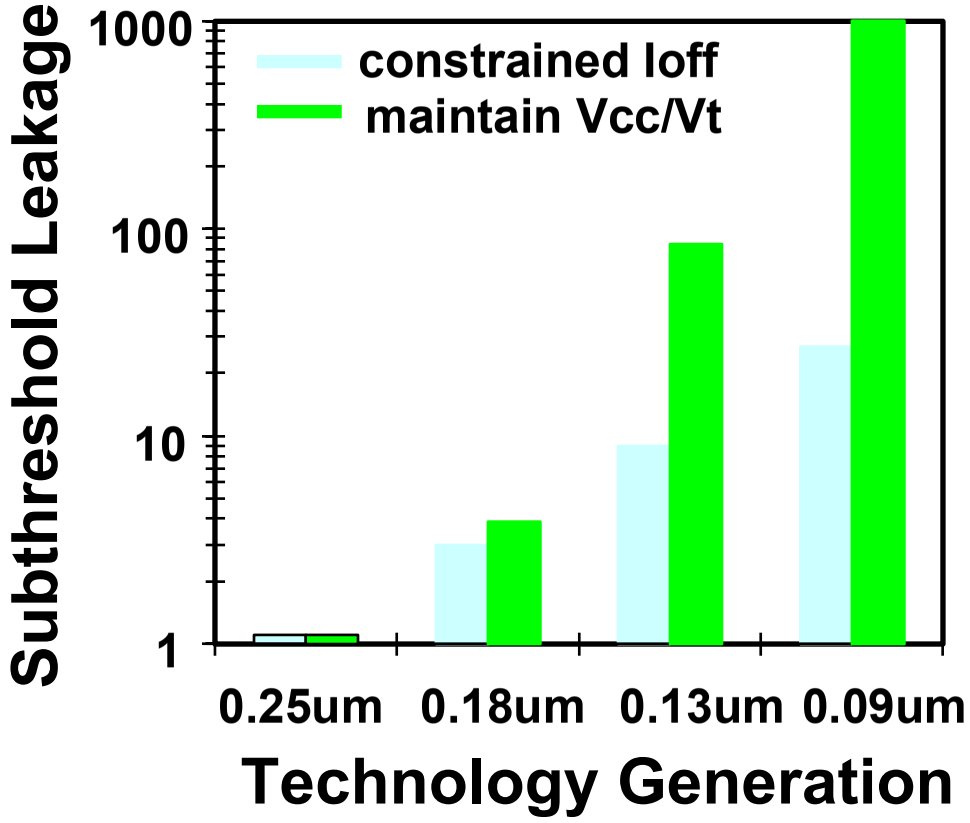
Barriers to Voltage Scaling

Voltage Scaling = Constant Electric Field Scaling

⬇ Voltage scaling is good for IC's active power, but degrades gate over drive. Requires V_T scaling.

- Leakage power
- Short-channel effects
- Special circuit functionality, noise
- Soft error
- Parameter variation

Barriers to Voltage Scaling



- Leakage power
- Short-channel effects
- Soft error
- Special circuit functionality

Delay

$$\tau_d = \frac{C_L V_{DD}}{I_D}$$

$$\tau_d = \frac{C_L}{(\frac{W}{2L})\mu C_{ox} V_{DD}(1-\frac{V_T}{V_{DD}})^2}$$ Long Channel MOSFET

$$\tau_d = \frac{C_L}{WC_{ox}\upsilon_{SAT}(1-\frac{V_T}{V_{DD}})}$$ Short Channel MOSFET

$$\tau = \frac{CL^{0.5} T_{ox}^{0.5}}{V_{DD}^{0.3}(0.9 - V_T/V_{DD})^{1.3}} (\frac{1}{W_n} + \frac{2.2}{W_p})$$ [1]

[1] C. Hu, "Low Power Design Methodologies," Kluwer Academic Publishers, p. 25.

Performance significantly degrades when V_{DD} approaches $3V_T$.

V_T Scaling: V_T and I_{OFF} Trade-off

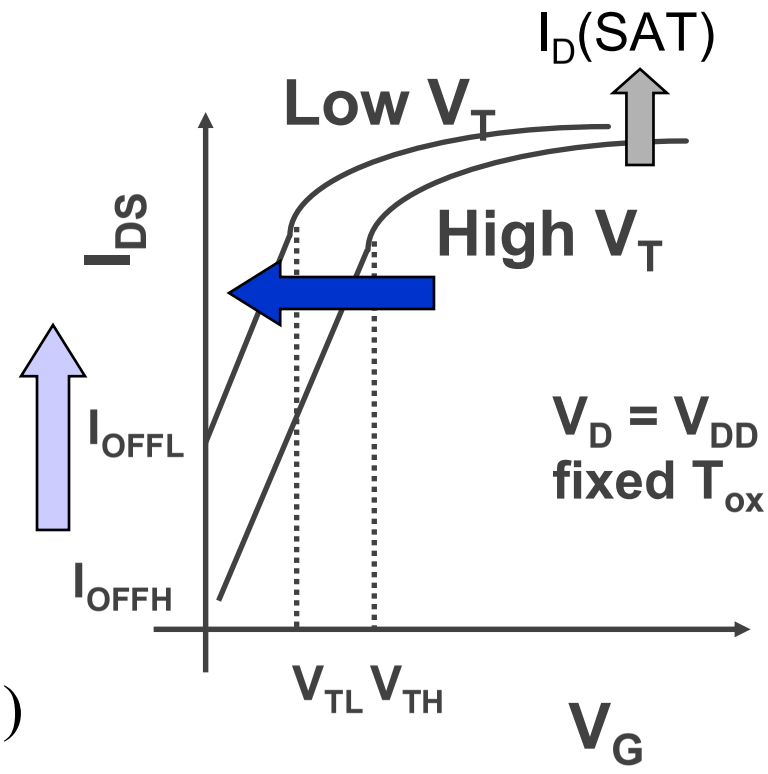
Performance vs Leakage:

$V_T \downarrow I_{OFF} \uparrow I_D(SAT) \uparrow$

$$I_{OFF} \propto I_{subth} \propto \frac{W_{eff}}{L_{eff}} K_1 e^{(V_{GS}-V_T)}$$

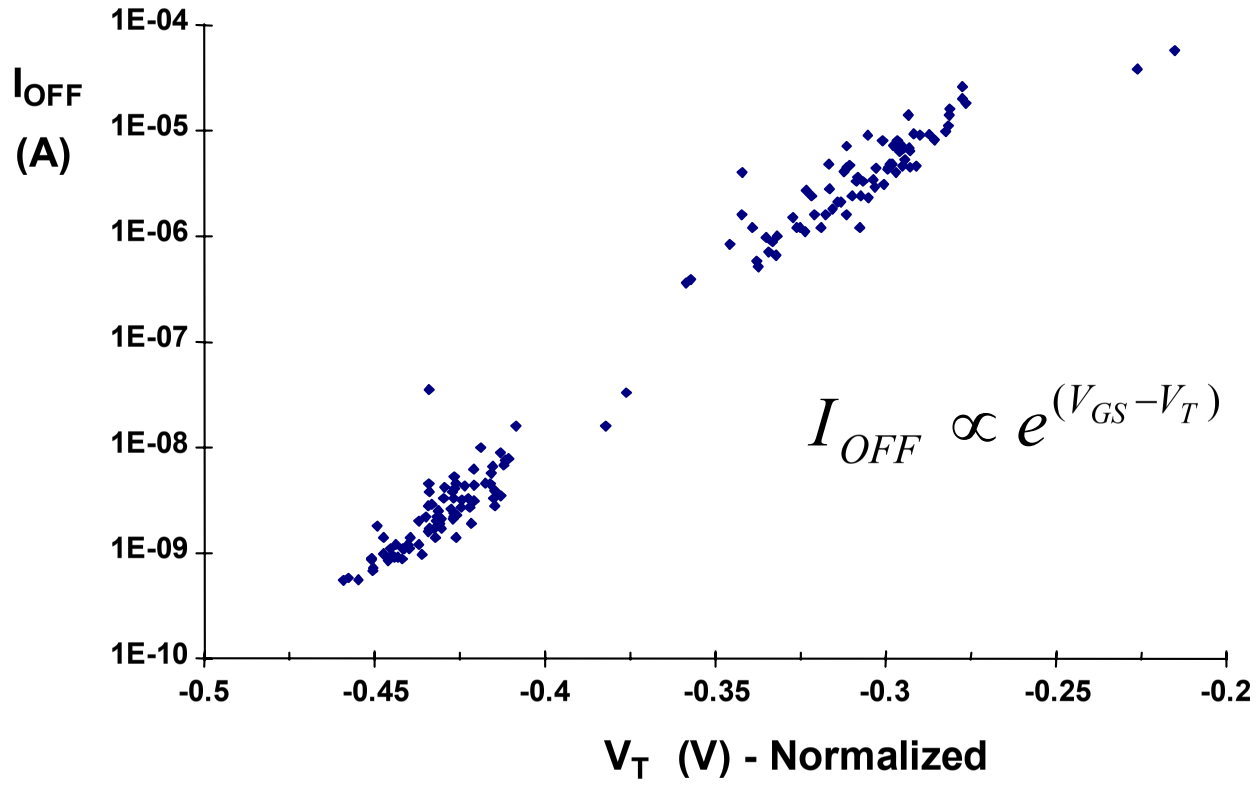
$$I_D(SAT) \propto \frac{W_{eff}}{L_{eff}} K_2 (V_{GS}-V_T)^2$$

$$I_D(SAT) \propto K_3 W_{eff} C_{ox} \upsilon_{SAT} (V_{GS}-V_T)$$



- As V_T decreases, sub-threshold leakage increases
- Leakage is a barrier to voltage scaling

I_{OFF} vs V_T

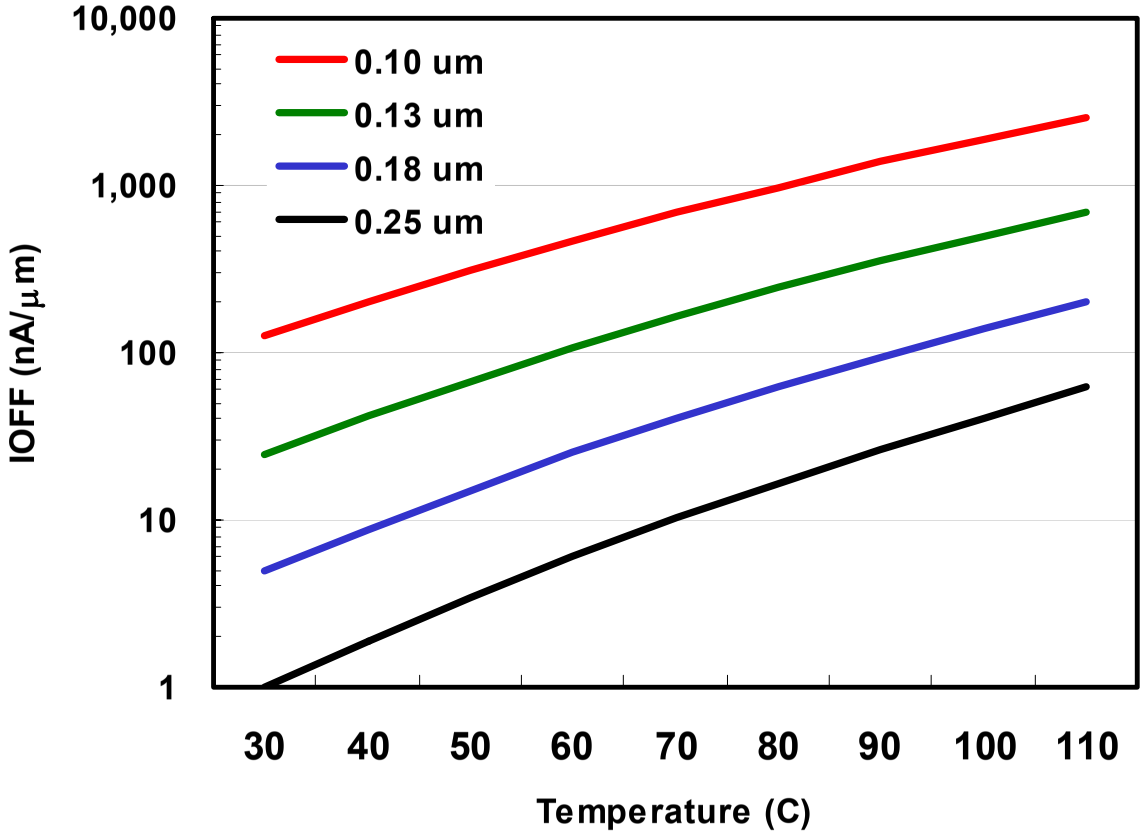


Log I_{OFF}

V_{TP} (V)

I_{OFF} is an exponential function of V_T.

Future: Projected Leakage Trends



I_{OFF} (0.25um) = 1 nA/um (scales 5X)
V_T (0.25um) = 450 mV (scales by 15%)

S_t (30C) = 80 mV/dec
S_t (100C) = 100
d V_T/dT = 0.7 mV/C

A Technology Scaling Barrier

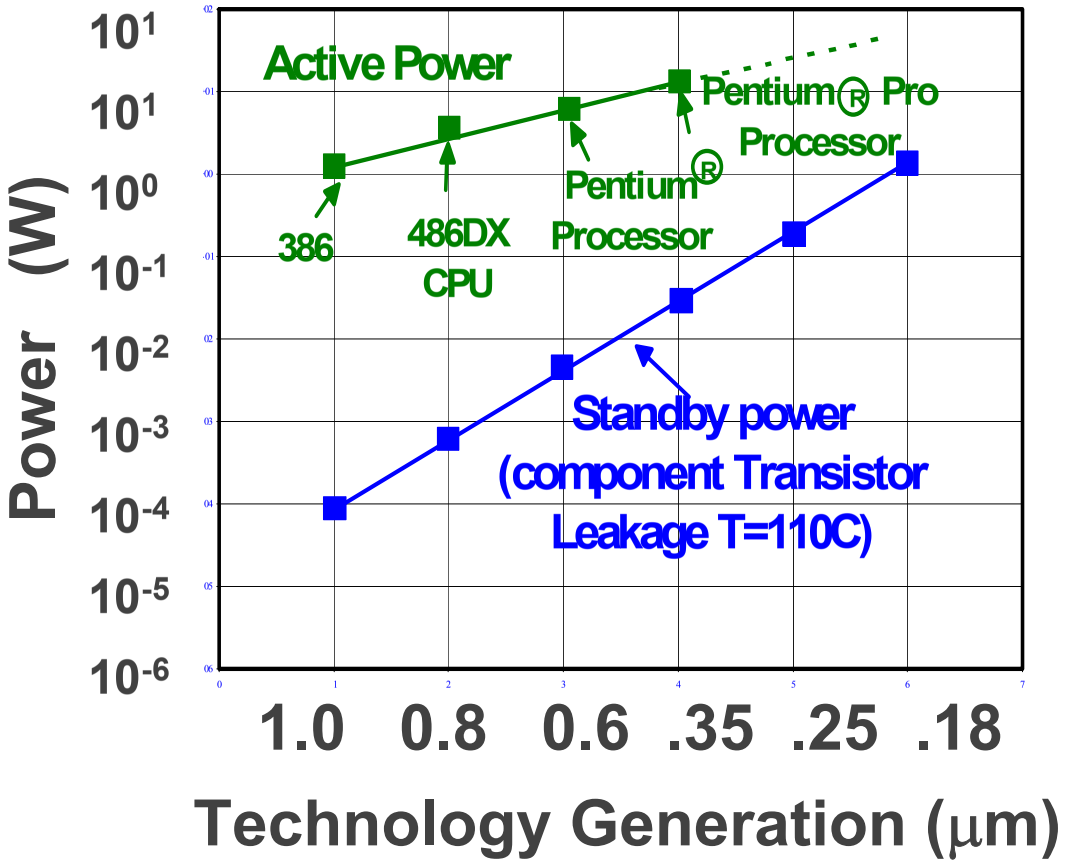
- Constant electric field scaling (V_{CC} scaling) to control IC's active power
- Loss in gate overdrive $(V_G-V_T)^n$
- Subthreshold leakage increases with V_T scaling

V. De et al., 1999.
A. Keshavarzi et al., 1997.
S. Thompson et al., 1997.
B. Davari, 1996.
Y. Taur et al., 1995.

T.C. Holloway et al., 1997.
R.A. Chapman et al., 1997.
M. Rodder et al., 1996.
D. Liu et al., 1993.

Why Excessive leakage an Issue?

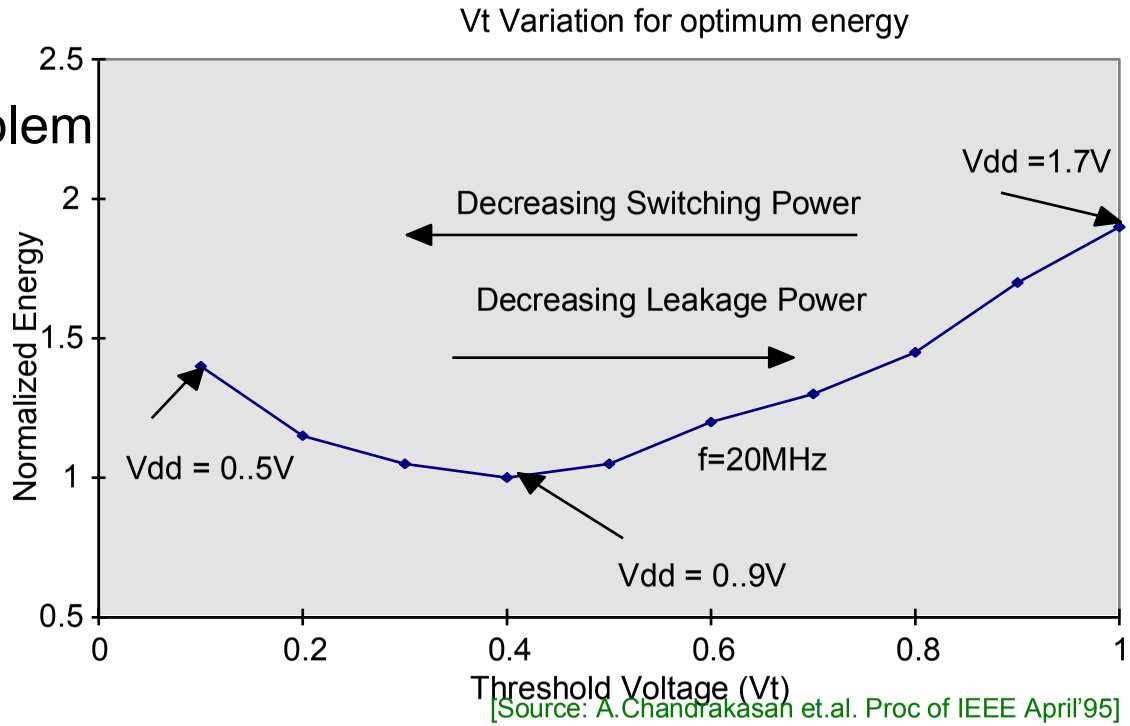
- Leakage component to active power becomes significant % of total powe
- Approaching ~10% in 0.18 μm technology
- Acceptable limit less than ~10%, implies serious challenge in V_T scaling!



Barrier ↓ high static leakage (standby) power

Power Trends

- Enable development of ultra low voltage circuits
- At lower Vt,
  - leakage becomes a problem
  - Signal integrity and Noise margin



[Source: A.Chandrakasan et.al. Proc of IEEE April'95]

- Multiple on-chip Vt, dynamic Vt
- Other challenges for low voltages ?

Trends in Microelectronics

- Improvement in device technology
  - Smaller circuits
  - Faster circuits
  - More circuits on a chip
- Higher Integration
  - More complex systems
  - Lower cost of computation
  - Higher reliability
- Limitations
  - Intrinsic device scaling limits
  - Cost of fabrication
  - Interconnect limitation
  - Large scale design management

Problems of Microelectronics

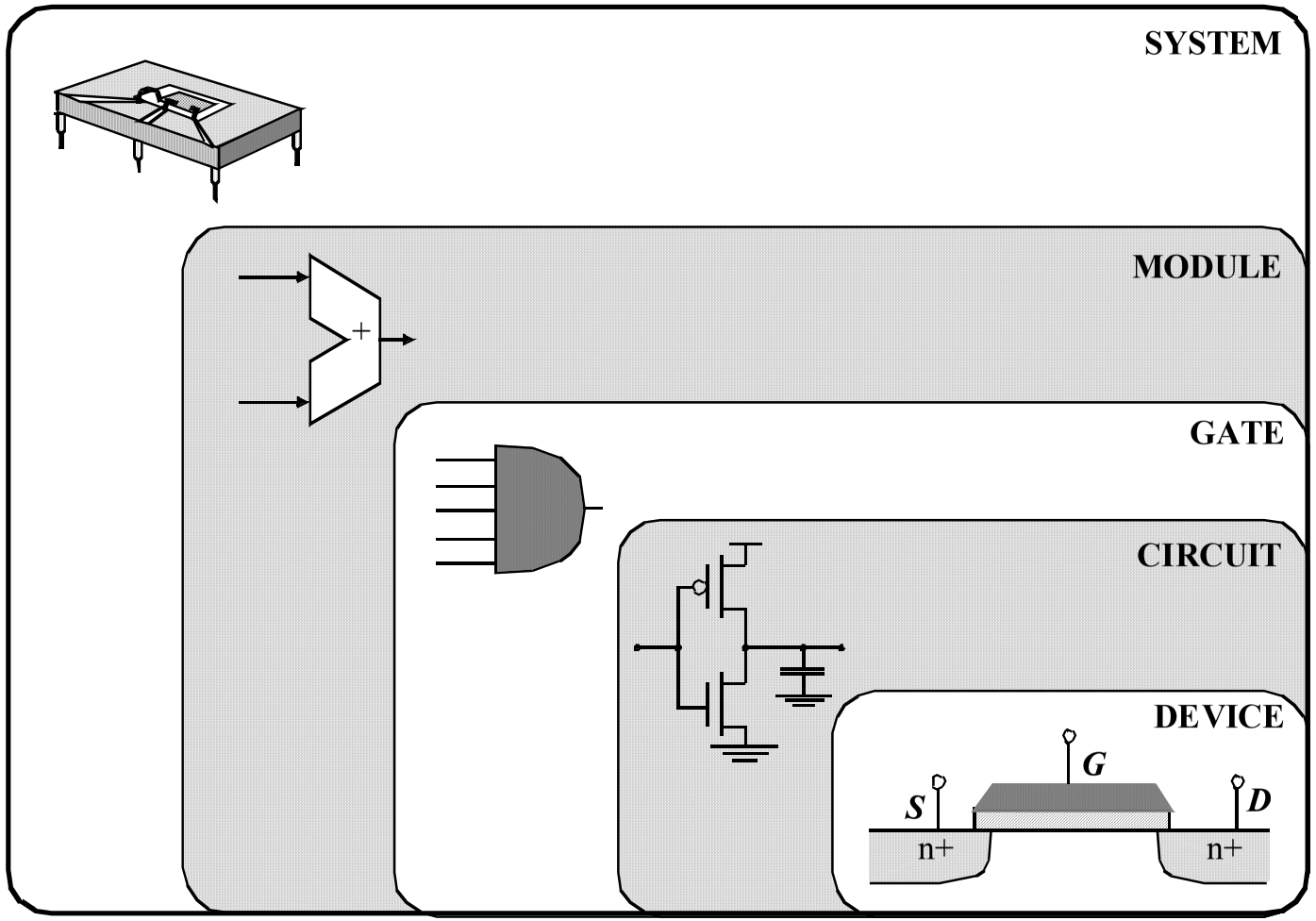
- Design Cost:
  - design time
  - fabrication time
  - impossibility to repair
  - reduce design cost to be competitive in price
- Marketing Issues:
  - use most recent technologies to stay competitive in performance
  - volume production is inexpensive
  - time-to-market is critical
  - evolving market
- Solution:
  - Hierarchical and abstraction
  - Different design styles
  - Computer-Aided-Design

Circuit and System Representations

Complex digital system ⟶ Component gates
+
Memory systems

- 3 design domains
  - Behavioral
    - specifies what a particular system does
  - Structural
    - how entities are connected together to effect the prescribed manner
  - Physical
    - how to actually build a structure that has the required connectivity to implement the prescribed behavior

Design Abstraction Levels



For a Digital Design

- Architecture
- Algorithm
- Module or Functional Block
- logical
- Switch
- Circuit
- Layout

Behavioral Representation Domain

- Hardware description language
  - VHDL, Verilog
- Boolean equation
- Within this domain, there are various level of abstraction
  - Algorithm
  - Register transfer level (communication between registers)

$$\text{Acc} \longleftarrow \text{Acc} + \text{R1}$$

  - Boolean equations

$$CO = A.B + A.C + B.C$$

$$\downarrow$$

carry

Behavioral Representation Domain - cont.

- Algorithm level (Verilog)

can include speed info

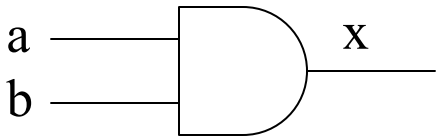
```
MODULE carry (co, a,b,c)
    output co
    input a, b, c
    assign co = (a&b)|(a&c)|(b&c);
ENDMODULE
```

Structural Domain

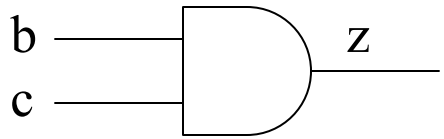
- The levels of abstraction include
  - module
  - gate
  - switch
  - circuit

```
MODULE    carry (co, a, b, c)
          input a, b, c;
          output co;
          wire x, y, z
               AND     g1 (x, a, b)
               AND     g2 (y, a, c)
               AND     g3 (z, b, c)
               OR      g4 (co, x, y, z);
ENDMODULE
```

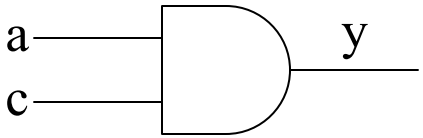
Structural Domain- cont.



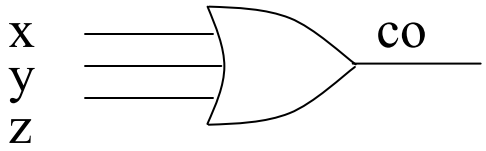
g1



g3



g2



g4

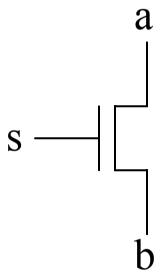
Physical Representation

```
MODULE    carry ;
          Input    a, b, c;
          output  co;
          boundary [0, 0, 100, 400]
                port a aluminum width = 1 origin = [0,2]
                port b aluminum width = 1 origin = [0,7]
                port
                .
                .
                .
                Port ci polysilicon …….
ENDMODULE
```

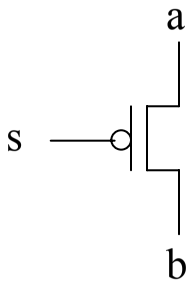
Transistor Level

```
MODULE   carry (co, a, b, c)
         input    a, b, c;
         output   co;
         wire     i1, i2, i3, i4, cn;
                  NMOS   n1(i1, vss, a)
                  NMOS   n2(i1, vss, b)
                           .
                           .
                           .
                  PMOS   p1(i3, vdd, b);
                  PMOS   p2(cn, i3, a);
                           .
                           .
                           .
ENDMODULE
```

CMOS Logic

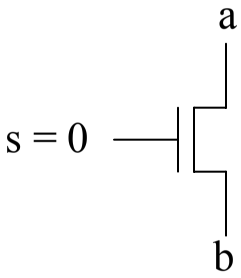


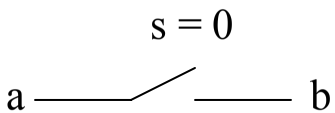
NMOS transistor

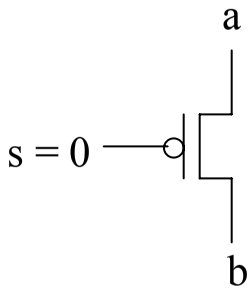


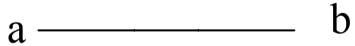
PMOS transistor

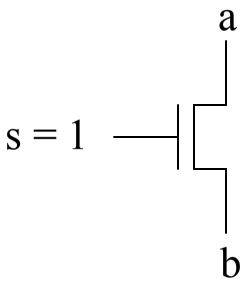
Consider them as switches

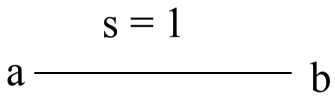


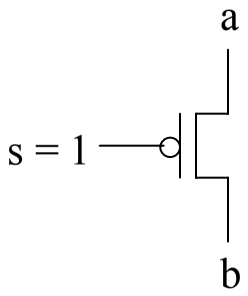


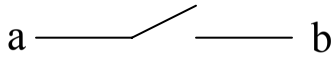




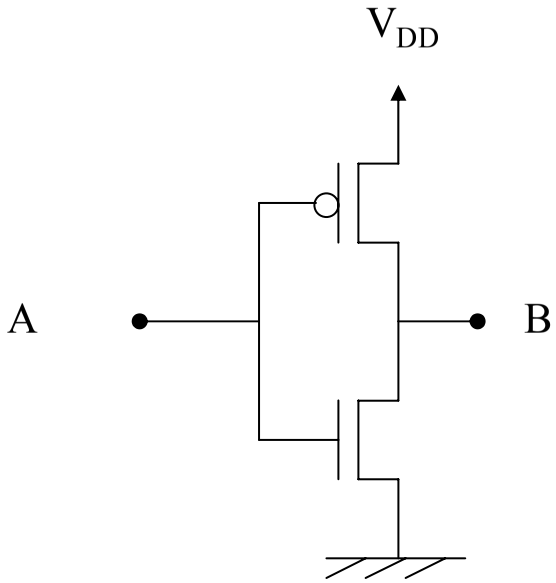






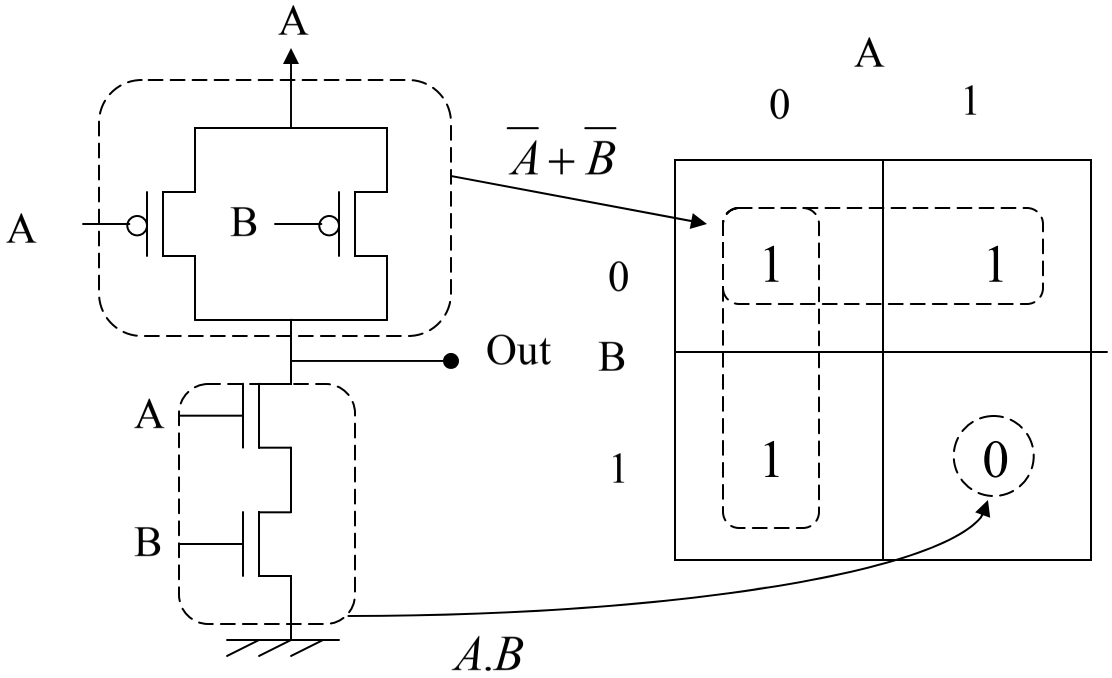


Inverter ($\overline{A}$)

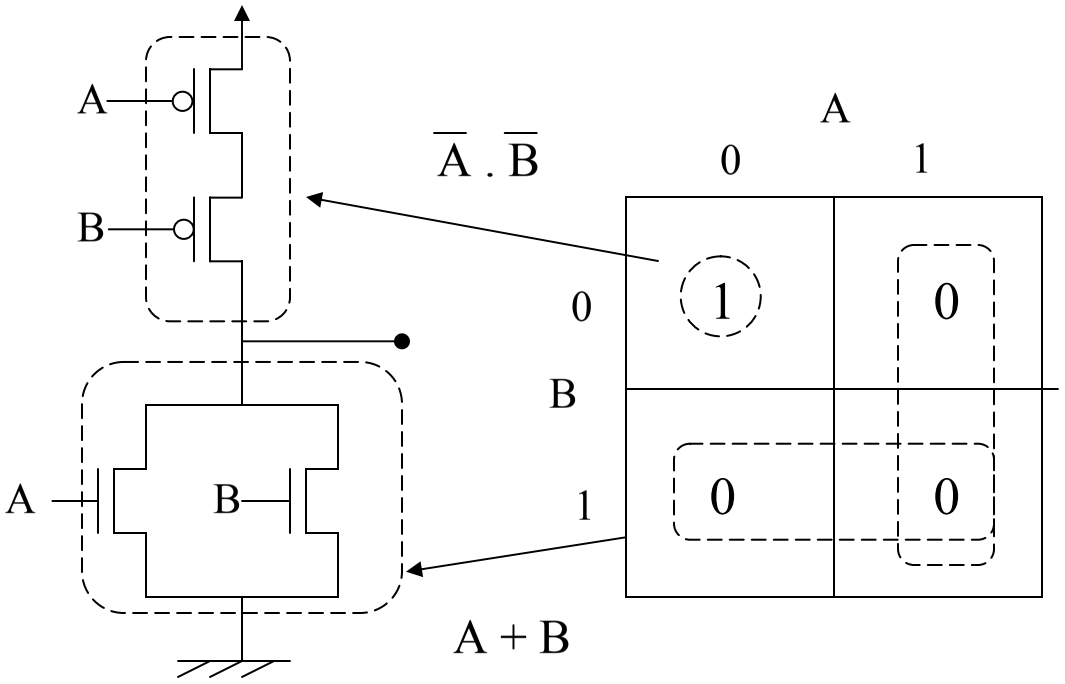


- Low power dissipation

NAND ($\overline{AB}$)



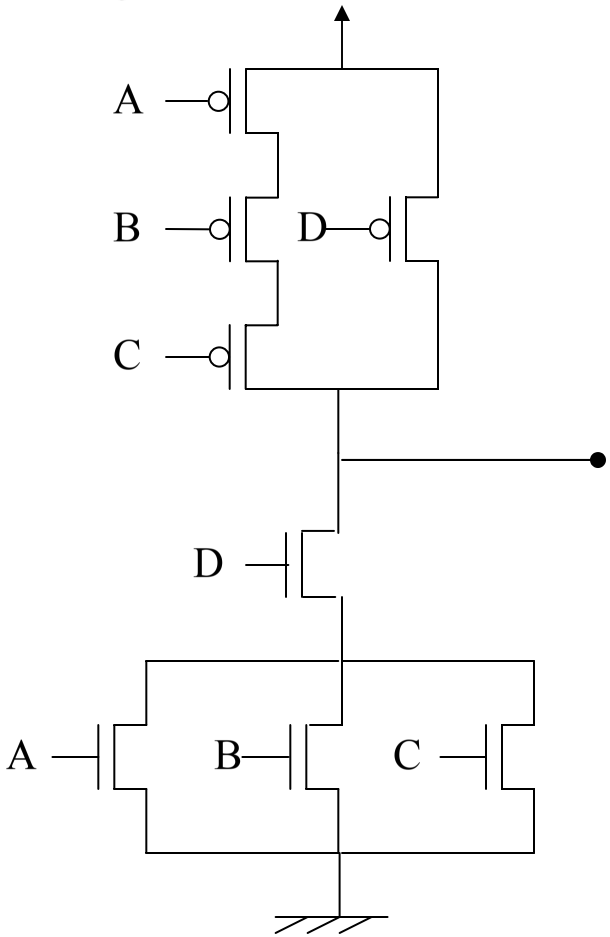
NOR ($\overline{A+B}$)



Complex Gates

$$F = \overline{((A+B+C).D)} = \overline{D} + \overline{A}\overline{B}\overline{C}$$

$$\overline{F} = (A+B+C).D$$



VLSI Design is Inter-Disciplinary

- Breadth of field
  - Semiconductor physics and technology
  - Integrated electronics
  - Systems design
  - Testing
  - Computer-Aided Design
- Depth of field
  - Complexity of fabrication technology
  - Difficulty of design problems