Term Project

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 15-Oct-2009 Due: 10-Dec-2009

Voltage Overscaling by Unbalanced Pipelining

Case Study: 8-bit Wallace Tree Multiplier

GOAL

The goal is to design an 8-bit Wallace Tree Multiplier with a *scaled-down supply voltage* that exploits *unbalanced* pipelining. You should try to optimize your design and deliver optimization results for 1) *performance* 2) *power* and 3) *area*.

Design Requirements

1) At the input, output, and intermediate stages, flip-flops are to be considered for both in schematic and layout. The overhead of these flip-flops should be taken into account while estimating performance, power, and area. You may think of considering low overhead flip-flops.
2) Clock skew does not need to be considered.
3) Include parasitic capacitances when extracting layout.
4) Do post-layout simulation to confirm the functionality of your design.

PIN Naming and Electrical Characteristics

1) *Inputs*: A_7 to A_0, B_7 to B_0
2) *Outputs*: S_15 to S_0
3) *Clock*: clk
4) *Supply & Ground*: vdd!, gnd!
5) *Rise and Fall time* of the input signals (including clock): 0.1 ns, *Delay time*: 1ns
6) *Max supply voltage*: 2.5 V