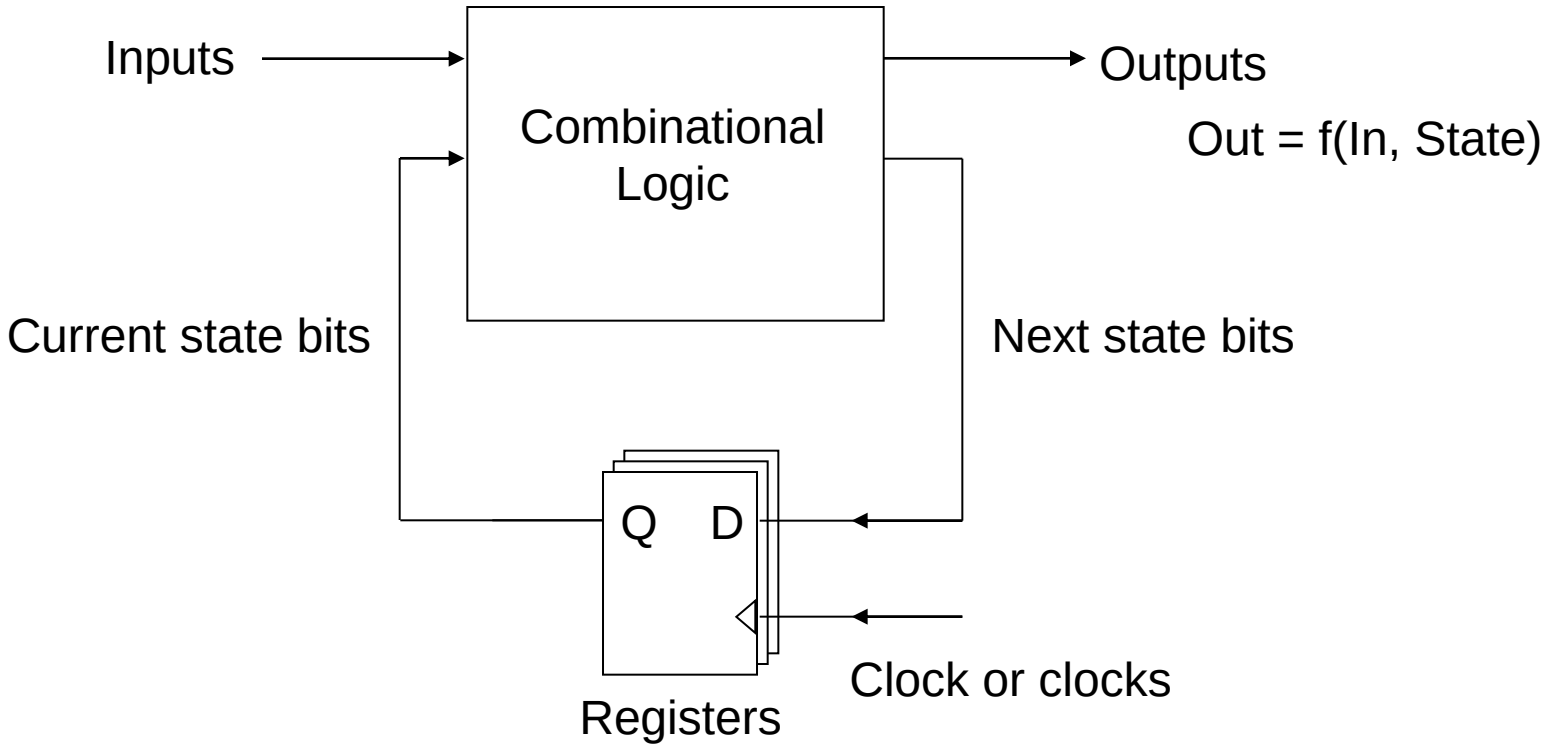
Sequential Logic

References:

Adapted from: *Digital Integrated Circuits: A Design Perspective*, J. Rabaey, Prentice Hall © UCB

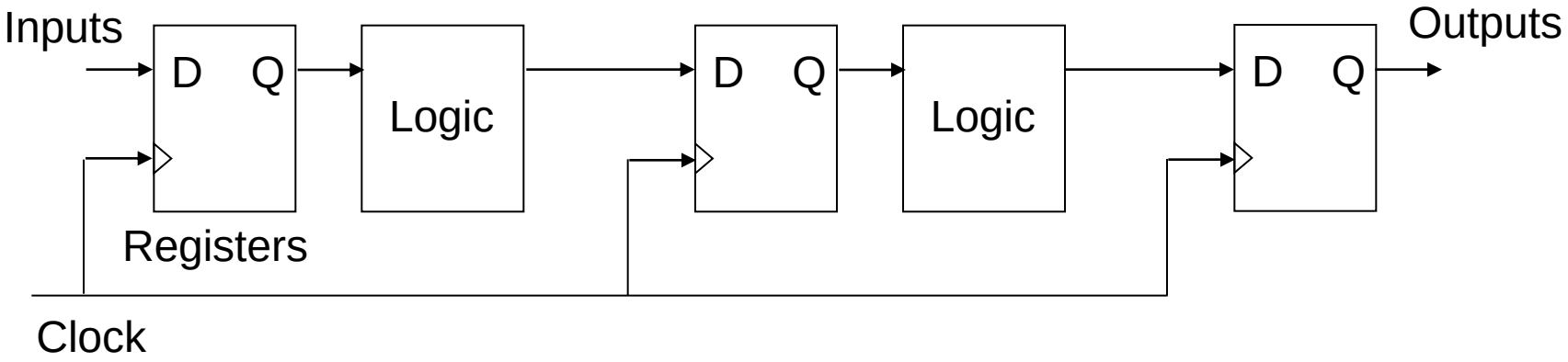
Principles of CMOS VLSI Design: A Systems Perspective, N. H. E. Weste, K. Eshraghian, Addison Wesley

Clocked Systems: Finite State Machines



Registers serve as storage element to store past history

Clocked Systems: Pipelined Systems

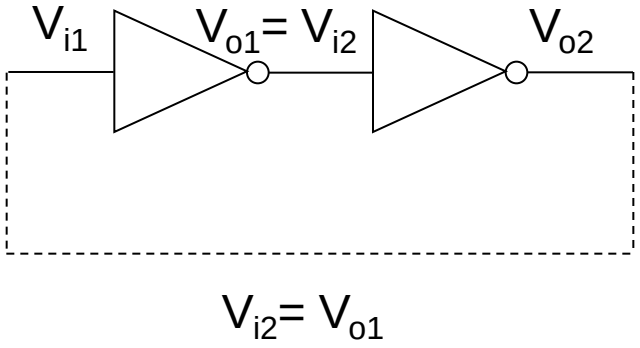


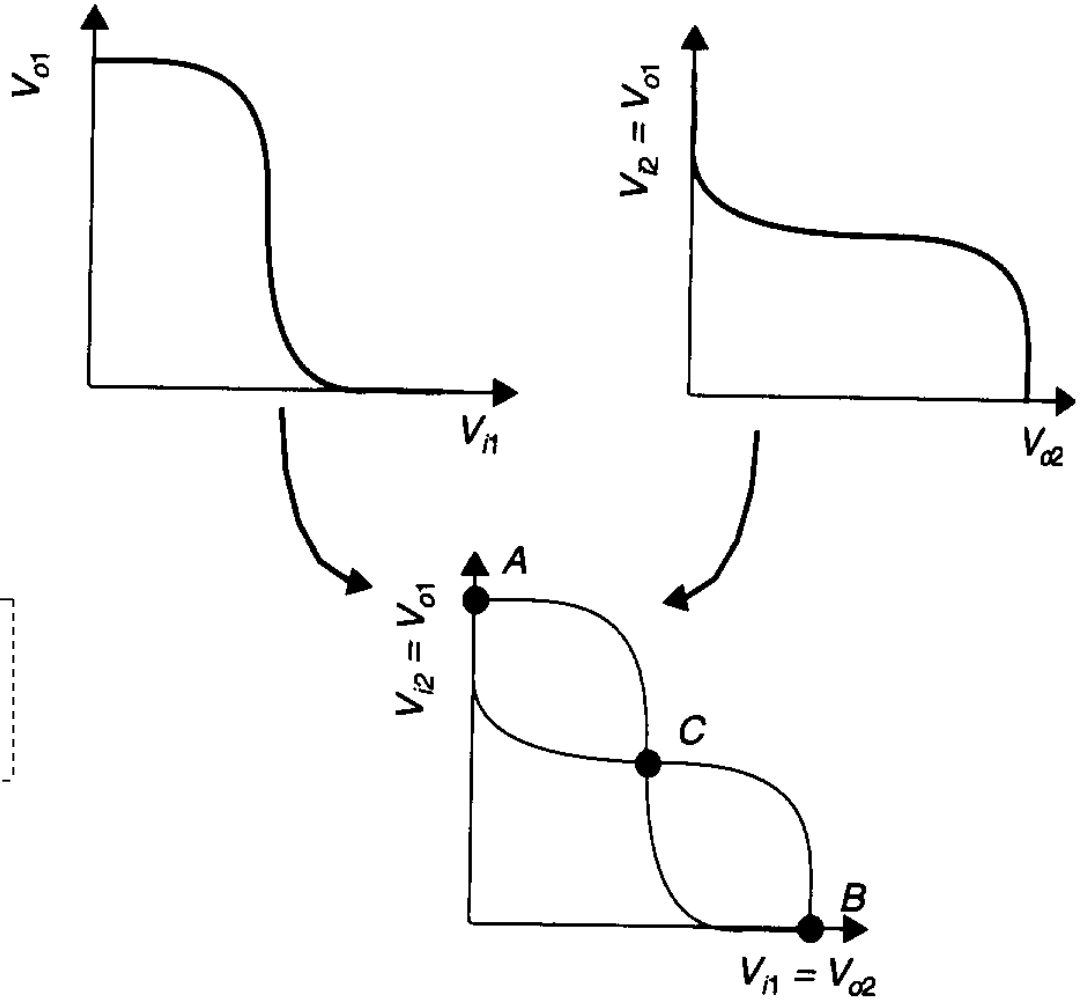
Registers serve as storage element to capture the output of each processing stage

Storage Mechanisms

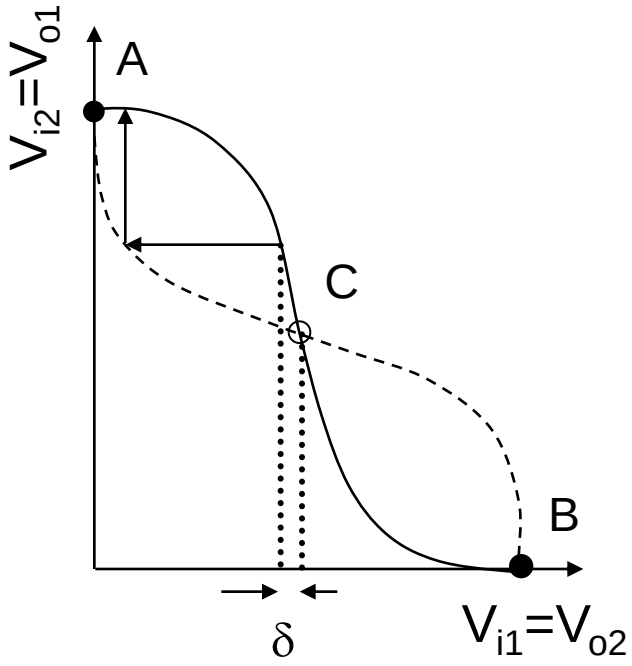
- Positive feedback
  - Connect one or more output signals back to the input
  - Regenerative, signal can be held indefinitely, static
- Charge-based
  - Use charge storage to store signal value
  - Need refreshing to overcome charge leakage, dynamic

Positive Feedback: Two Cascaded Inverters

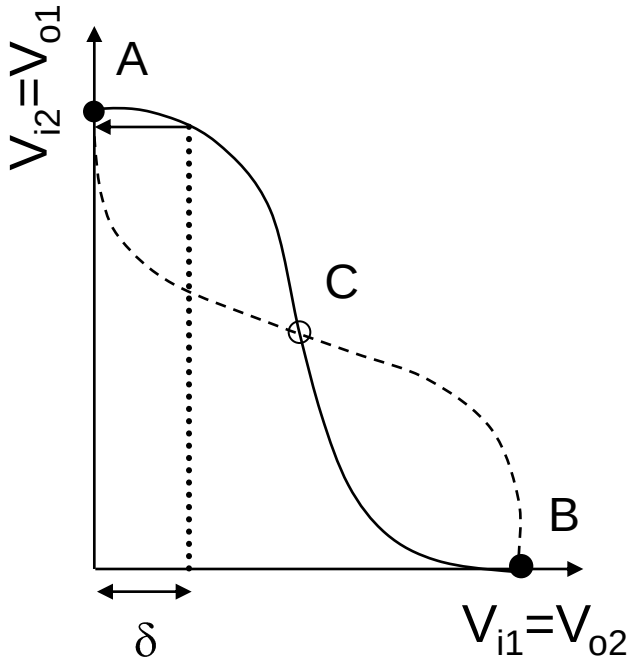




Bi-Stability and Meta-Stability



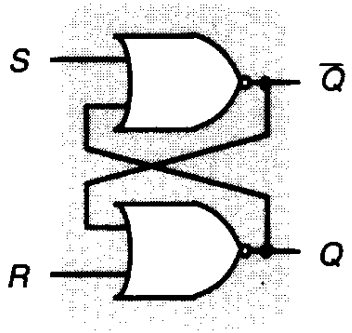
Gain larger than 1 amplifies the deviation from C



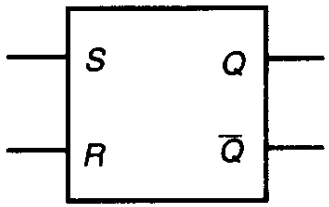
Gain less than 1 reduces the deviation from A

SR-Flip Flop

- NOR-based SR flip-flop, positive logic



Schematic

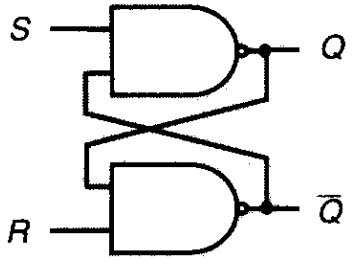


Logic Symbol

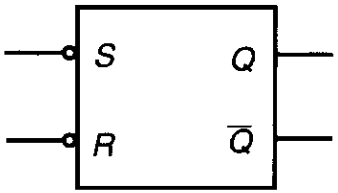
S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

Characteristic table

- NAND-based SR flip-flop, negative logic



Schematic



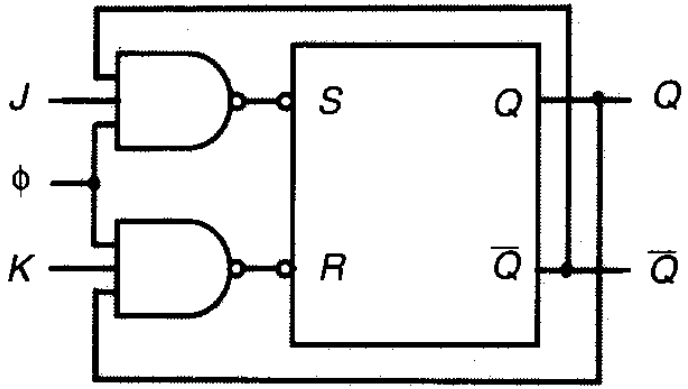
Logic Symbol

S	R	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	1	1

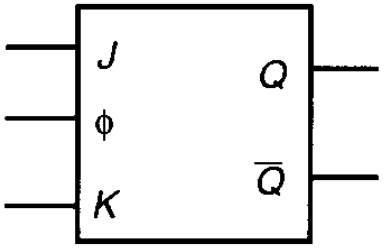
Characteristic table

Forbidden state

JK- Flip Flop



Schematic



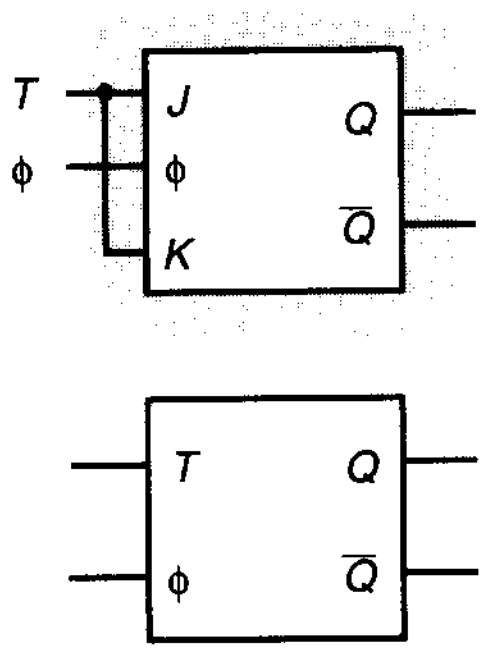
Logic Symbol

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

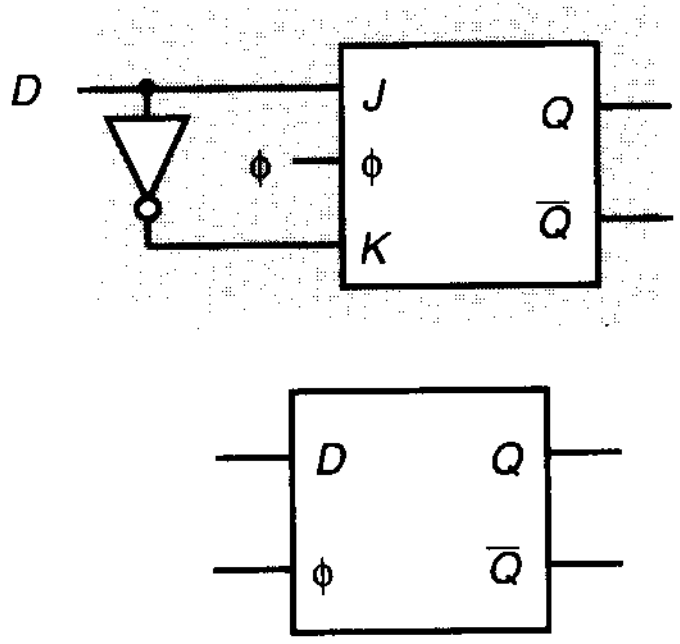
Characteristic table

- Clock input ϕ to synchronize changes in the output logic states of flip-flops
- Forbidden state is eliminated,
- But repeated toggling when J = K = 1, need to keep clock pulse small < propagation delay of FF

Other Flip-Flops



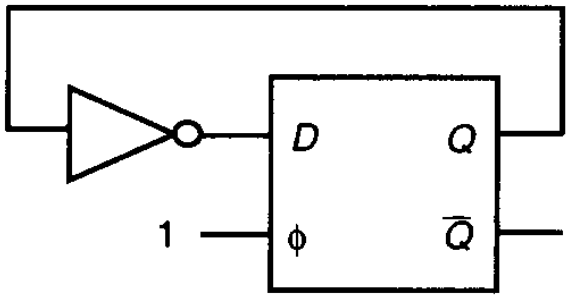
Toggle or T flip-flop

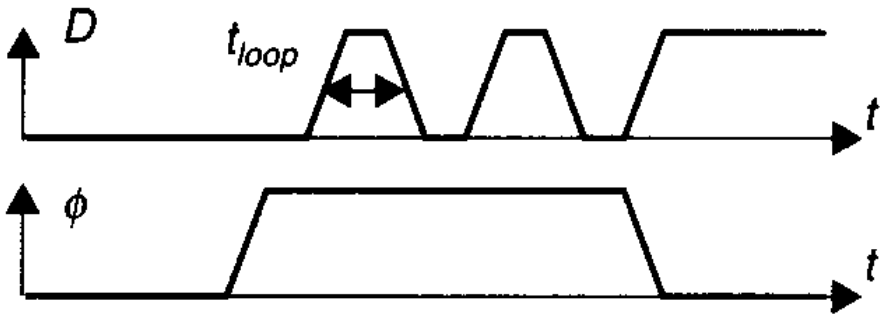


Delay or D flip-flop

Race Problem

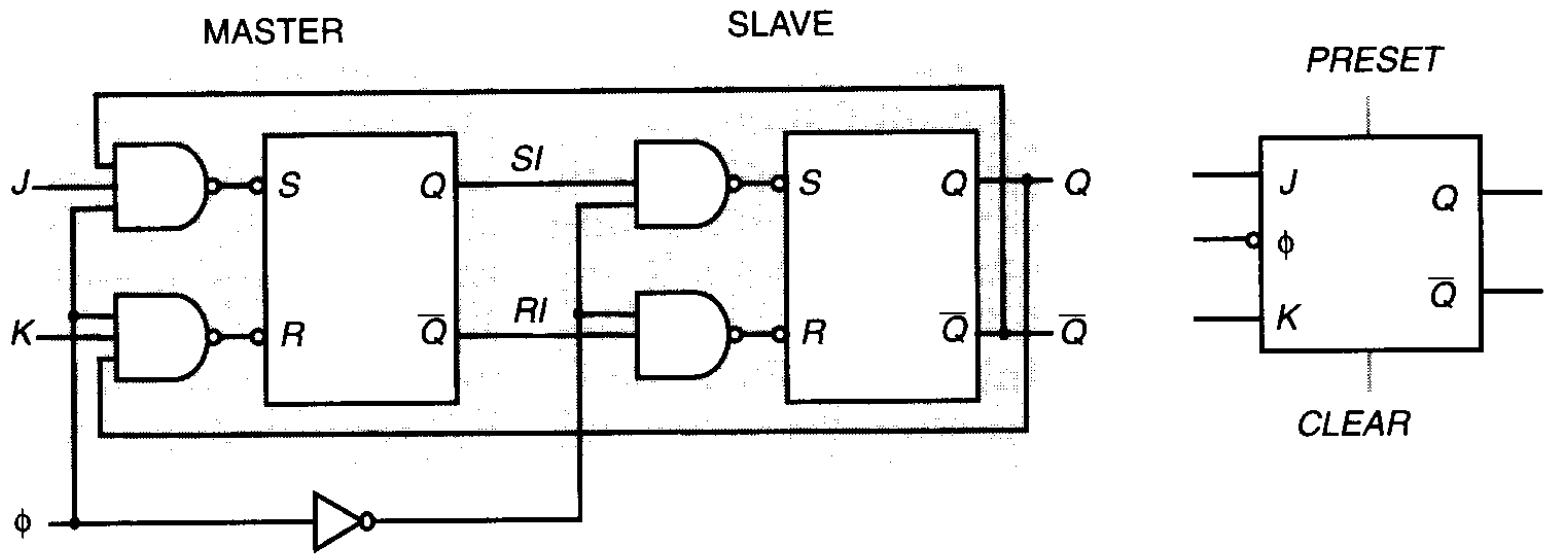
- A flip-flop is a latch if the gate is transparent while the clock is high (low)





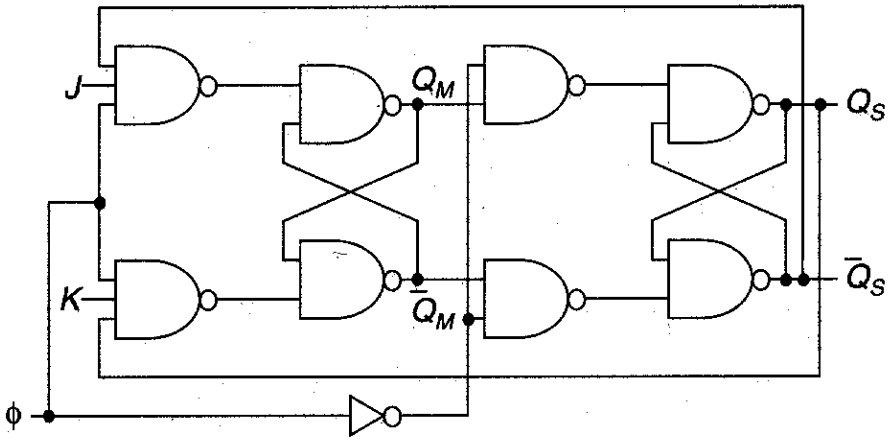
- Signal can raise around when ϕ is high
- Solutions:
  - Reduce the pulse width of ϕ
  - Master-slave and edge-triggered FFs

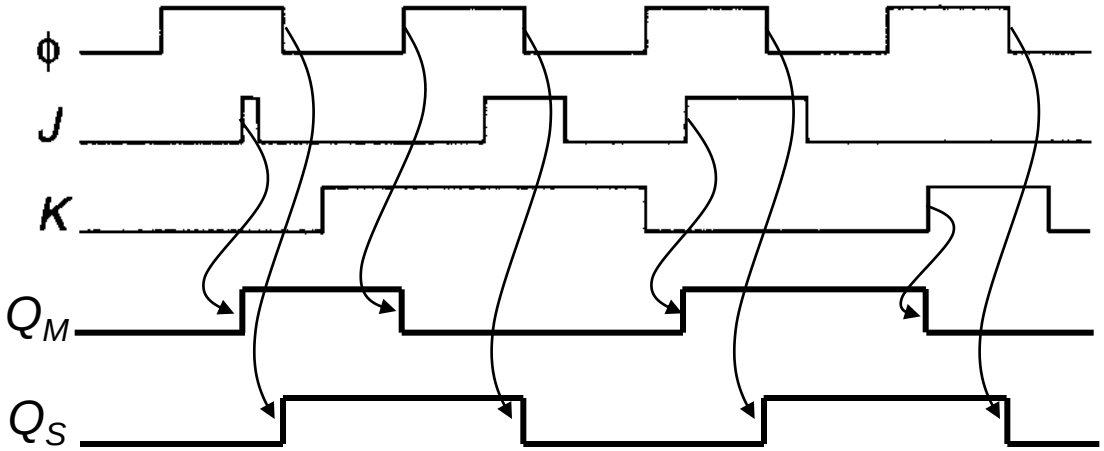
Master-Slave Flip-Flop



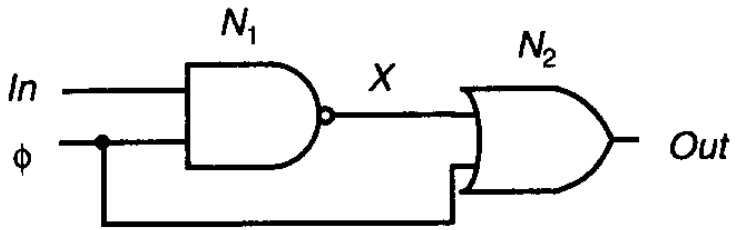
- Either master or slave FF is in the hold mode
- Pulse lengths of clock must be longer than propagation delay of latches
- Asynchronous or synchronous inputs to initialize the flip-flop states

One-Catching or Level-Sensitive

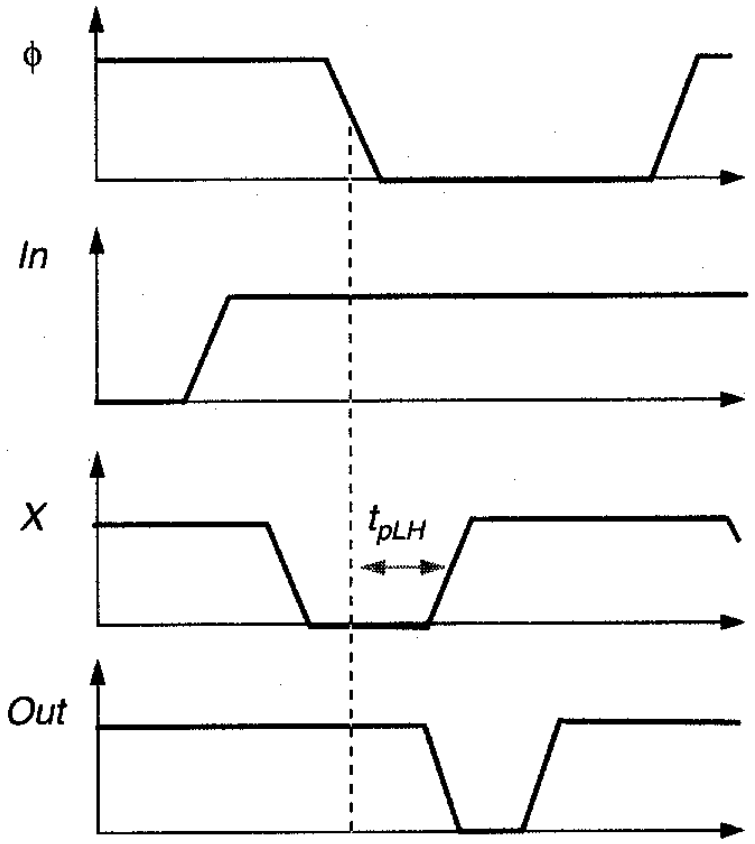




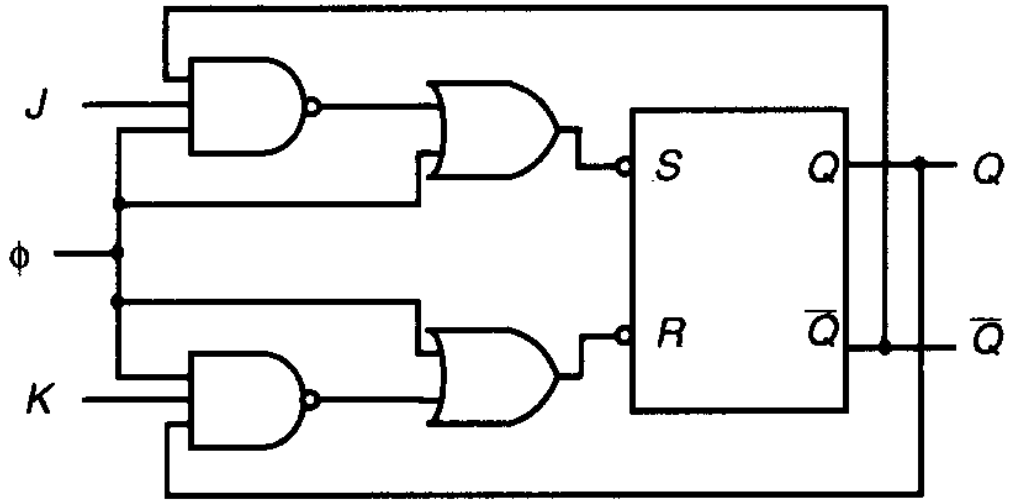
Propagation Delay Based Edge-Triggered

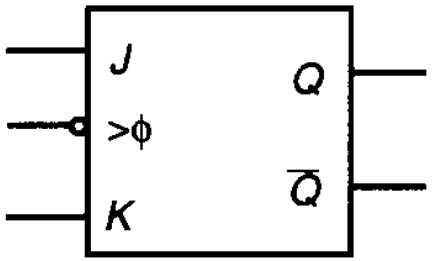


- Depend only on the value of *In* just before the clock transition

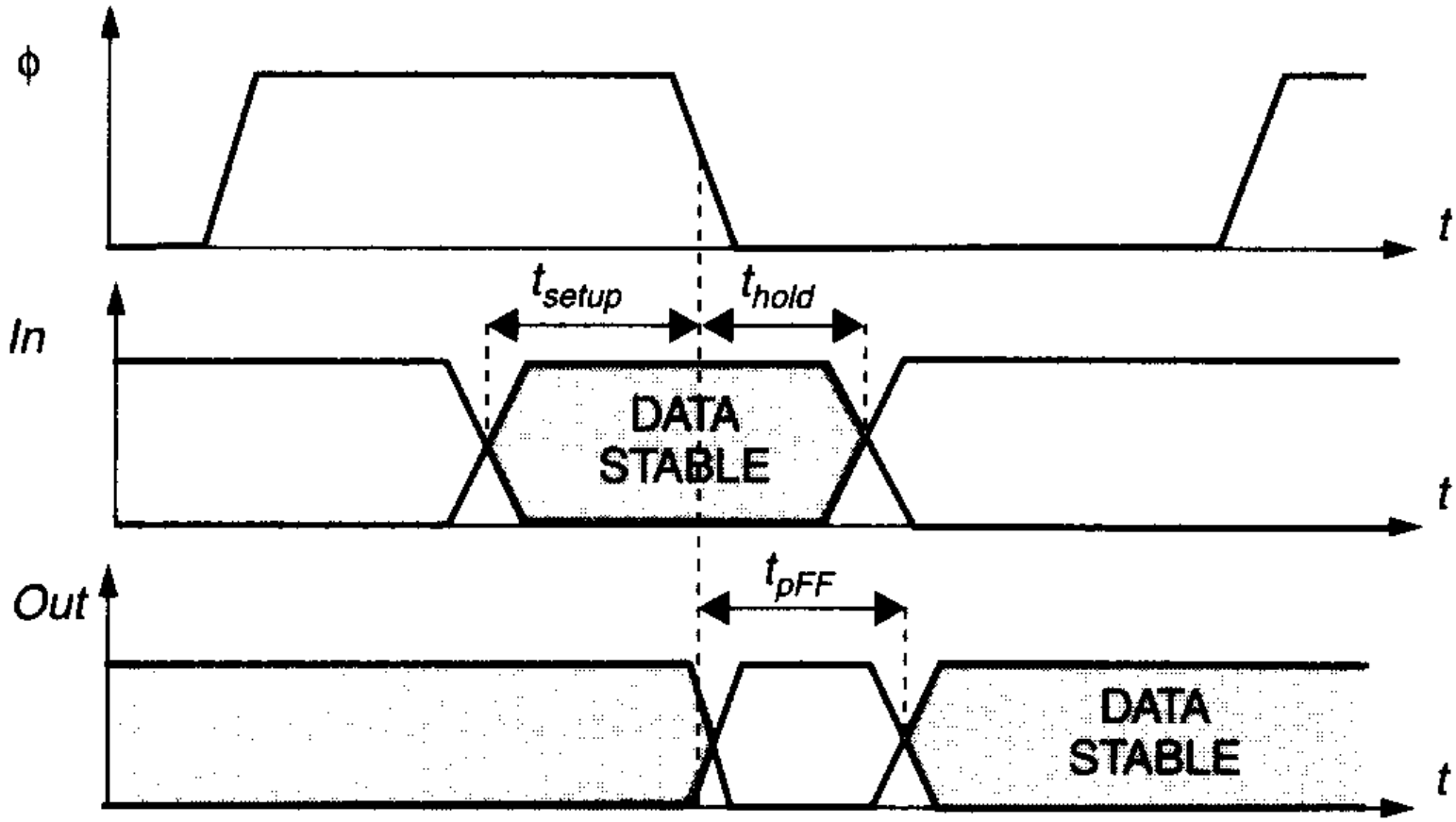


Edge Triggered Flip-Flop

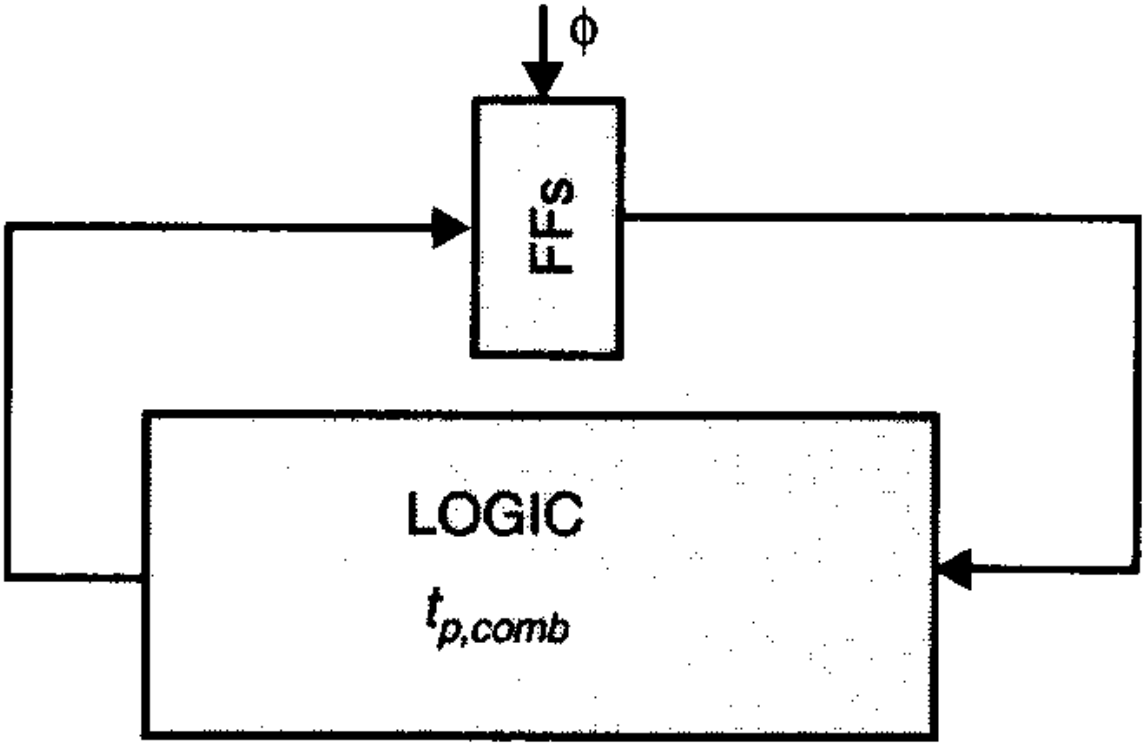




Flip-Flop: Timing Definitions



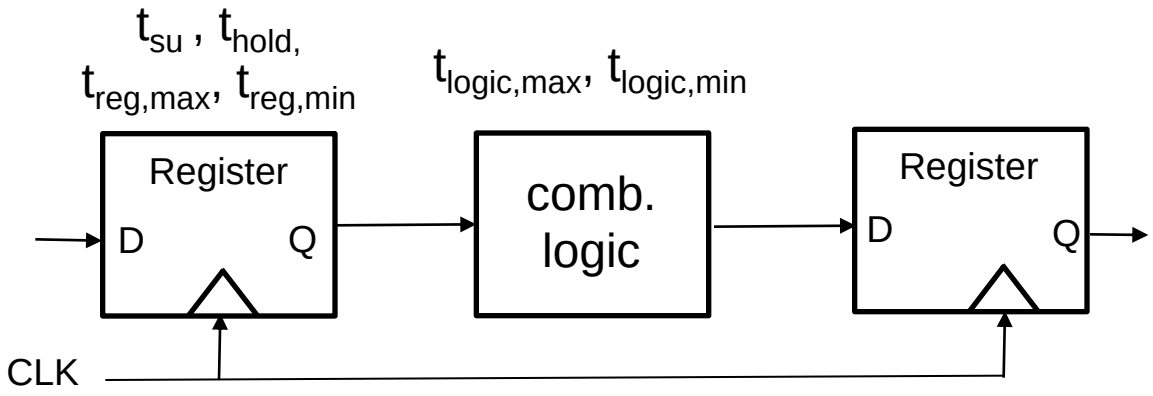
Maximum Clock Frequency



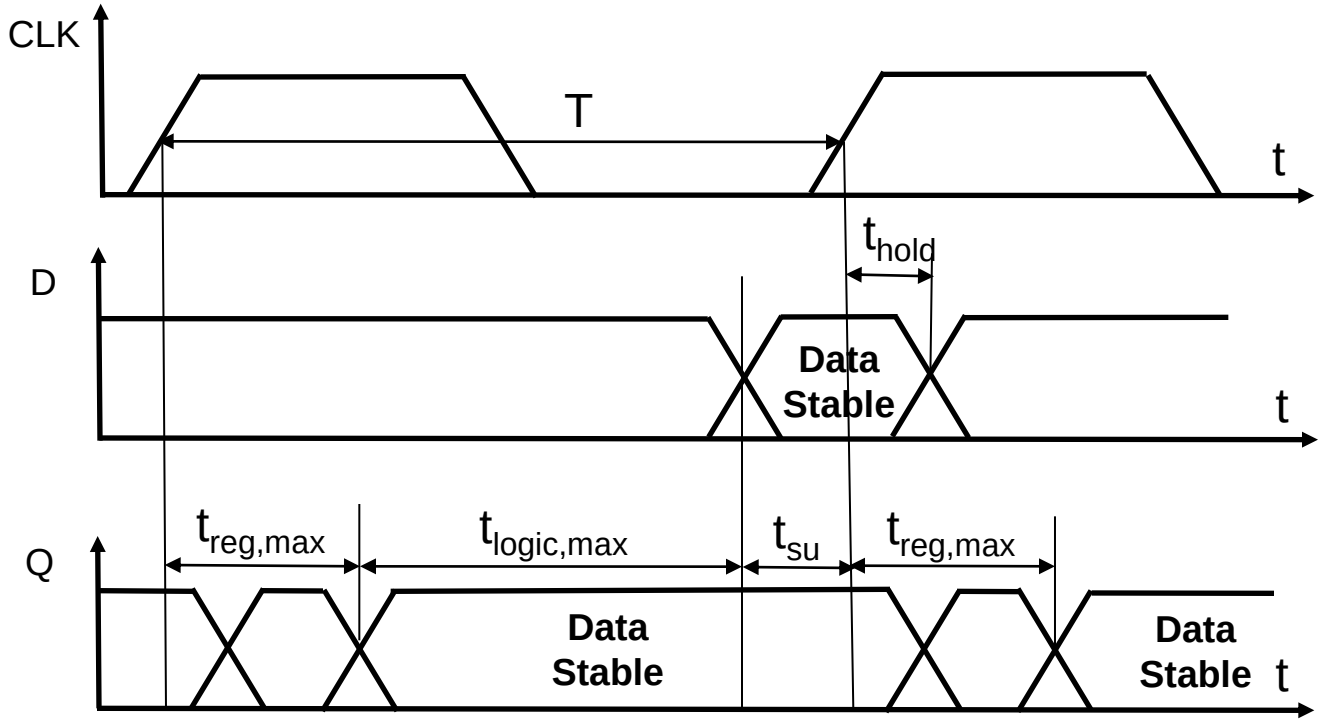
$$t_{pFF} + t_{p,comb} + t_{setup} < T$$

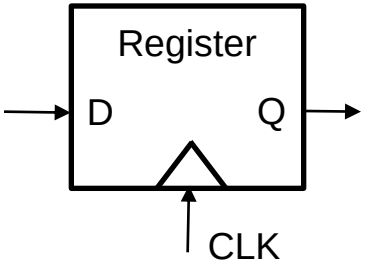
Timing Metrics in Sequential Circuits

- Setup Time (t_{su}) is the time that the data inputs must be valid **before** the clock transition
- Hold Time (t_{hold}) is the time that the data inputs must be valid **after** the clock transition
- Propagation delays ($t_{reg,max}$, $t_{reg,min}$) – D input is copied to Q



Setup Time, Hold Time, and Propagation Delay



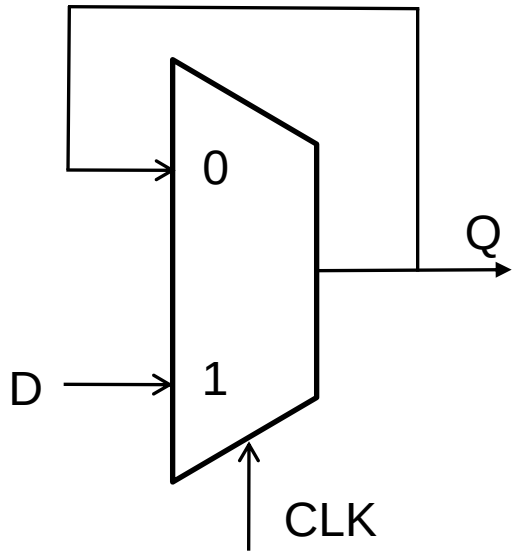


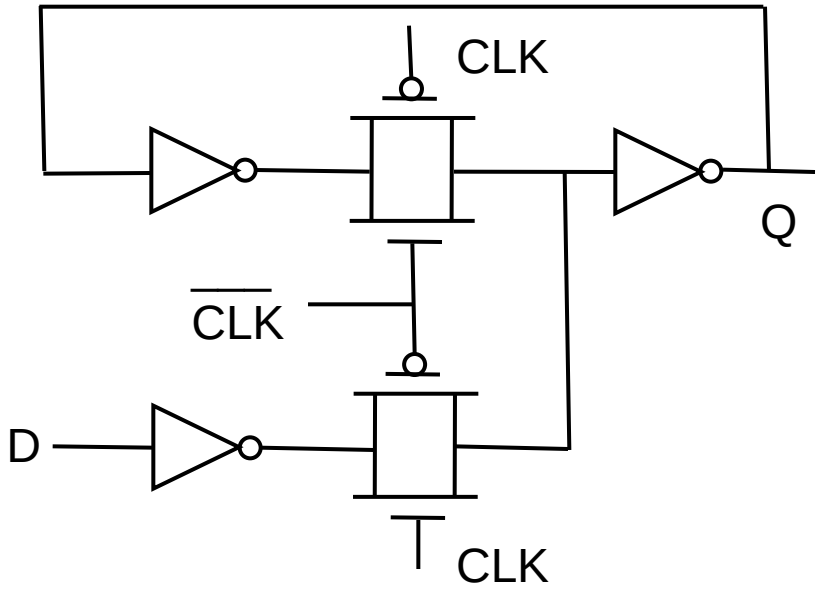
$$t_{reg,\max} + t_{\log ic,\max} + t_{setup} \leq T$$

$$t_{\log ic,\min} + t_{reg,\min} \geq t_{hold}$$

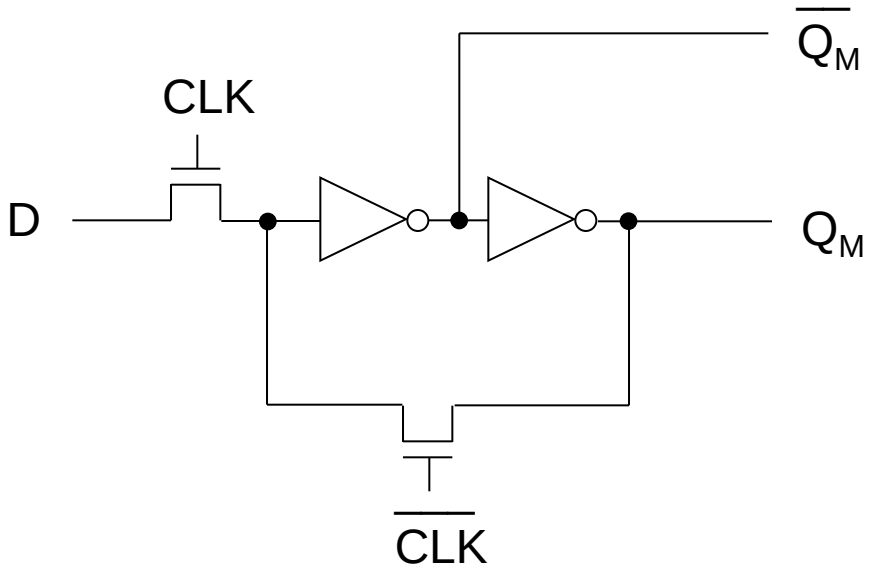
Multiplexer Based Latches

- A latch is a **level-sensitive** device





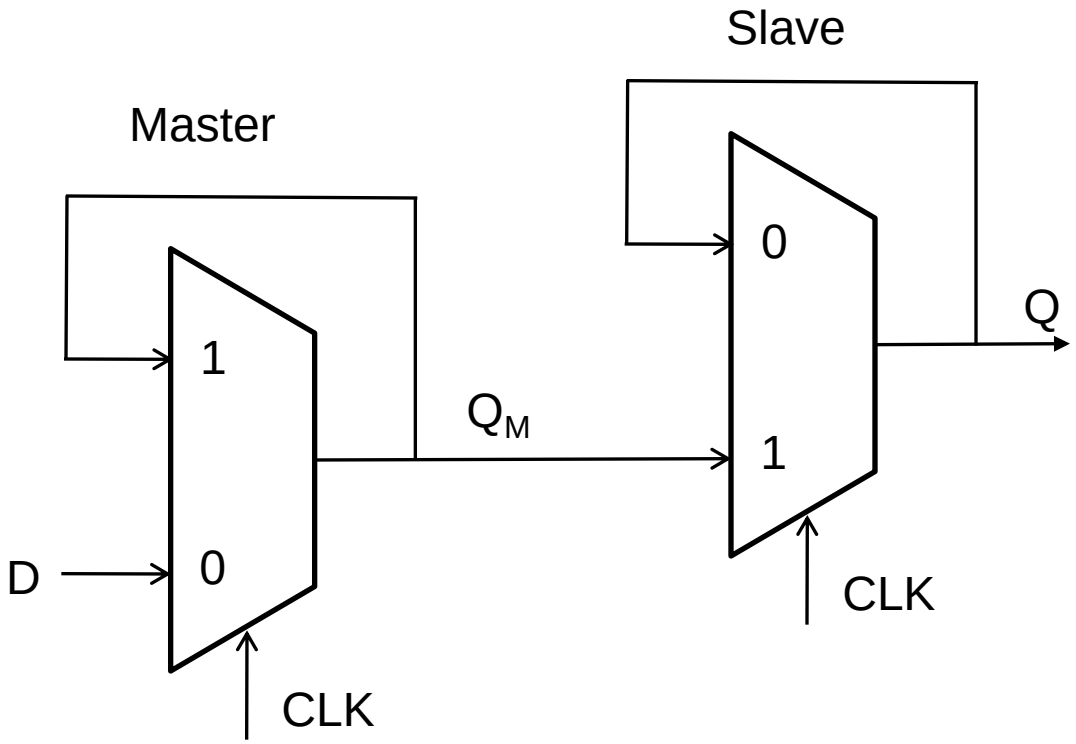
NMOS-only MUX based Latch



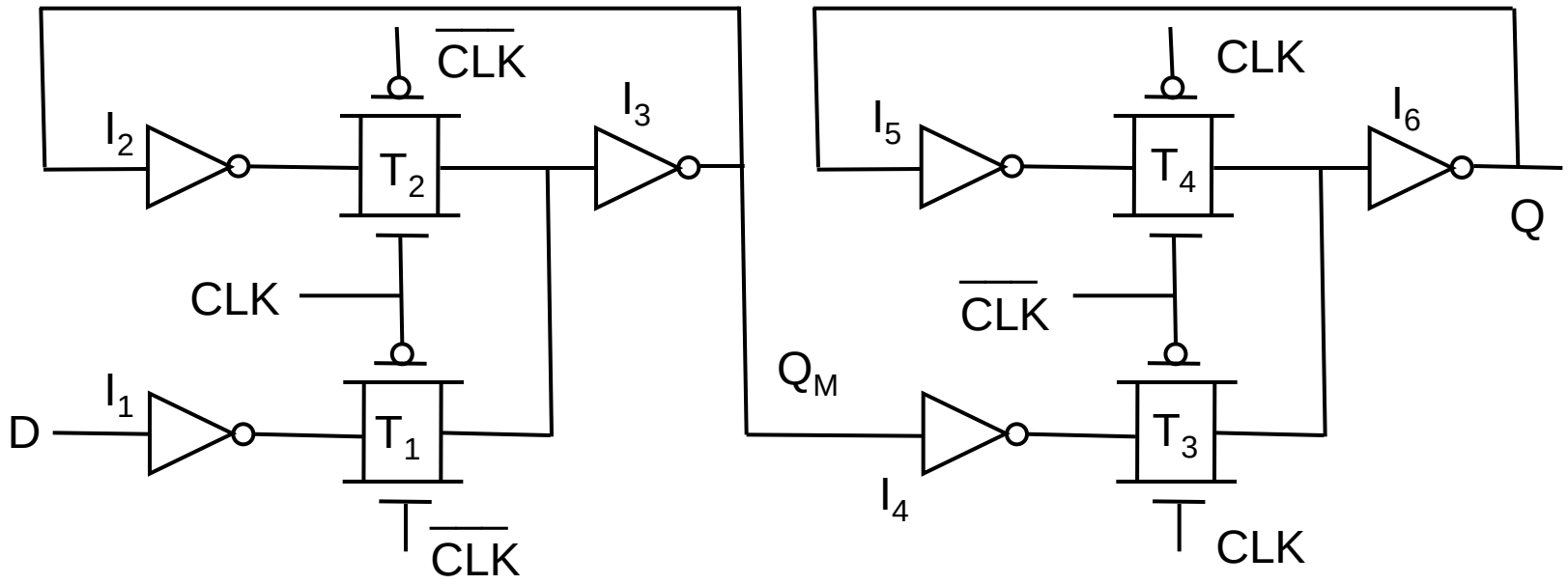
- Load of only 2 transistors to clock signals
- Passes a degraded high voltage of $V_{DD} - V_{Tn}$

Master Slave Edge-Triggered Register

- A register is an **edge-triggered** storage element
- A Flip-Flop is any **bistable** component formed by the **cross-coupling** of gates

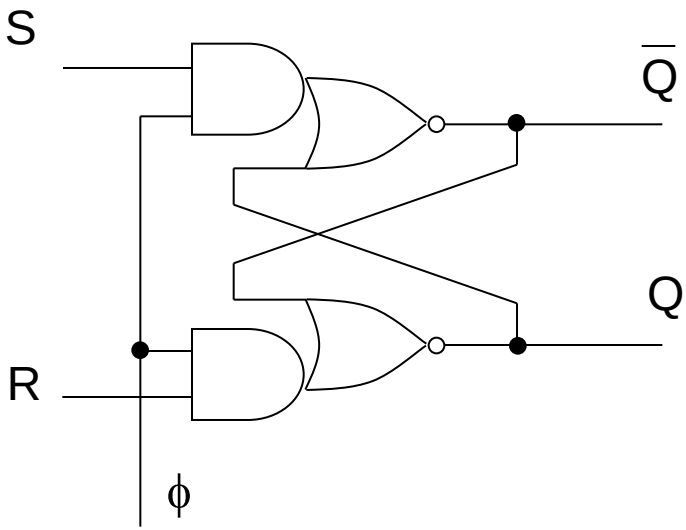


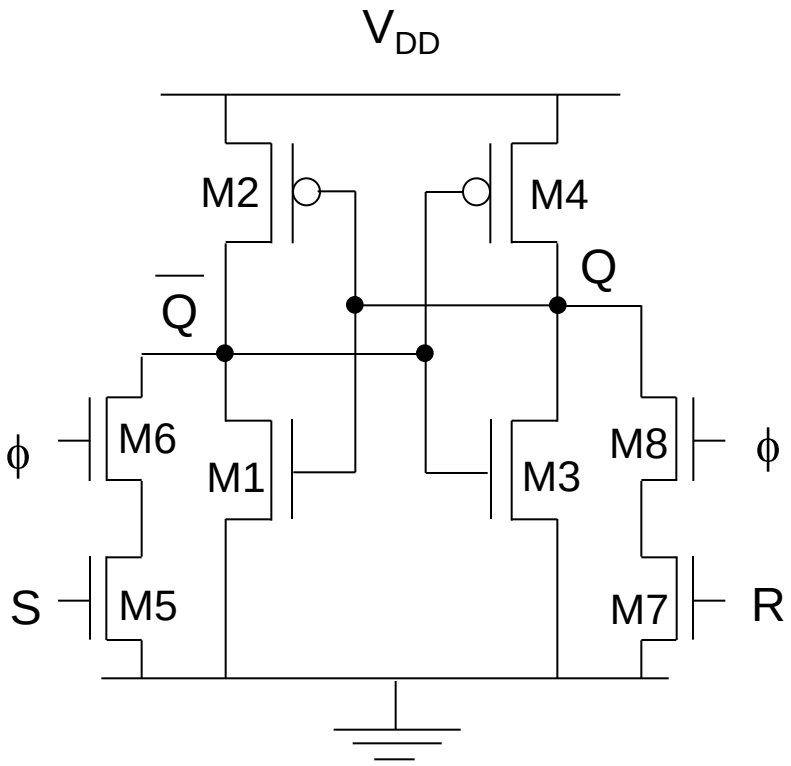
Master Slave Edge-Triggered Register



- Setup Time: $3*t_{inv} + t_{tx}$ $(I_1 \rightarrow T_1 \rightarrow I_3 \rightarrow I_2)$
- Propagation Delay: $t_{tx} + t_{inv}$ $(T_3 \rightarrow I_6)$
- Hold Time: 0

CMOS Clocked SR Flip-Flop





Transistor Sizing of SR Flip-Flop

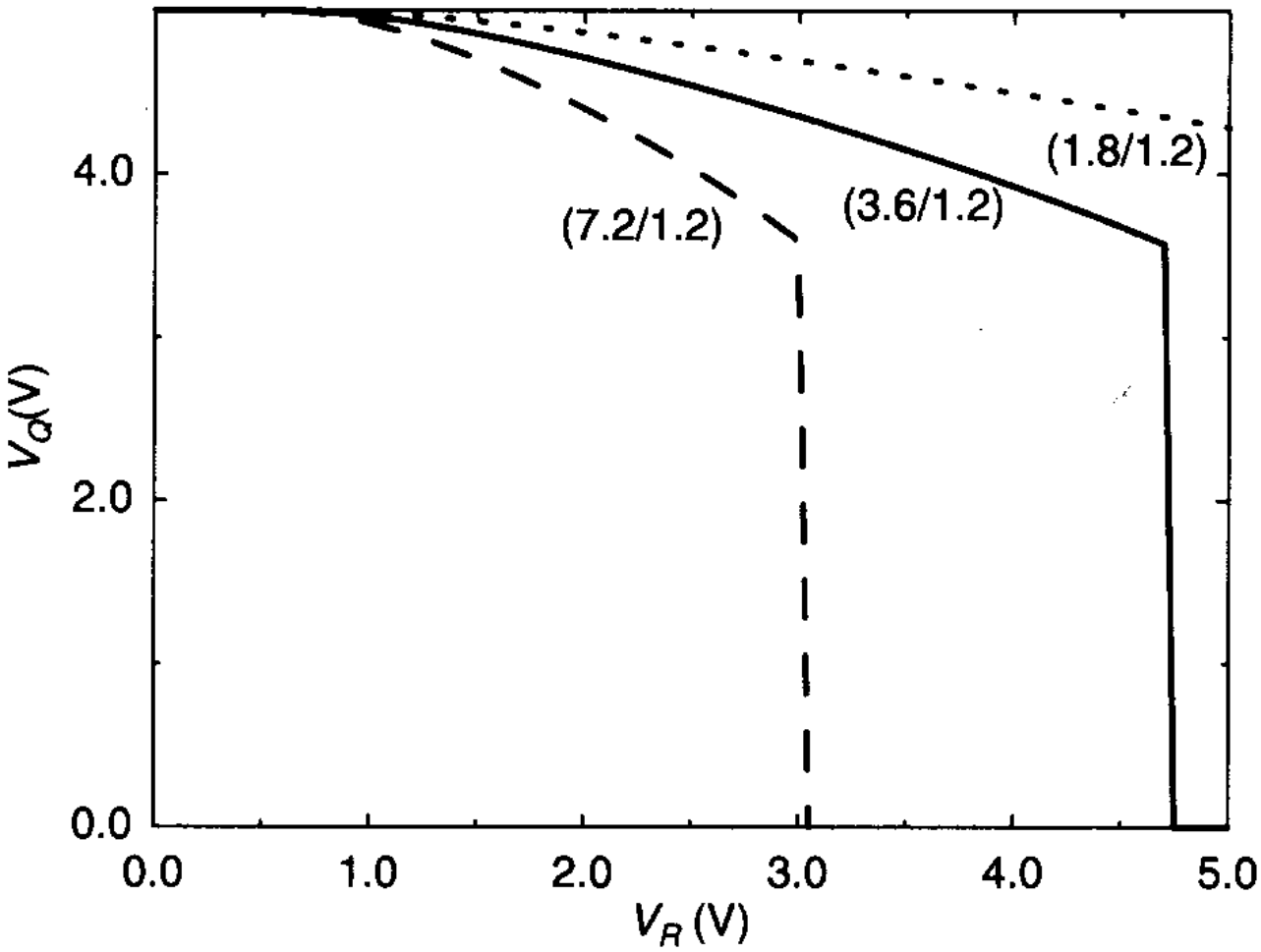
- Assume transistors of inverters are sized so that V_M is $V_{DD}/2$, mobility ratio $\mu_n/\mu_p = 3$
  - $(W/L)_{M1} = (W/L)_{M3} = 1.8/1.2$
  - $(W/L)_{M2} = (W/L)_{M4} = 5.4/1.2$
- To bring Q from 1 to 0, need to properly ratio the sizes of pseudo-NMOS inverter (M7-M8)-M4
  - V_{OL} must be lower than $V_{DD}/2$

$$k_{n,M78}\left((V_{DD}-V_{tn})\frac{V_{DD}}{2}-\frac{V_{DD}^2}{8}\right)=k_{p,M4}\left((V_{DD}-|V_{tp}|)\frac{V_{DD}}{2}-\frac{V_{DD}^2}{8}\right)$$

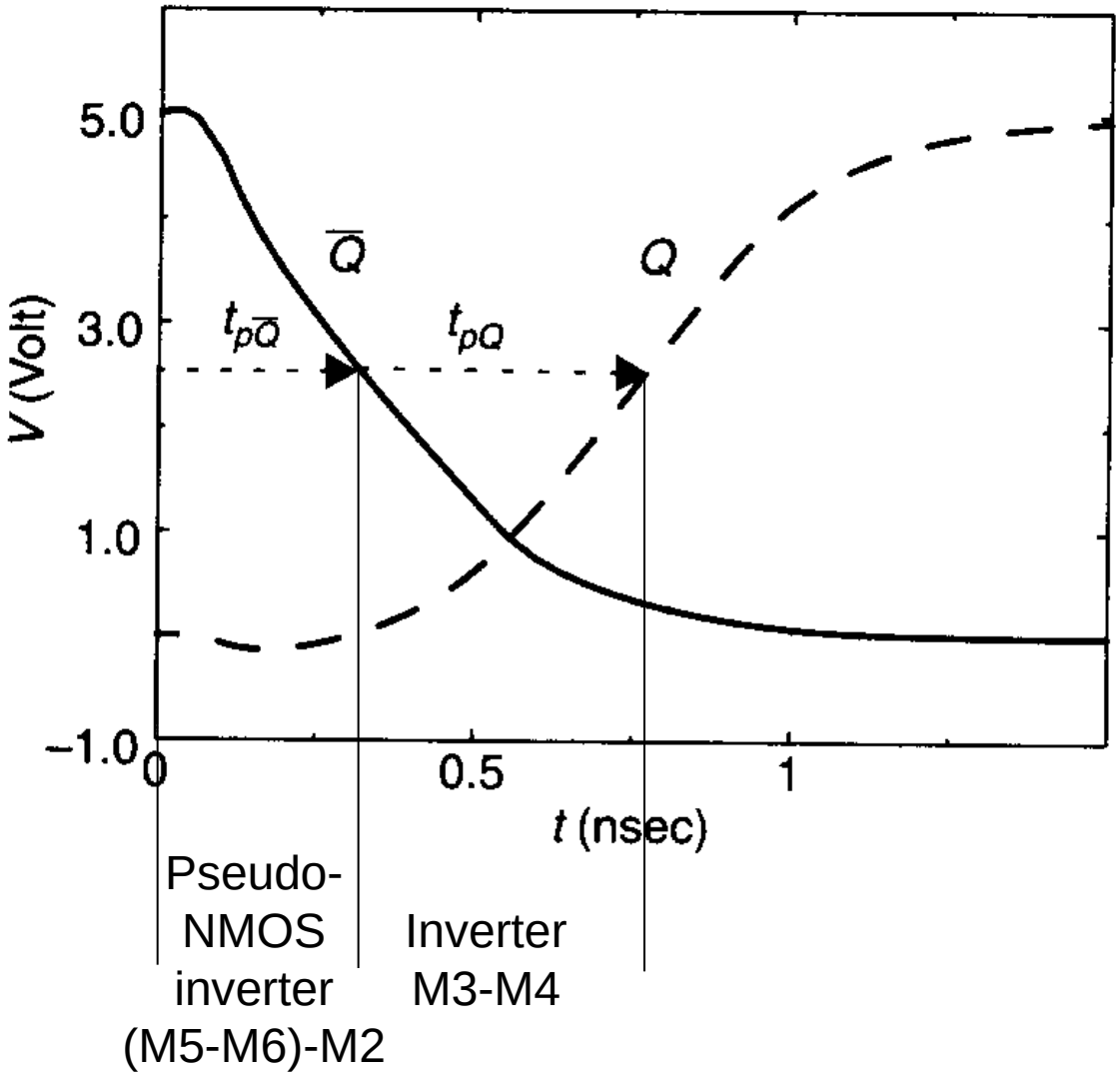
$$(W/L)_{M78} \geq \frac{\mu_p}{\mu_n}(W/L)_{M4} = (W/L)_{M3}$$

$$(W/L)_{M7} = 2(W/L)_{M78} \geq 2(W/L)_{M3} = (3.6/1.2)$$

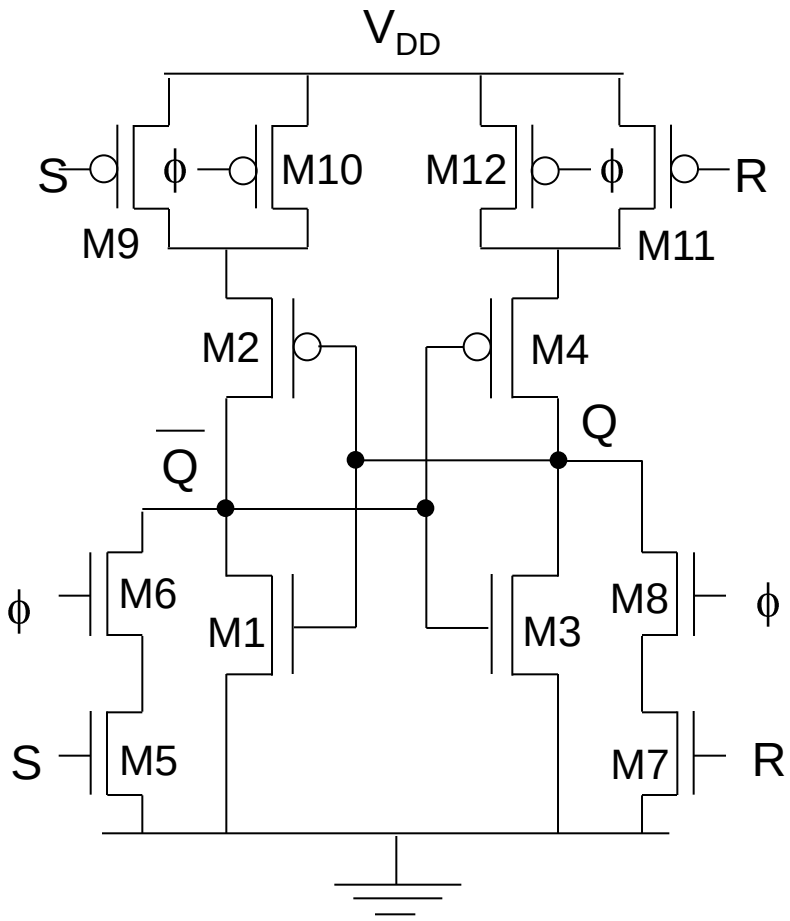
Flip-Flop: Transistor Sizing



Propagation Delay



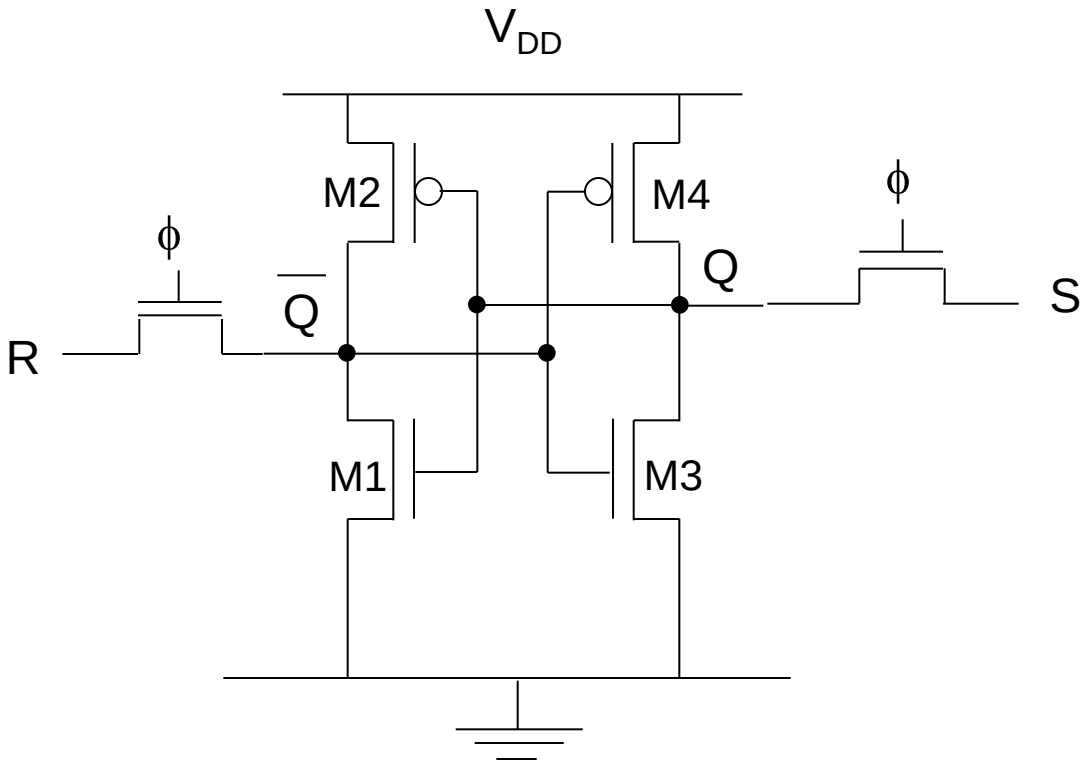
Complementary CMOS SR Flip-Flop

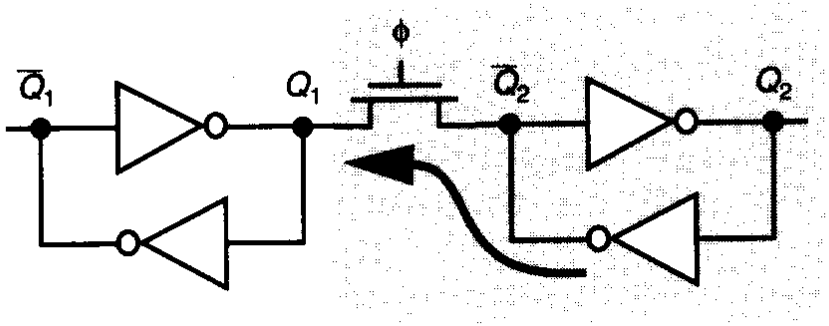


Eliminates pseudo-NMOS inverters

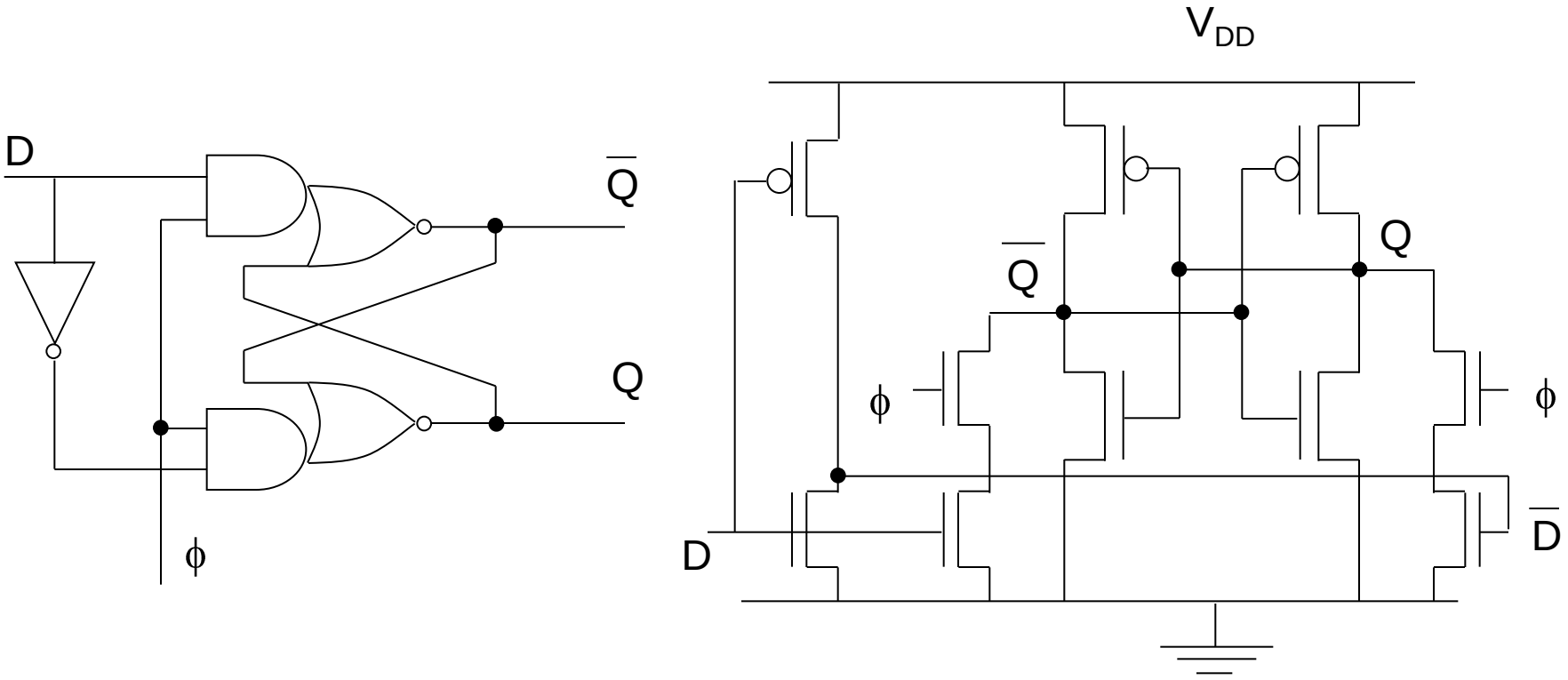
$\Rightarrow$ Faster switching and smaller transient current

6-Transistor SR Flip-Flop

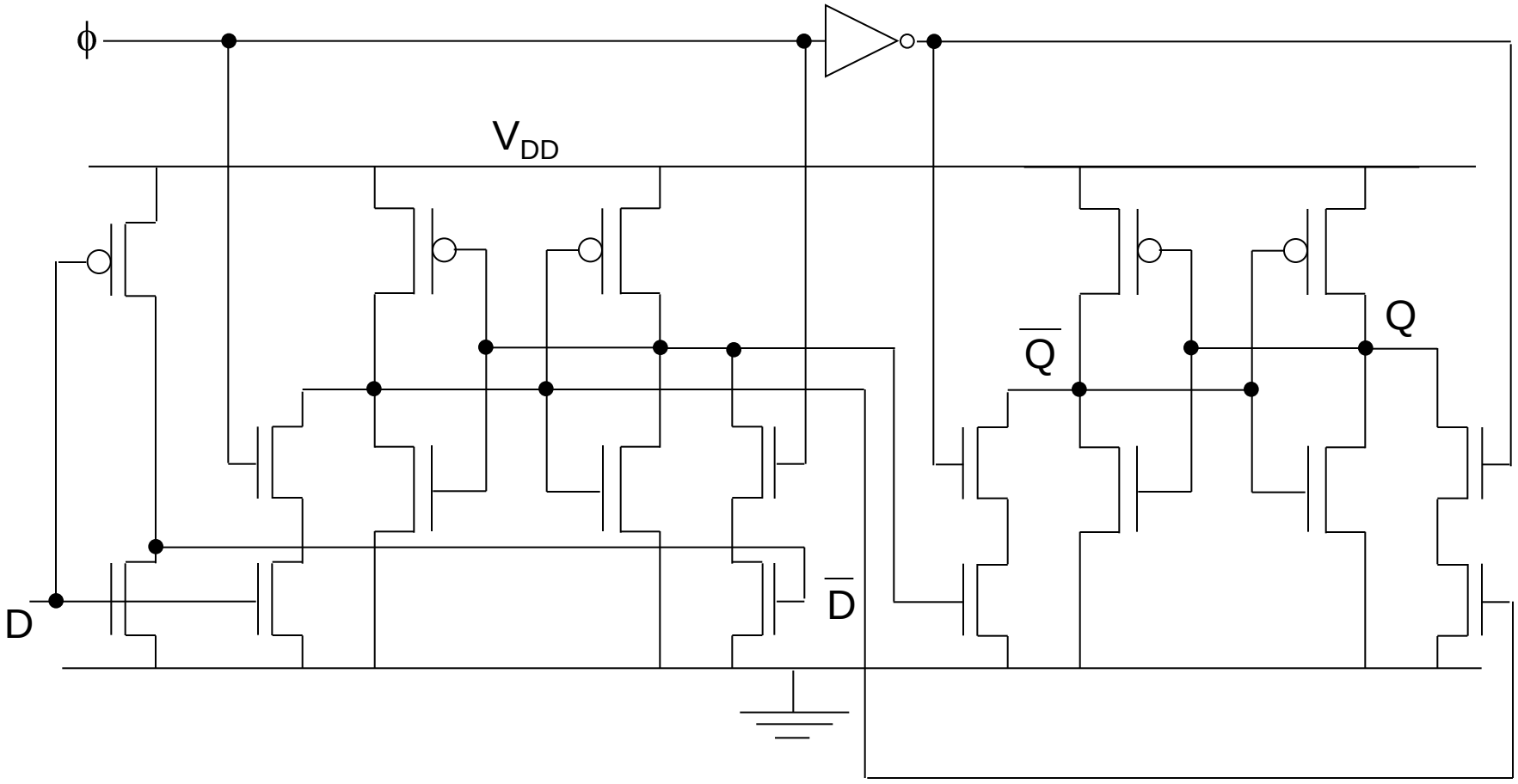




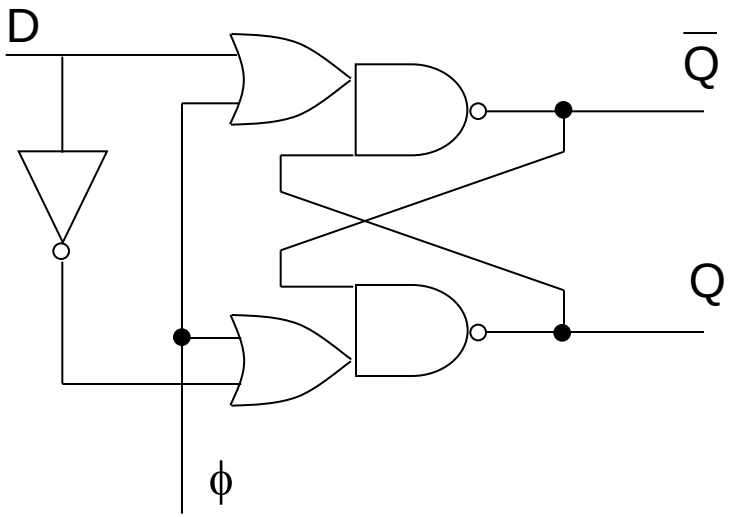
CMOS D Flip-Flop

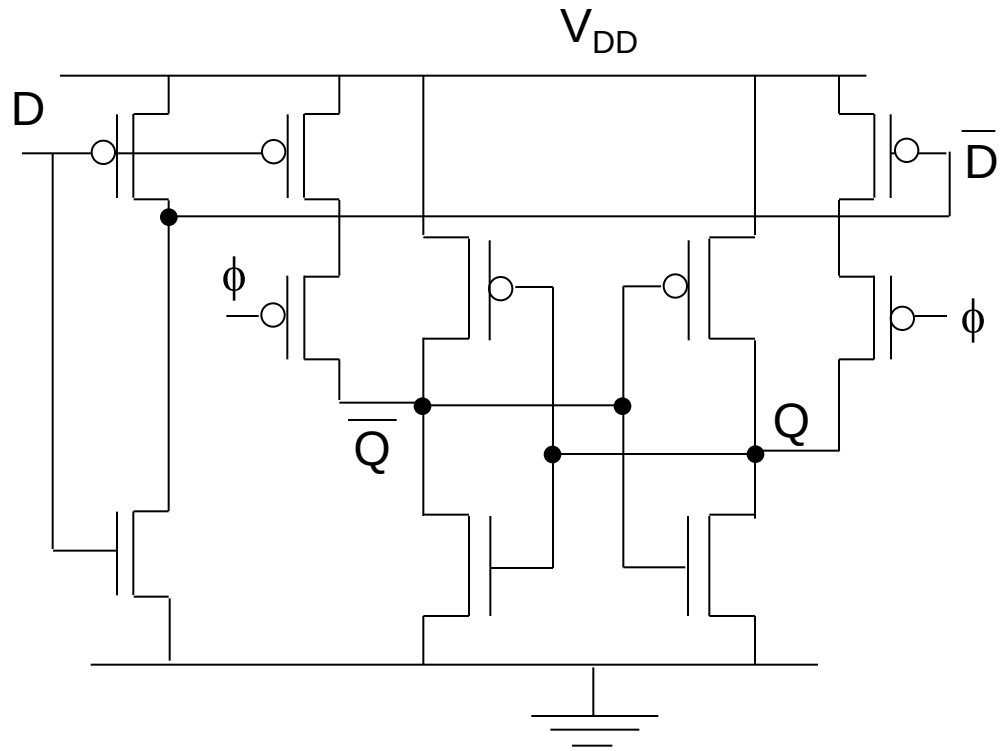


Master-Slave D Flip-Flop

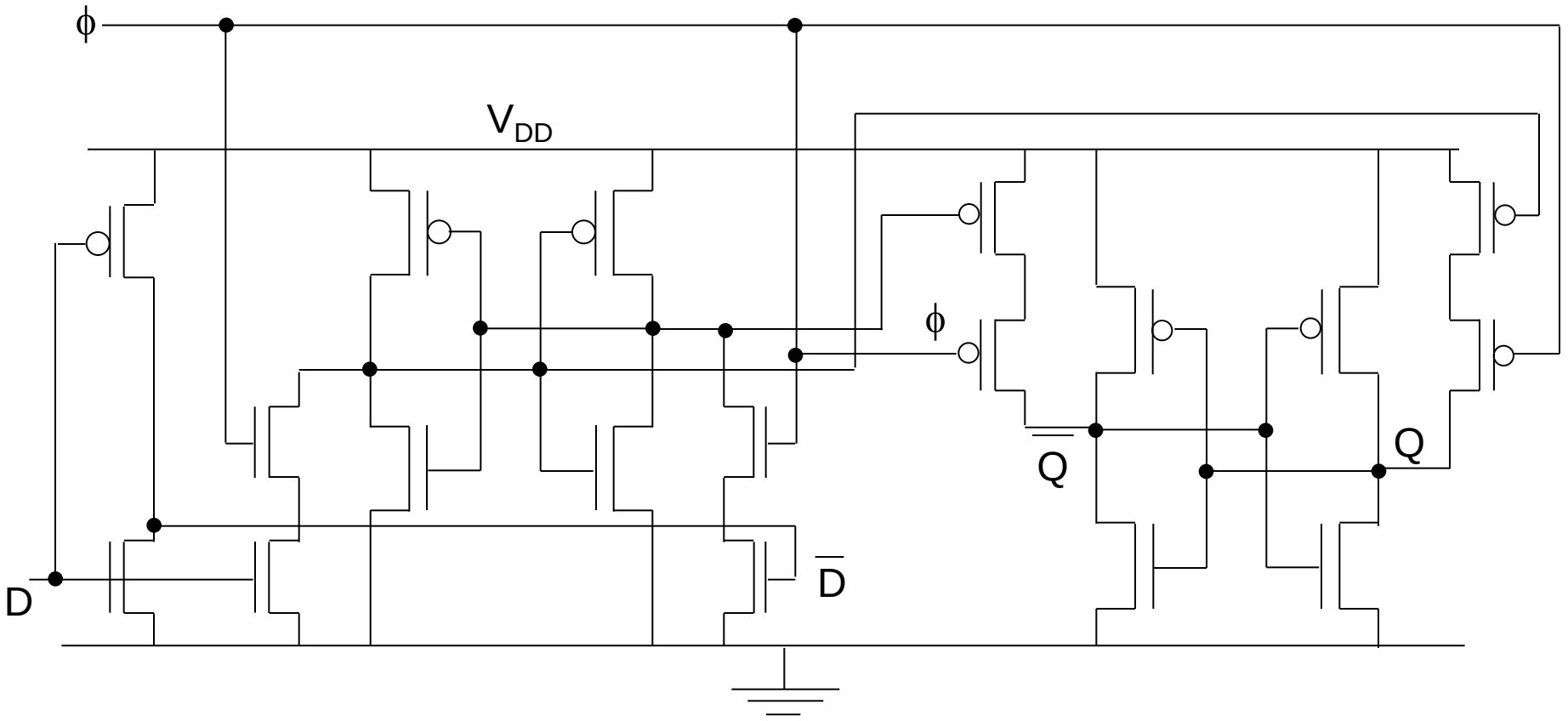


Negative-Level Sensitive D Flip-Flop

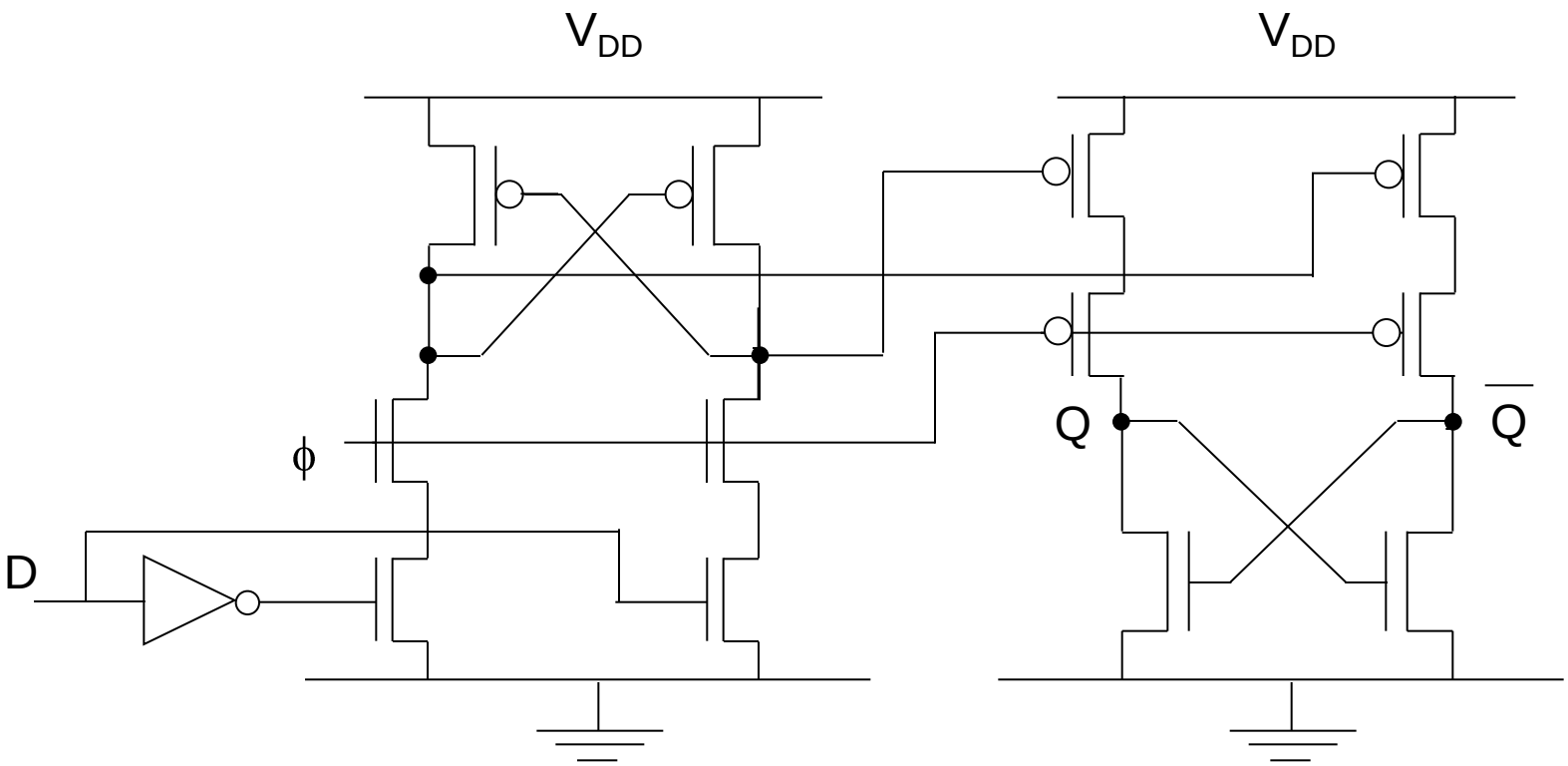




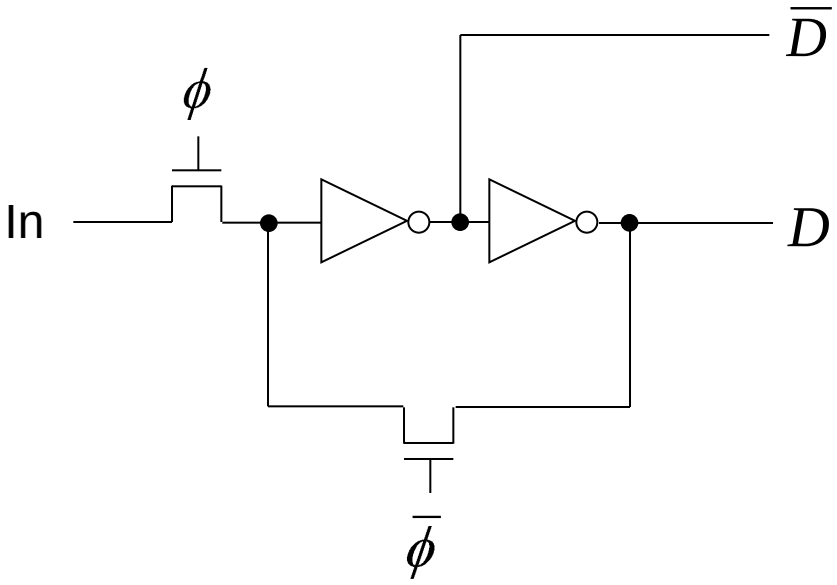
Master-Slave D Flip-Flop

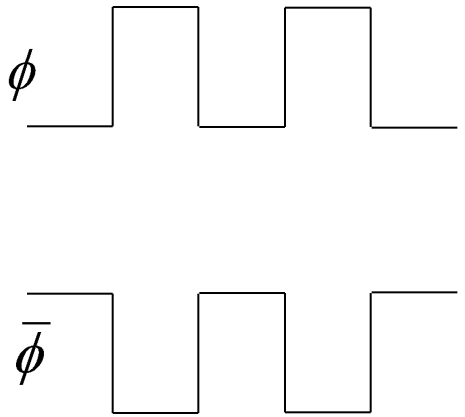


CVSL-Style Master-Slave D-FF



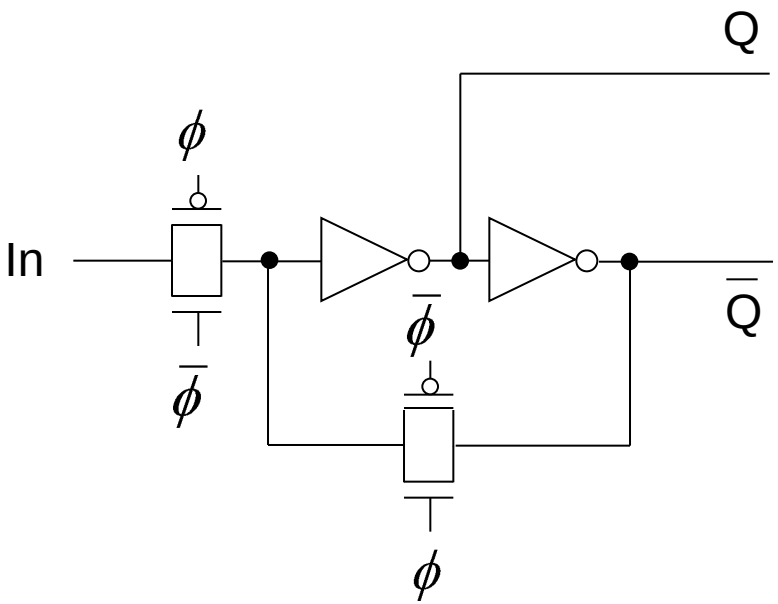
Charge-Based Storage

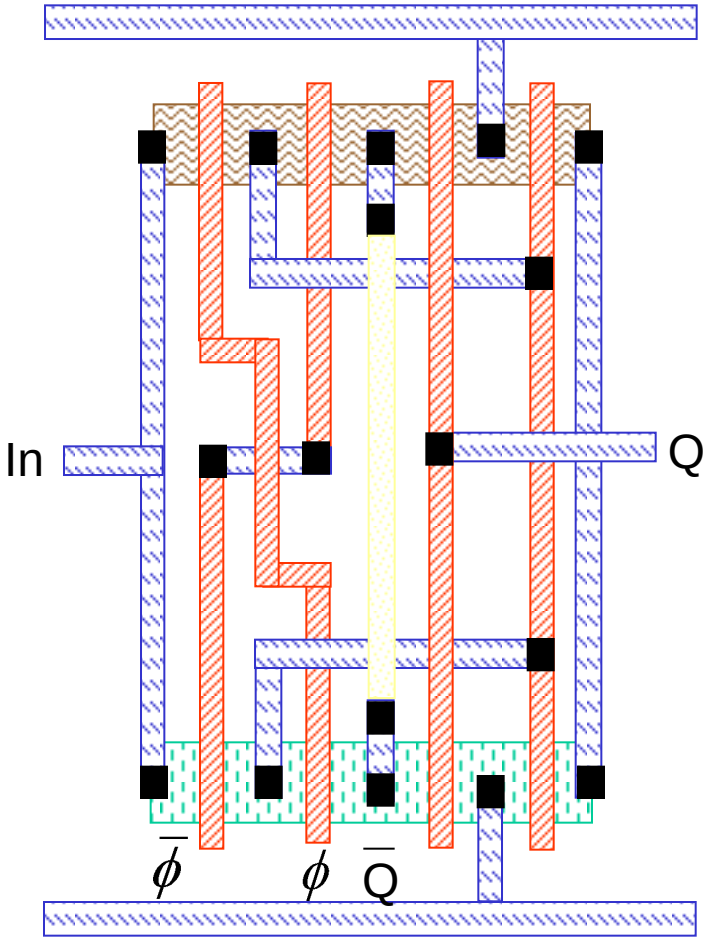




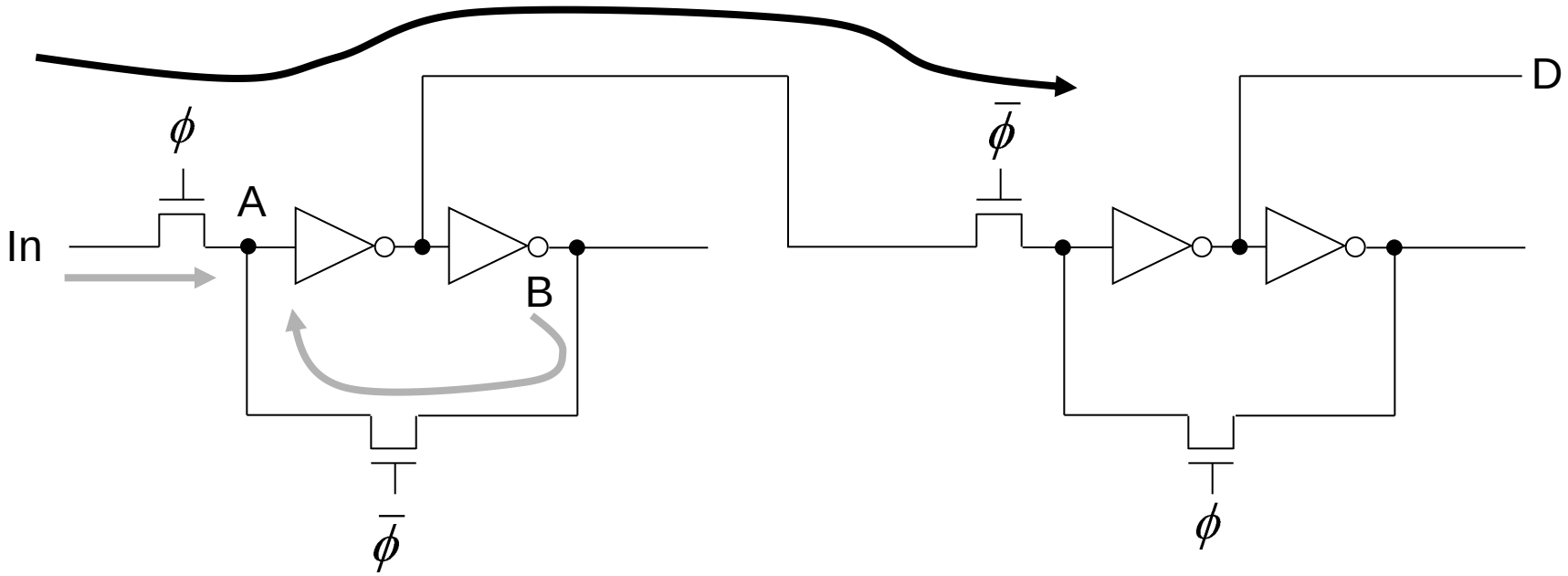
Pseudo-static Latch

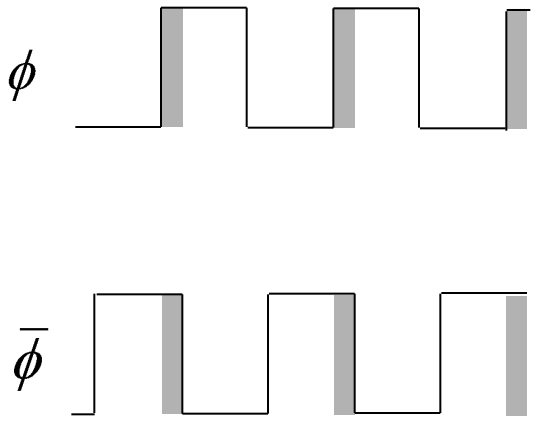
Layout of a D Flip-Flop





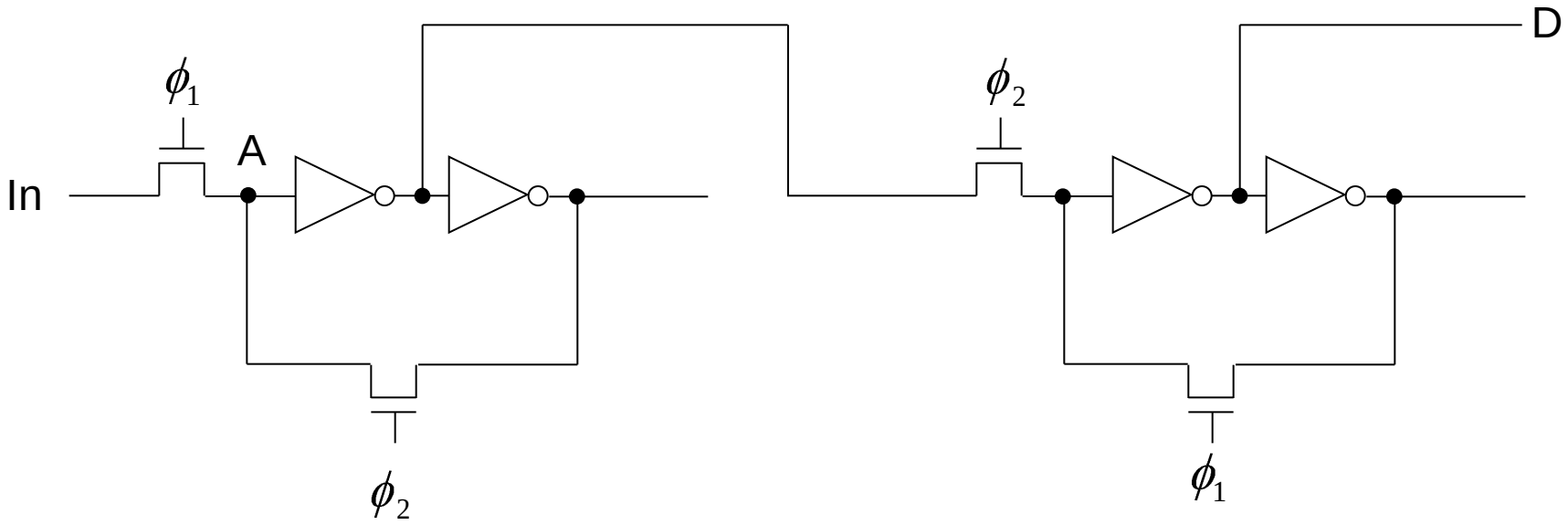
Master-Slave Flip-Flop

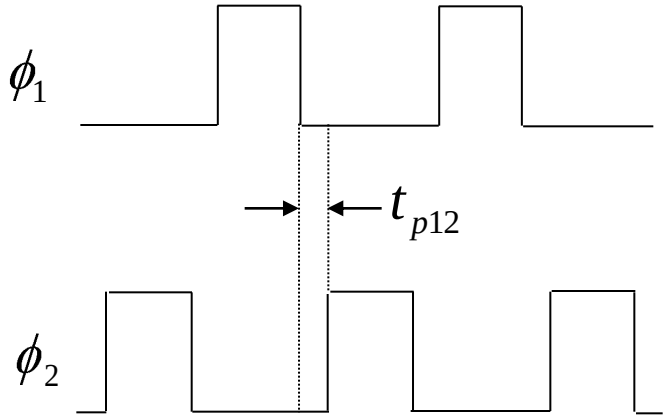




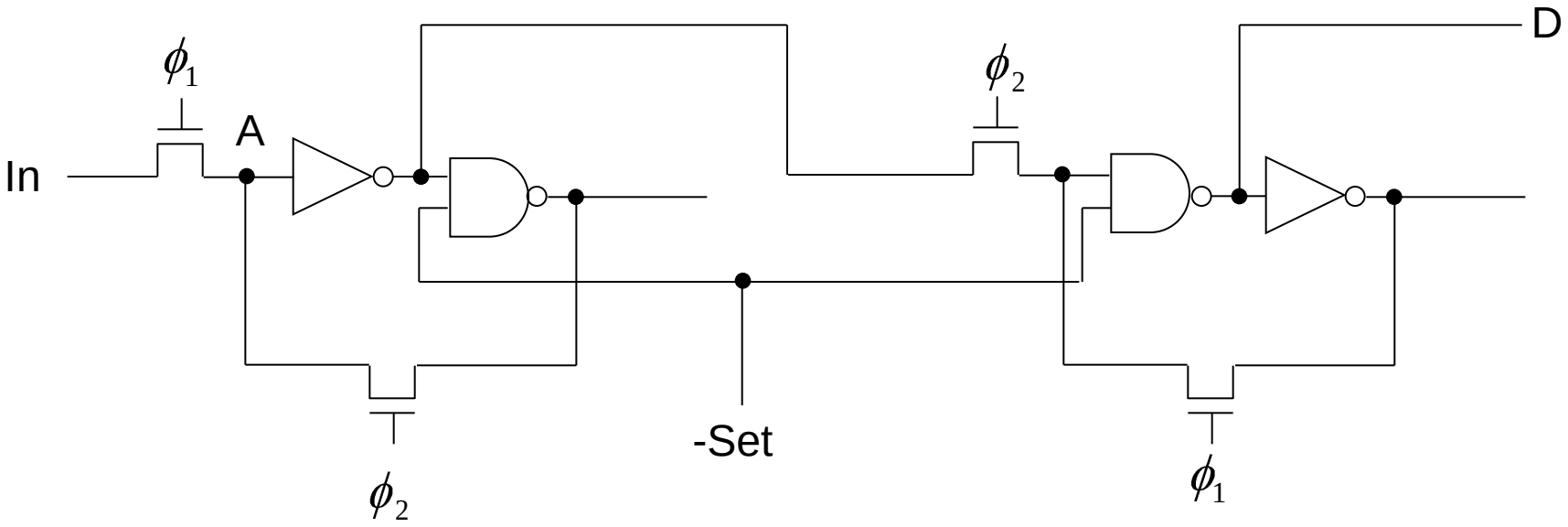
- Overlapping clocks can cause
  - race conditions
  - undefined signals

2 Phase Non-Overlapping Clocks

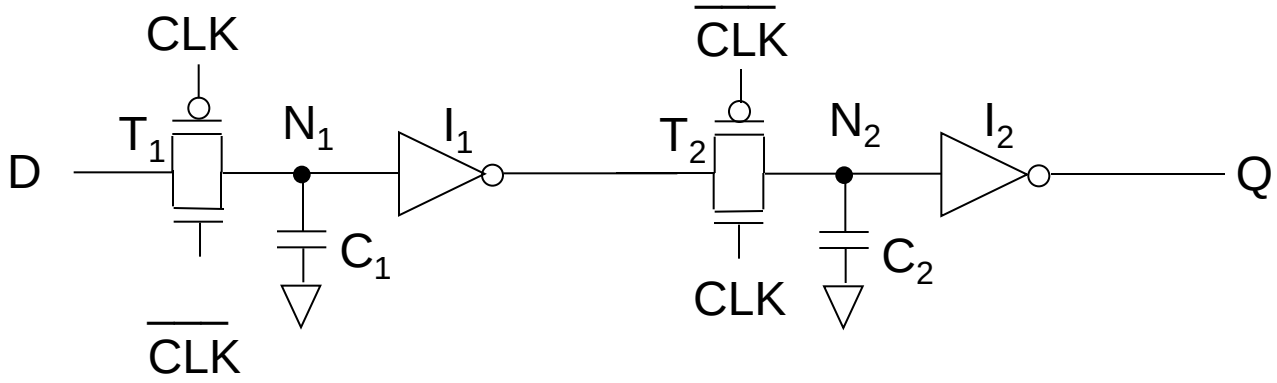


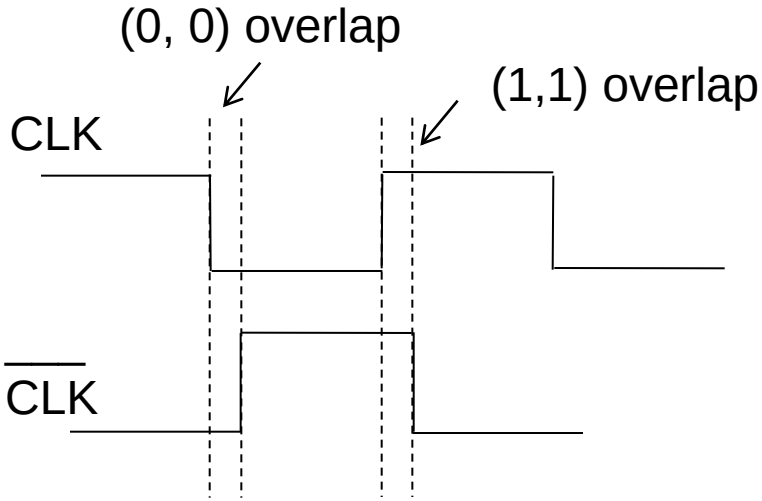


Asynchronous Setting



Dynamic Edge-Triggered Register

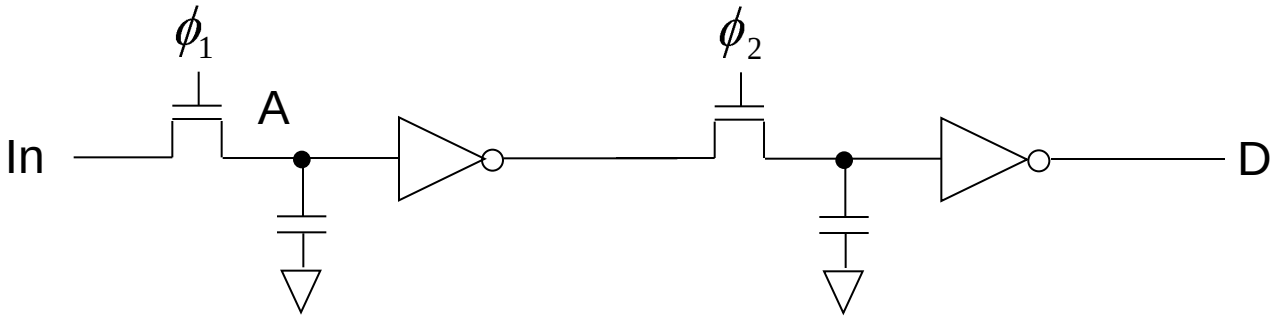


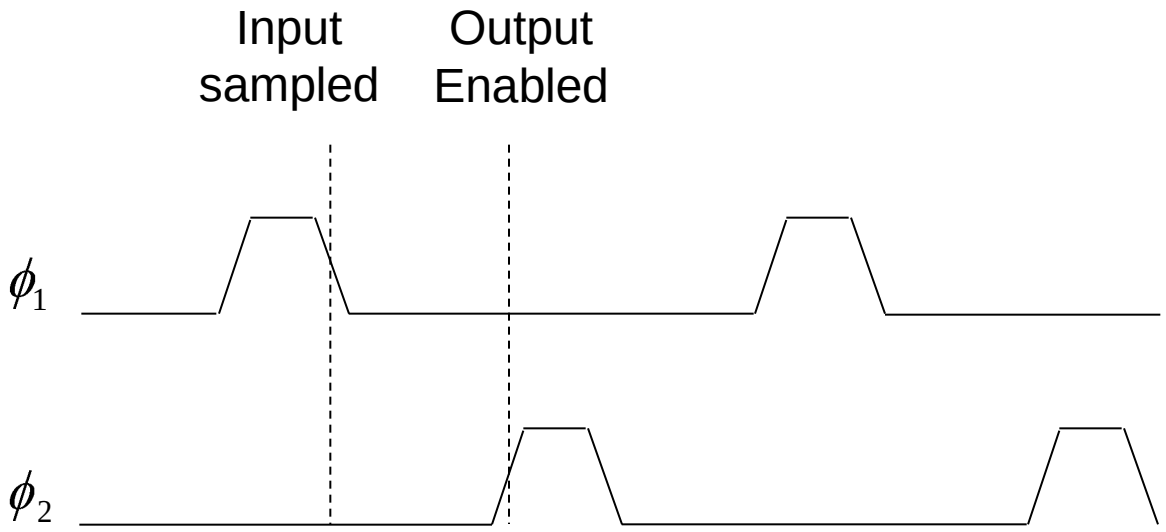


$$t_{(0,0)overlap} < t_{T1} + t_{I1} + t_{T2}$$

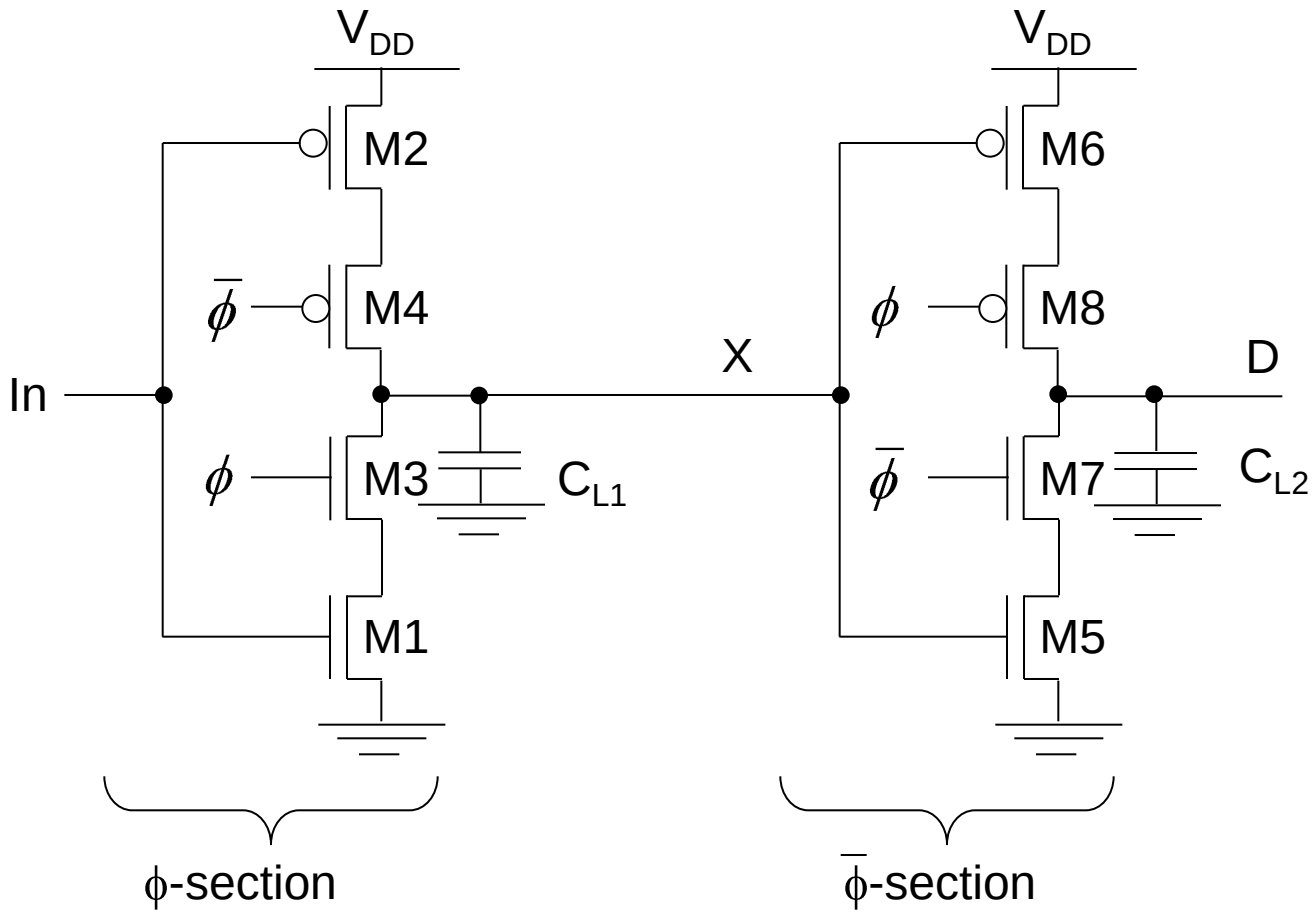
$$t_{hold} > t_{(1,1)overlap}$$

2-phase Dynamic Flip-Flop



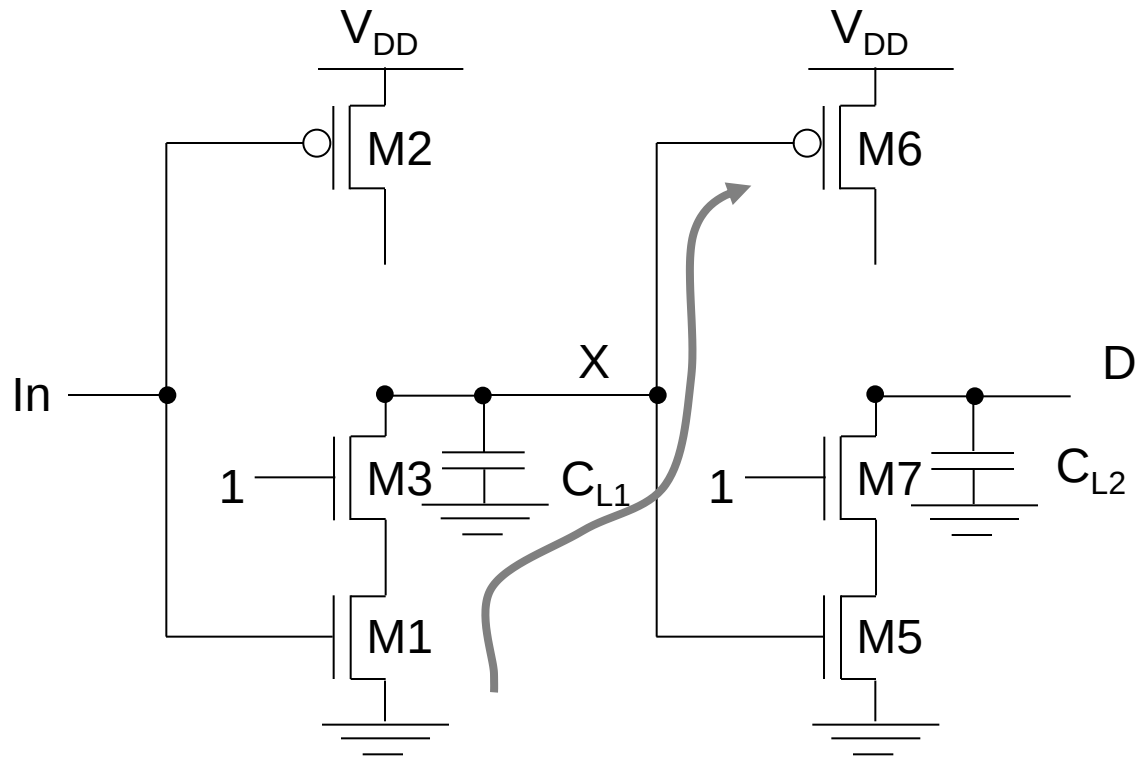


Flip-flop Insensitive to Clock Overlap



C²MOS Latch or Clocked CMOS Latch

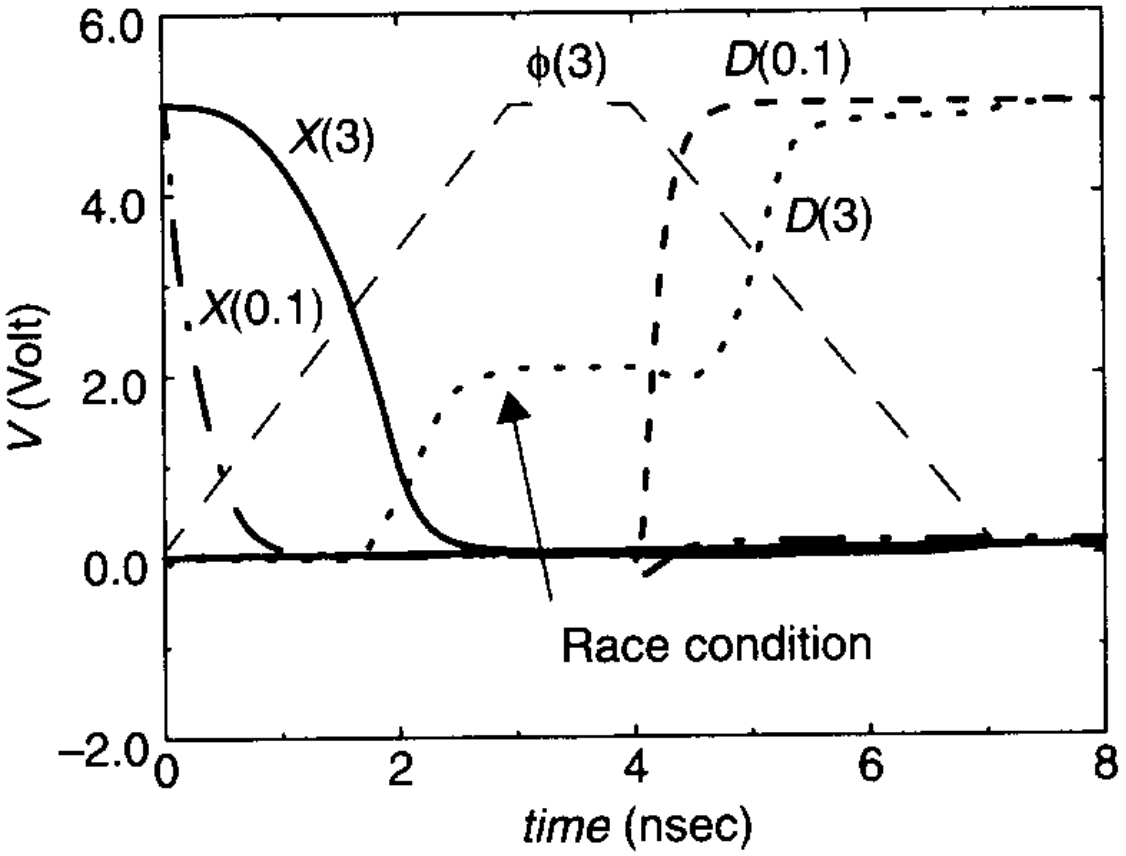
C^2MOS Latch Avoids Race Conditions



- Cascaded inverters: needs one pull-up followed by one pull-down, or vice versa to propagate signal
- (1-1) overlap: Only the pull-down networks are active, input signal cannot propagate to the output
- (0-0) overlap: only the pull-up networks are active

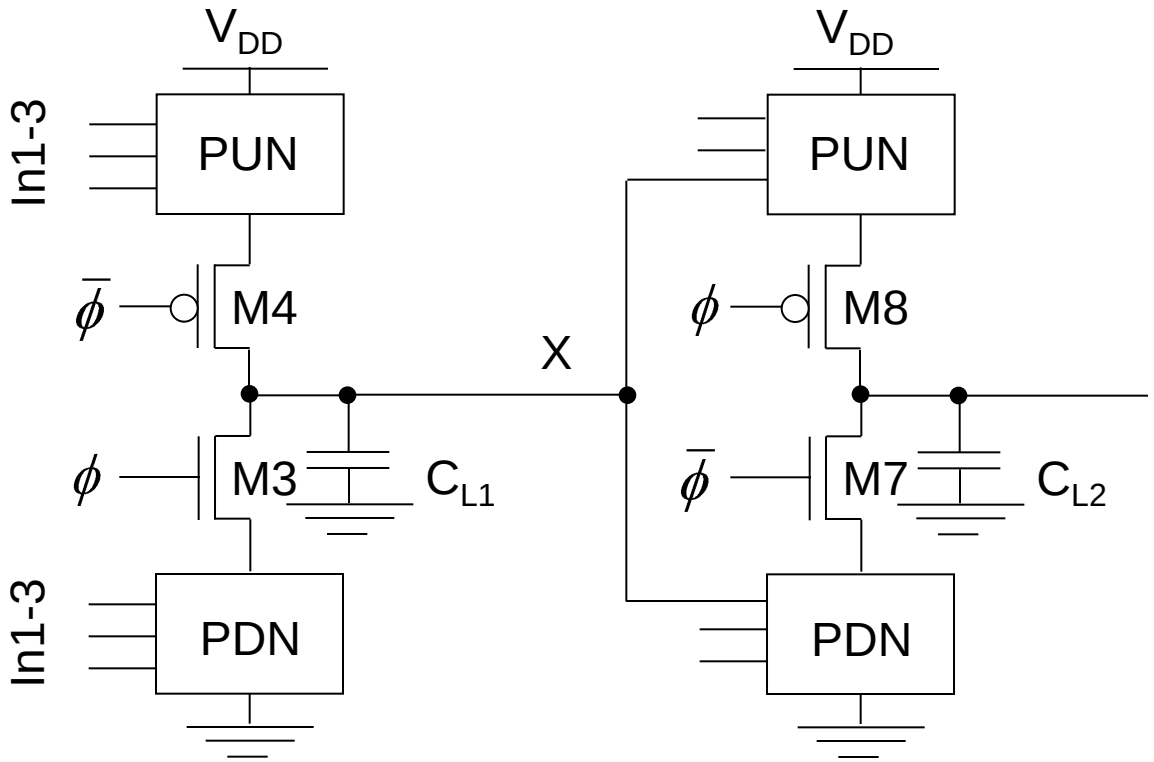
C^{2}MOS Latch Avoids Race Conditions

- C^{2}MOS latch is insensitive to overlap, as long a the rise and fall times of clock edges are sufficiently small



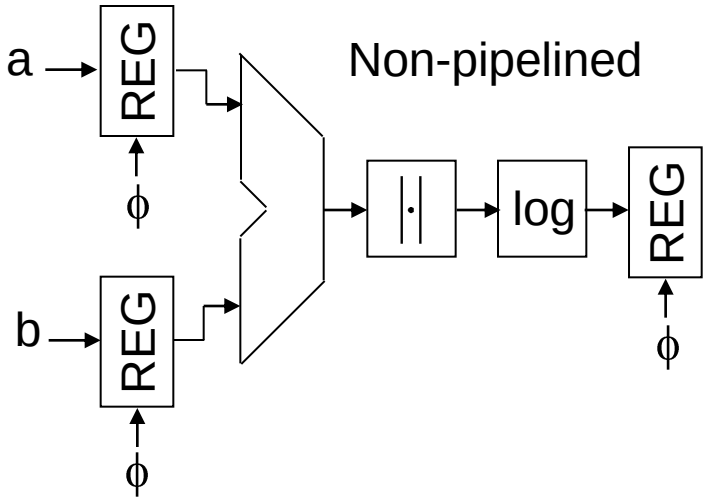
Clocked CMOS Logic

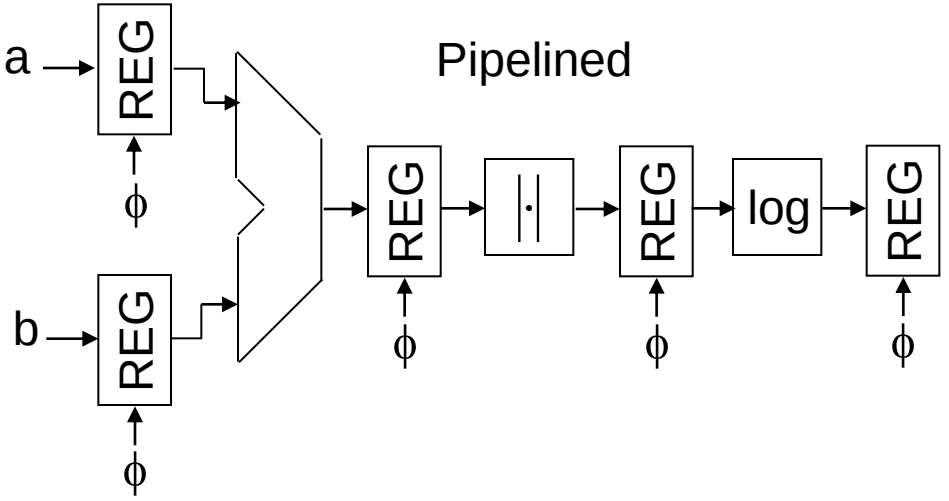
- Replace the inverter in a C^2MOS latch with a complementary CMOS logic



- Divide the computation into stages: Pipelining

Pipelining



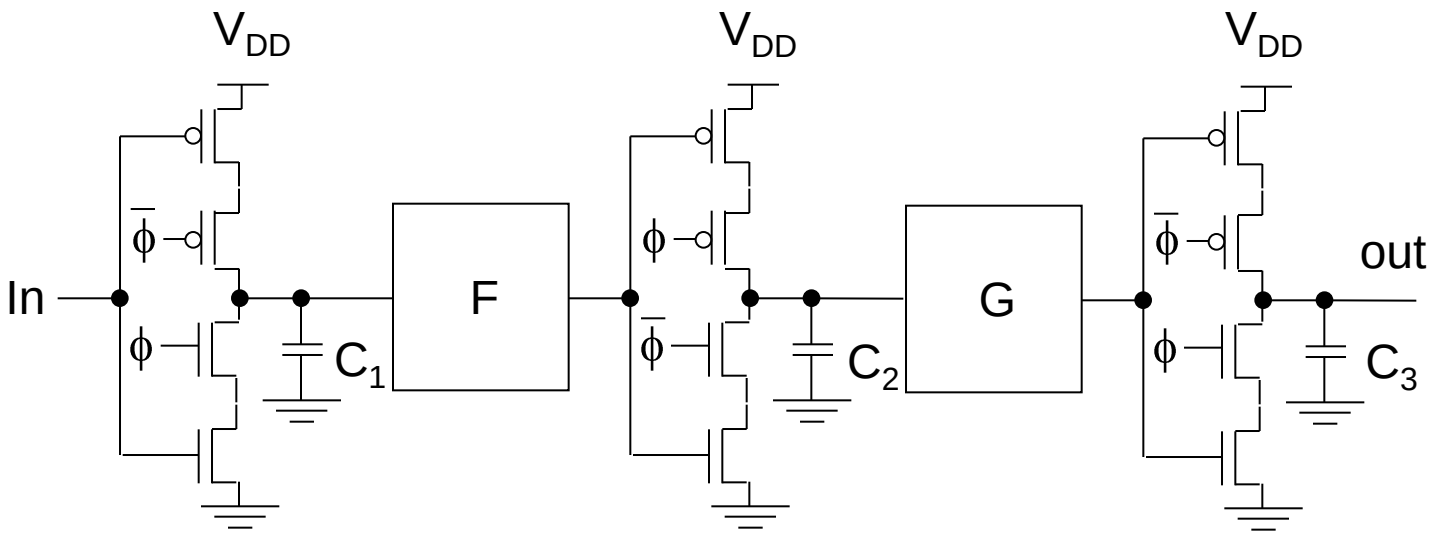


$$T_{\min} = t_{p,reg} + t_{p,logic} + t_{setup,reg}$$

$$T_{\min,pipe} = t_{p,reg} + \max(t_{p,adder}, t_{p,abs}, t_{p,\log}) + t_{setup,reg}$$

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 - b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$

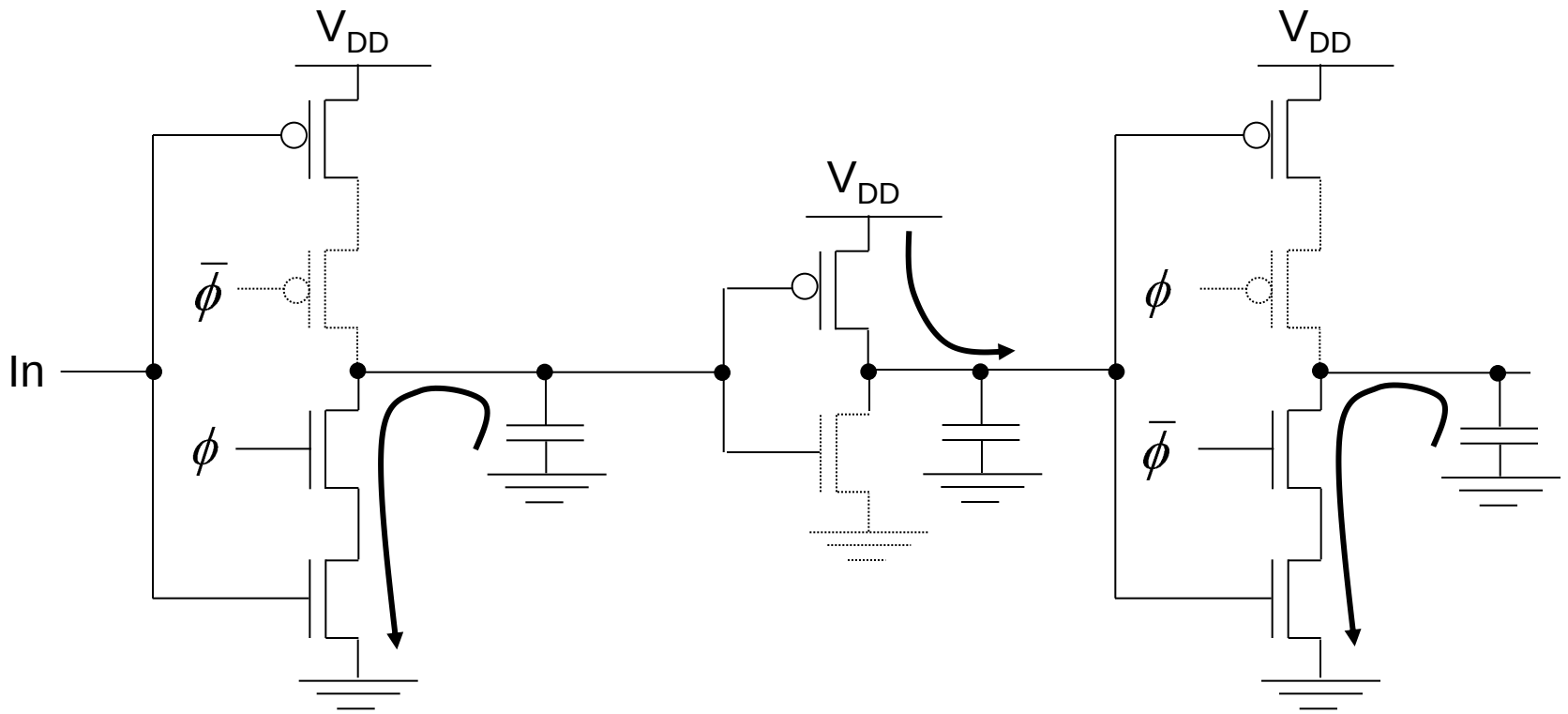
Pipelined Logic using C^2MOS



NORA CMOS (NO-RAce logic)

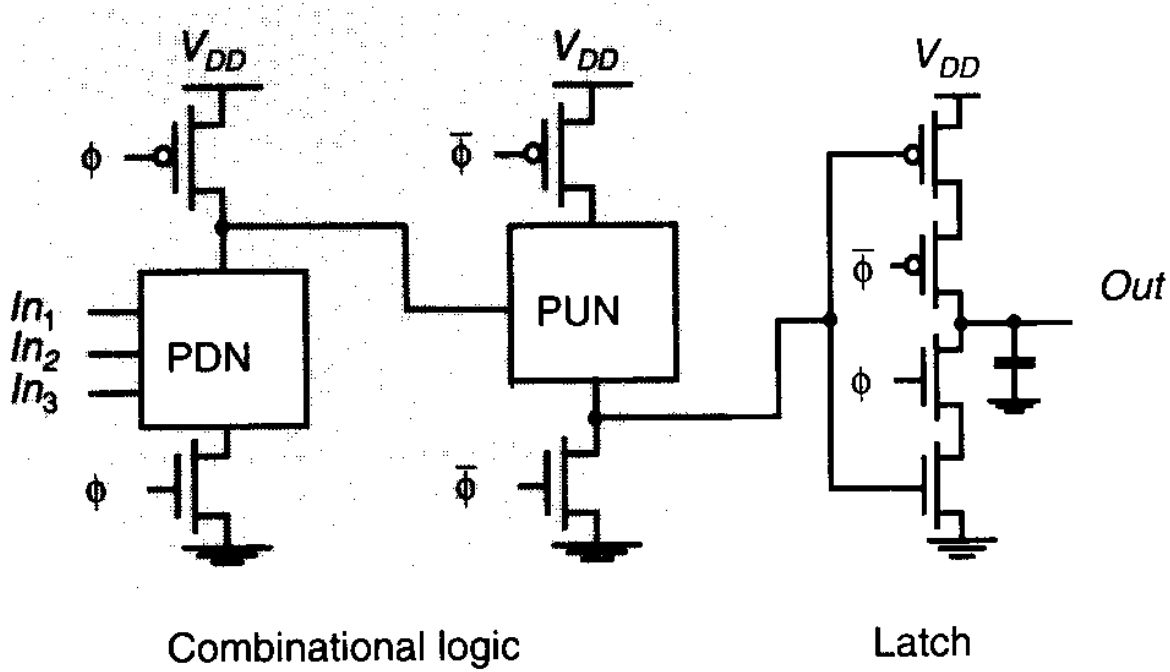
Race free as long as all the logic functions F and G between the latches are non-inverting

Example



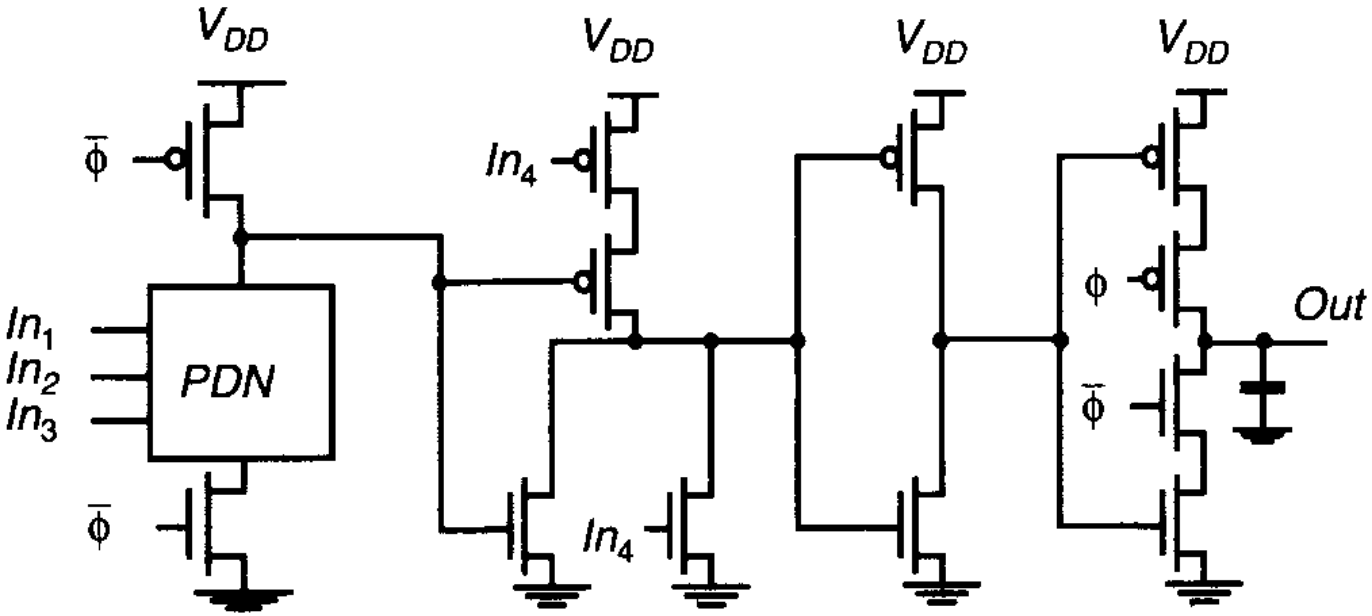
Number of static inversion should be even

NORA CMOS ϕ-module



	Logic	Latch
$\phi = 0$	Precharge	Hold
$\phi = 1$	Evaluate	Evaluate

NORA CMOS $\overline{\phi}$-module

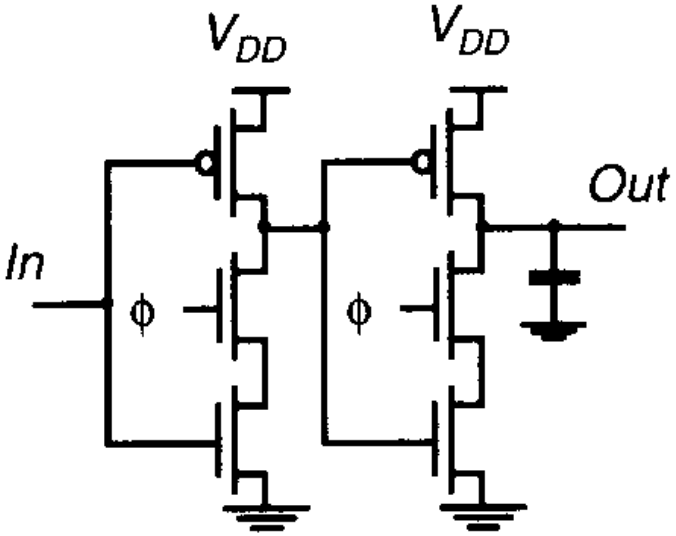


	Logic	Latch
$\phi = 0$	Evaluate	Evaluate
$\phi = 1$	Precharge	Hold

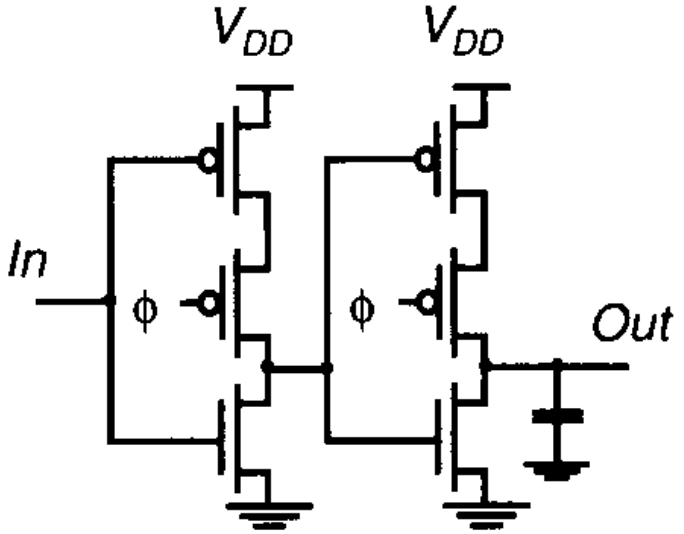
NORA Logic

- NORA data path consists of a chain of alternating ϕ and $\overline{\phi}$ modules
- Dynamic-logic rule: single $0 \rightarrow 1$ ($1 \rightarrow 0$) transition for dynamic ϕn-block (ϕp-block)
- C^2MOS rule:
  - If dynamic blocks are present, even number of static inversions between a latch and a dynamic block
  - Otherwise, even number of static inversions between latches
- Static logic may glitch, best to keep all of them after dynamic blocks

Doubled C^{2}MOS Latches

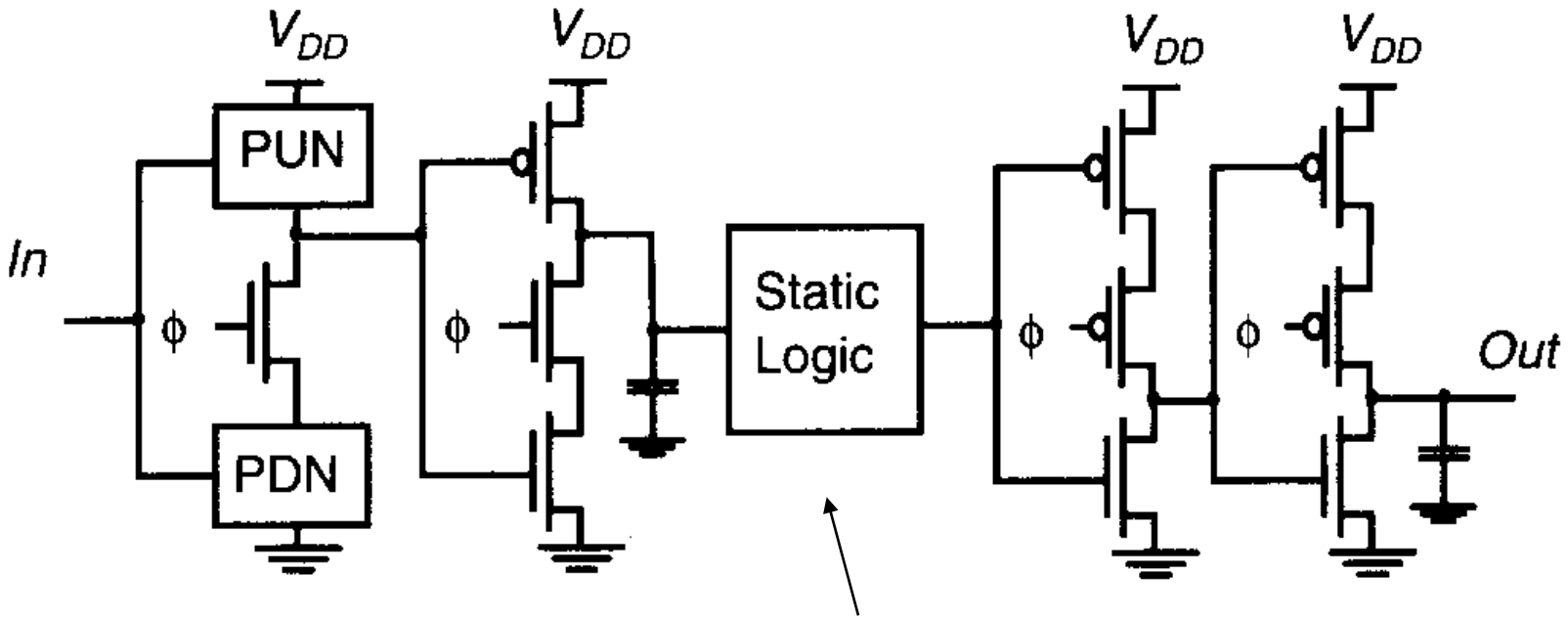


Doubled n-C^{2}MOS latch



Doubled p-C^{2}MOS latch

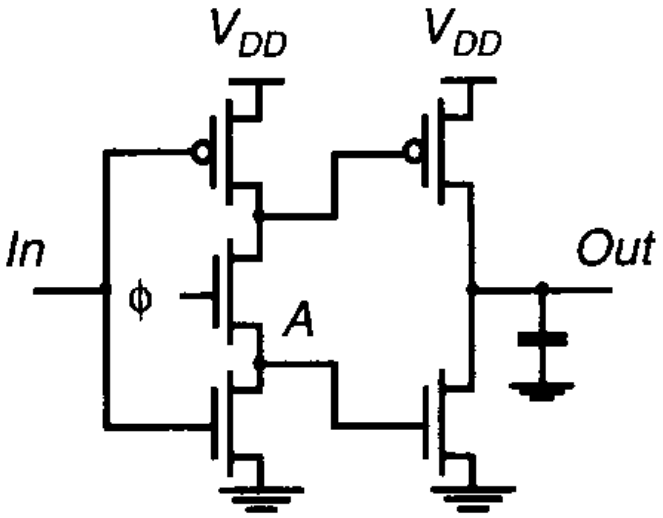
TSPC - True Single Phase Clock Logic

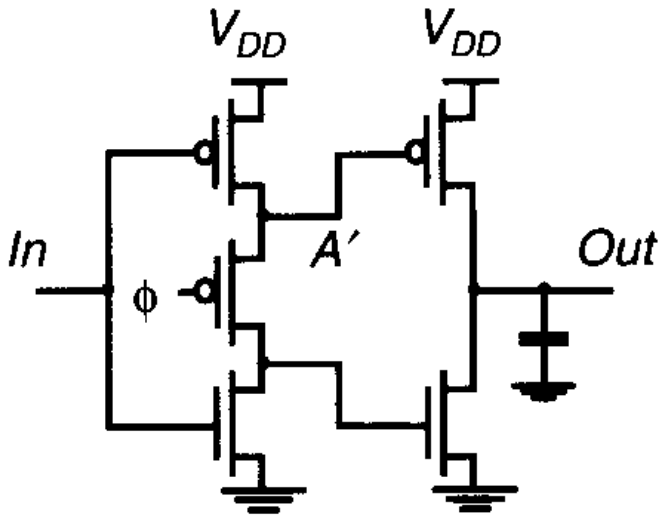


Including logic into the latch

Inserting logic between the latches

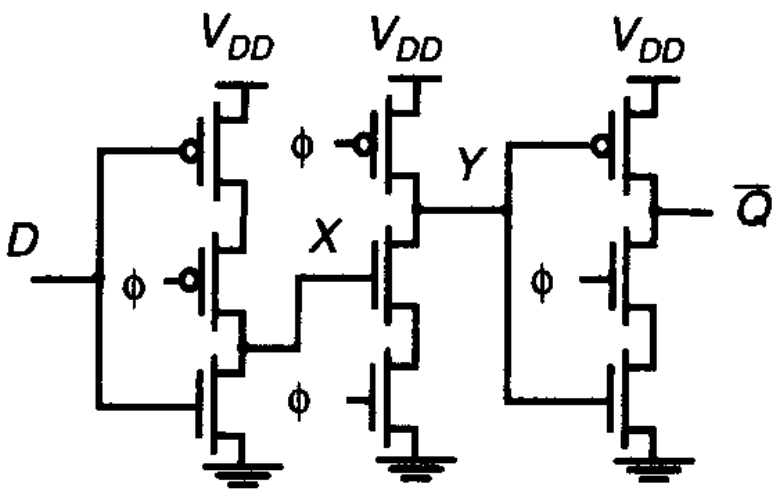
Simplified TSPC Latches



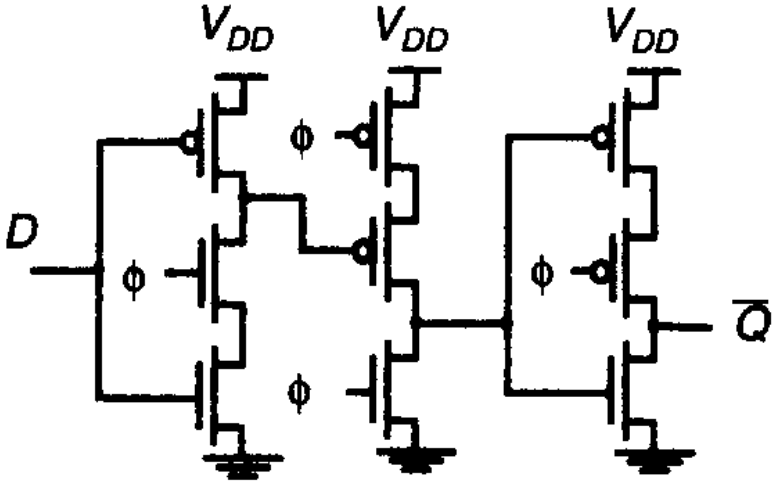


A and A’ do not have full logic swing

Master-Slave Flip-flops

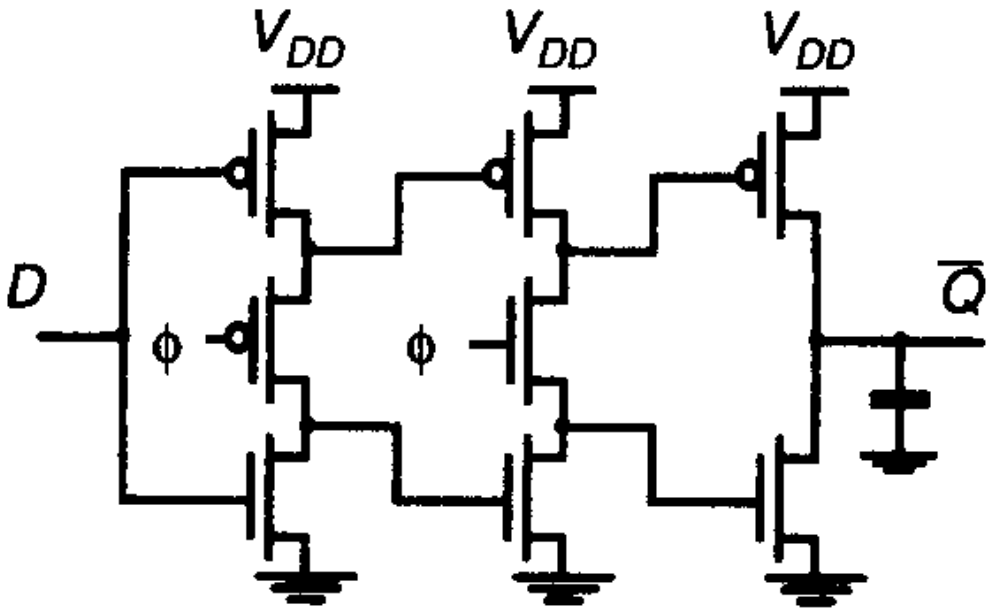


Positive-edge triggered D-FF



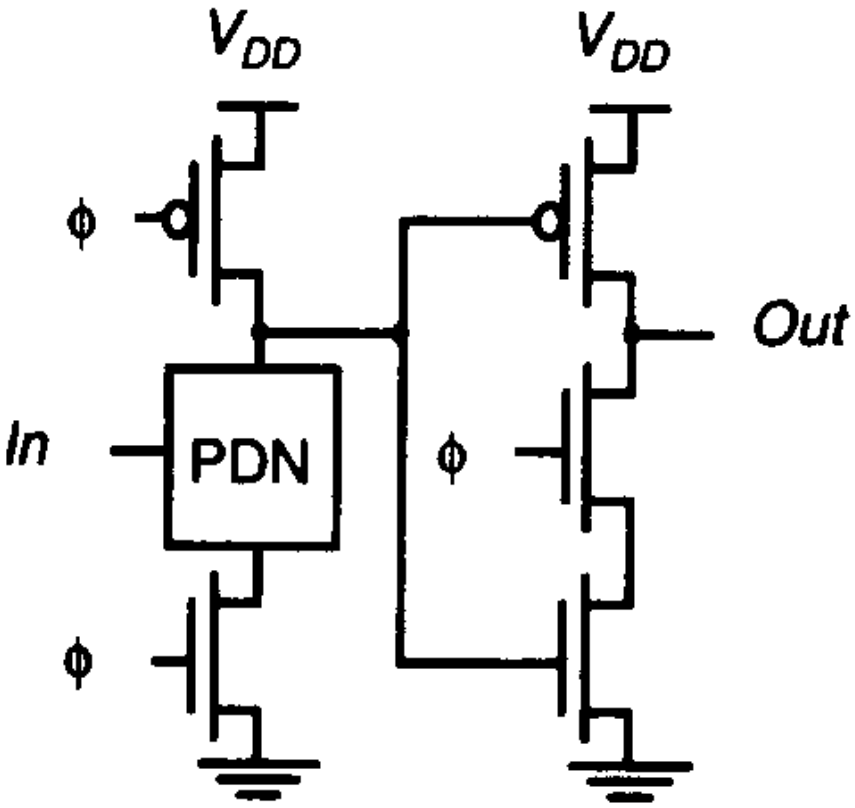
Negative-edge triggered D-FF

Master-Slave Simplified TSPC Flip-Flops

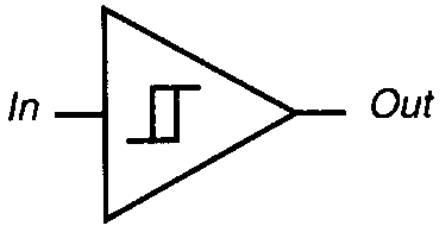


- Positive edge-triggered D flip-flops
- Reduces clock load

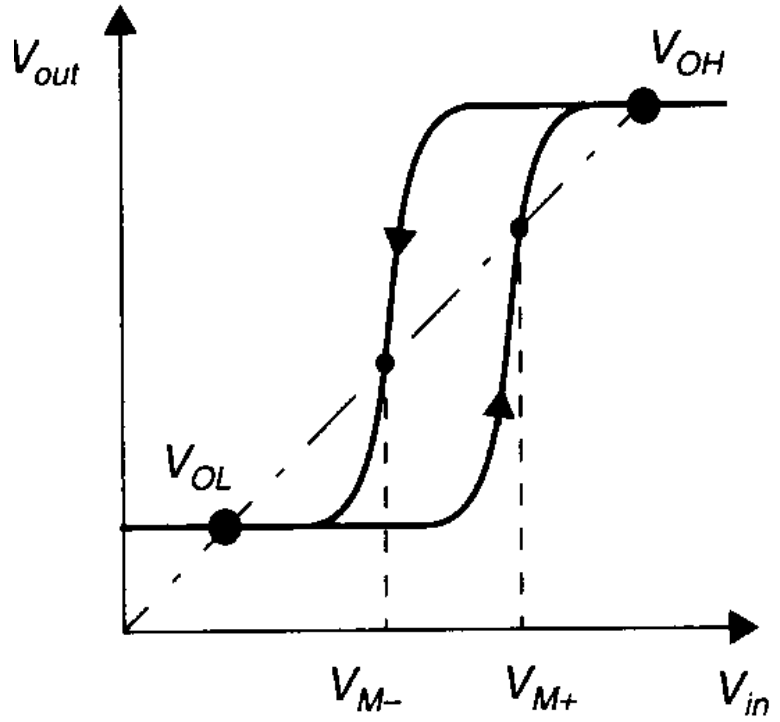
Further Simplication



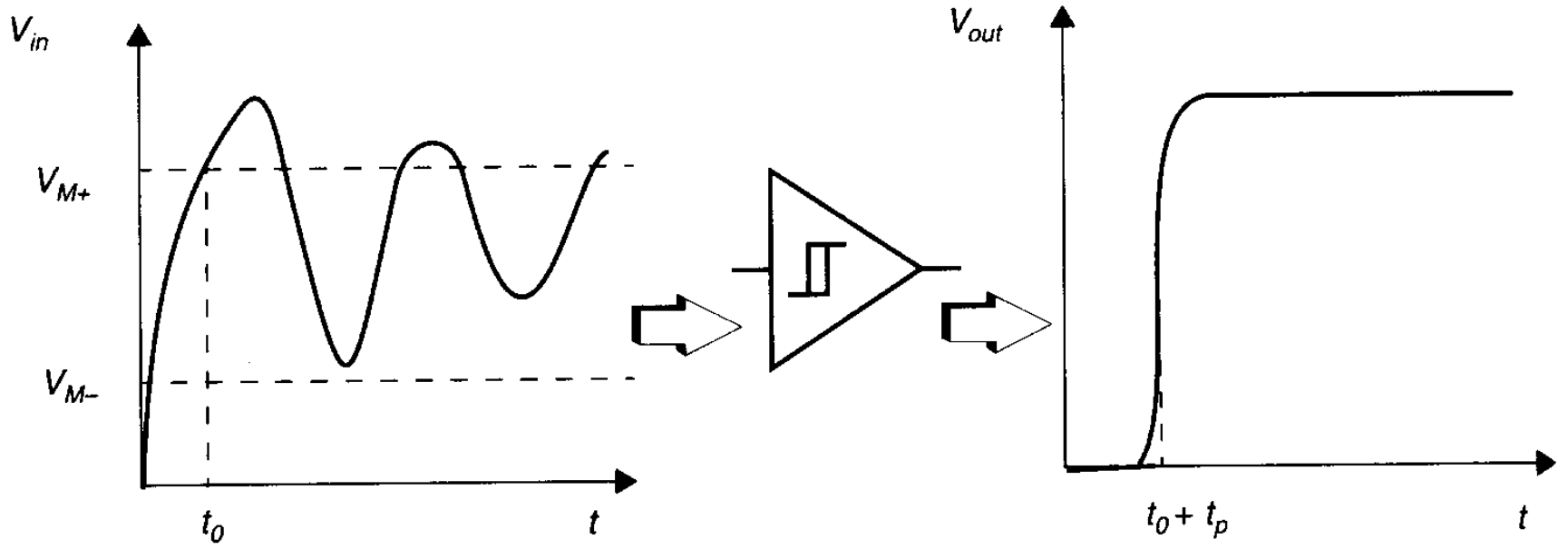
Schmitt Trigger



- VTC with hysteresis
- Restores signal slopes

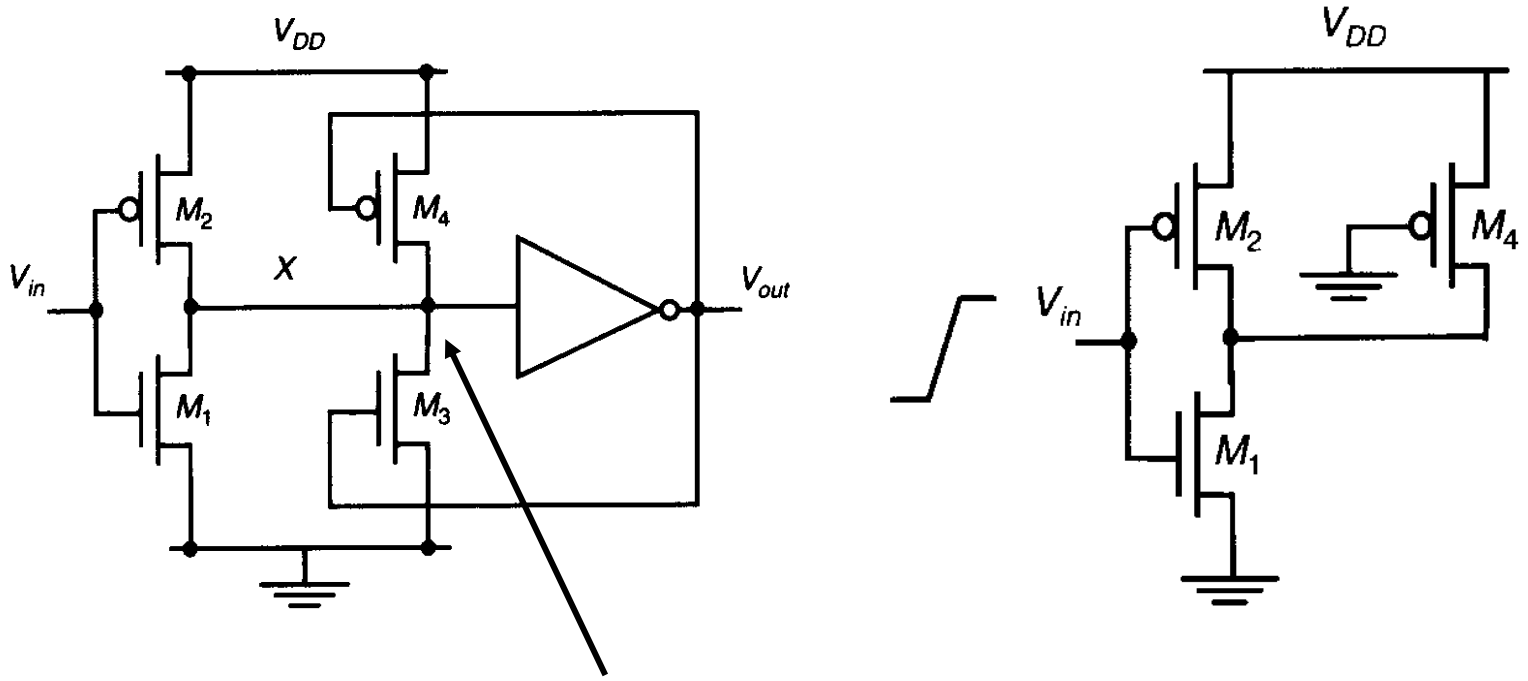


Noise Suppression using Schmitt Trigger



Sharp low-to-high transition

CMOS Schmitt Trigger



Moves switching threshold
of first inverter

Sizing of M3 and M4

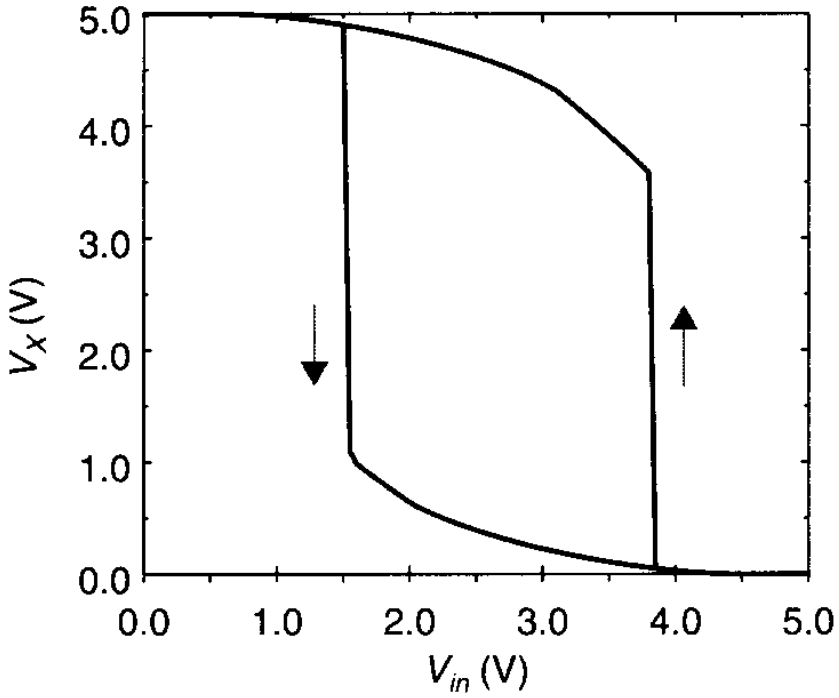
- V_{M+} = 3.5V
  - M1 and M2 are in saturation; M4 is in triode region

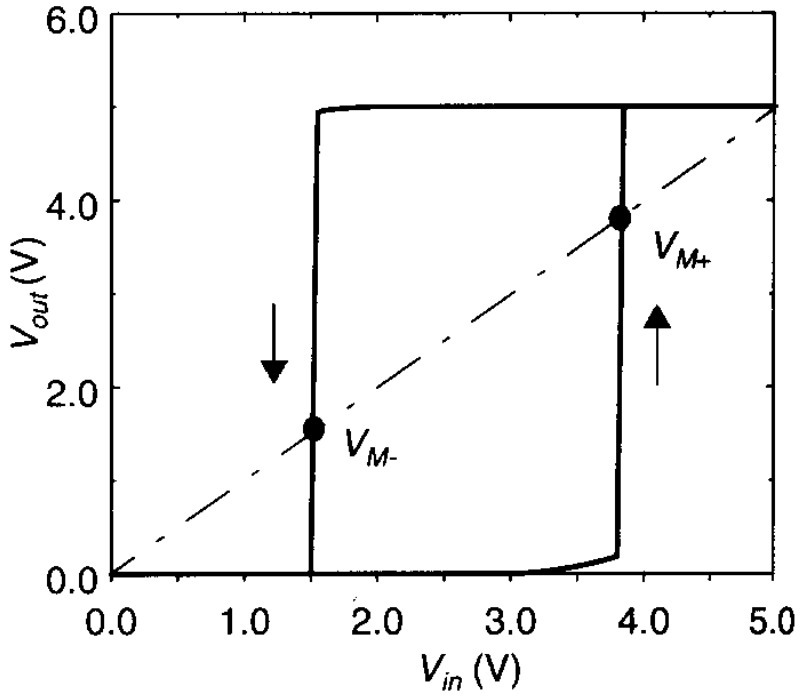
$$\frac{k_1}{2}\left(V_{M+}-V_{tn}\right)^2 =$$

$$\frac{k_2}{2}\left(V_{DD}-V_{M+}-|V_{tp}|\right)^2 + k_4\left(\left(V_{DD}-|V_{tp}|\right)\left(V_{DD}-V_{M+}\right)-\frac{\left(V_{DD}-V_{M+}\right)^2}{2}\right)$$

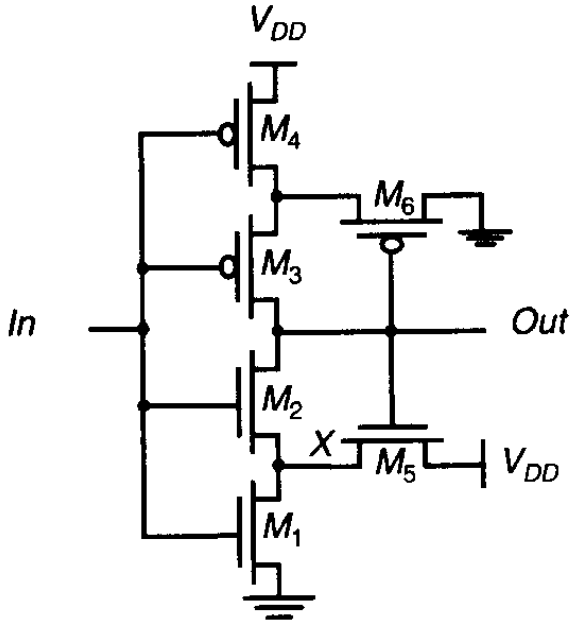
- V_{M-} = 1.5V
  - M1 and M2 are in saturation; M3 is in triode region

Schmitt Trigger: Simulated VTC





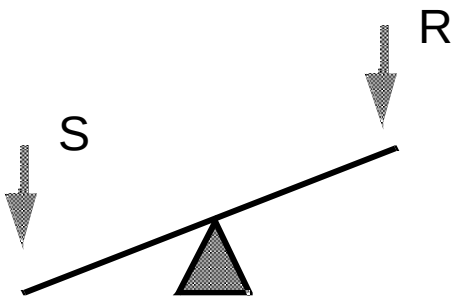
CMOS Schmitt Trigger



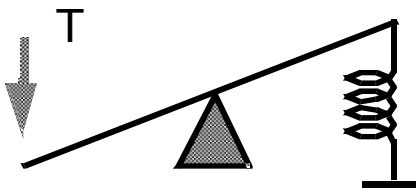
- In = 0, at steady state, $V_{Out} = V_{DD}$, $V_X = V_{DD} - V_{tn}$
- In makes a $0 \rightarrow 1$ transition
  - Saturated load inverter M1-M5 discharges X
  - M2 inactive until $V_X = V_{in} - V_{tn}$
  - Use V_{in} to approximate V_{M-}
  - M1-M5 in saturation

$$\frac{k_1}{2}\left(V_{M-} - V_{tn}\right)^2 = \frac{k_5}{2}\left(V_{DD} - V_{M-}\right)^2$$

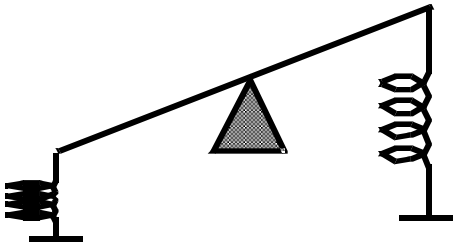
Multivibrator Circuits



Bistable Multivibrator
flip-flop, Schmitt Trigger

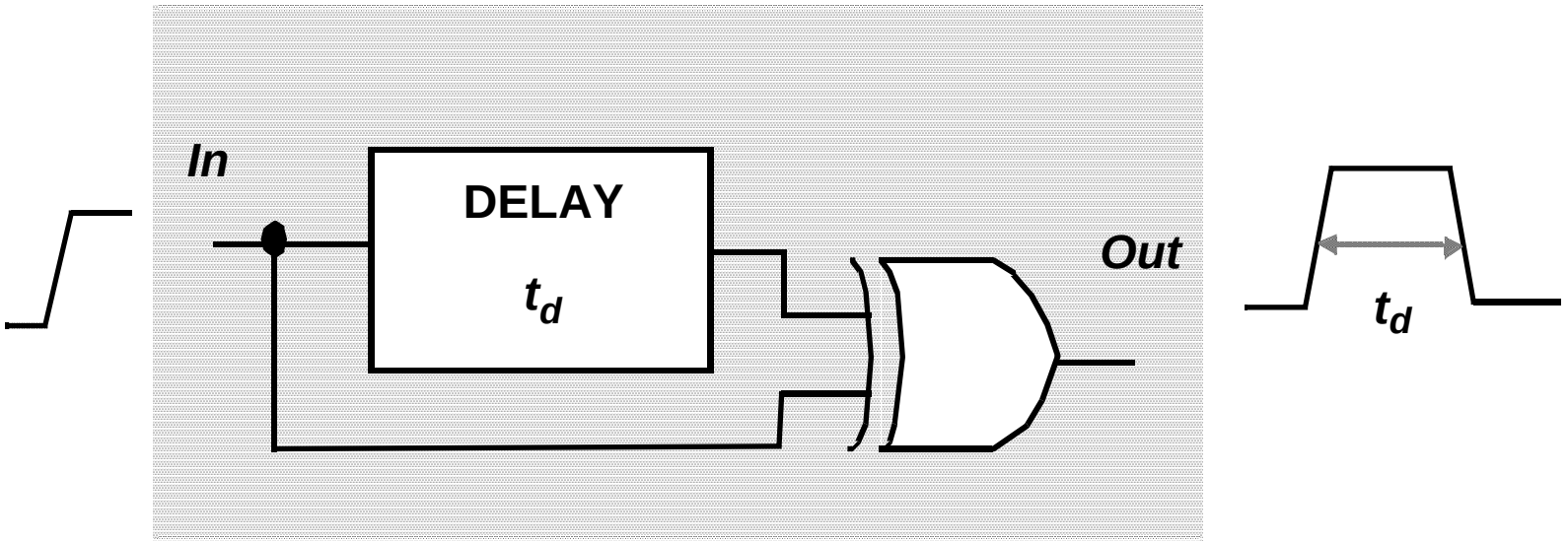


Monostable Multivibrator
one-shot



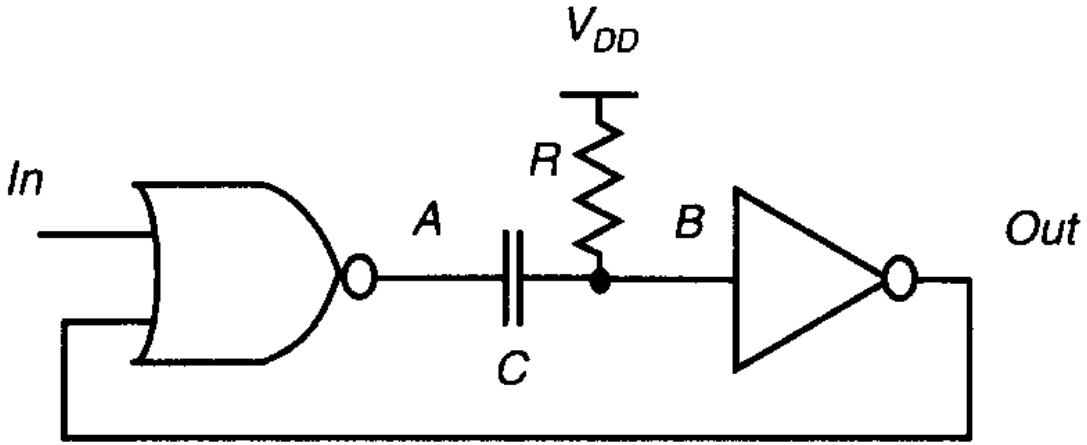
Astable Multivibrator
oscillator

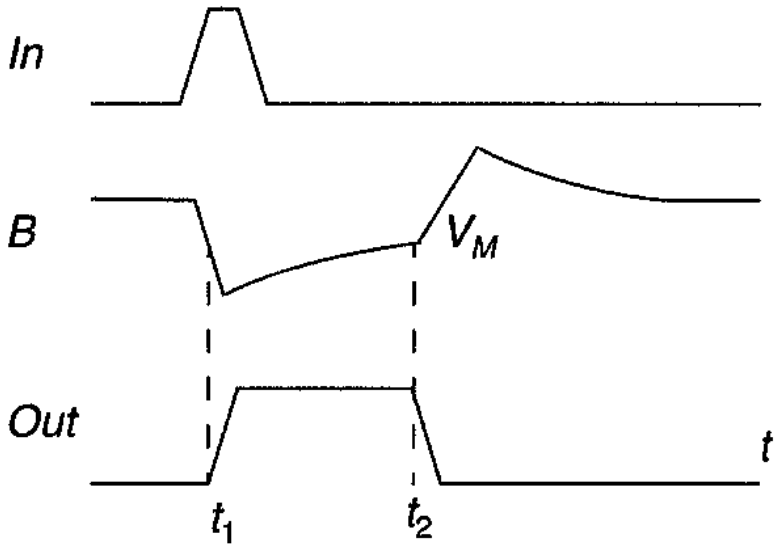
Transition-Triggered Monostable



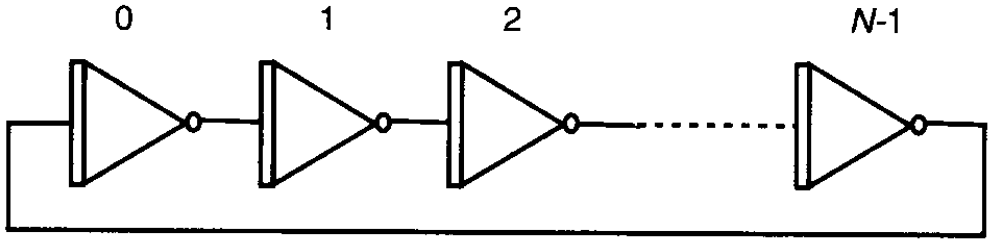
Detects changes in the input signal
produces a pulse to initialize subsequent circuitry
e.g., address transition detection in static memories

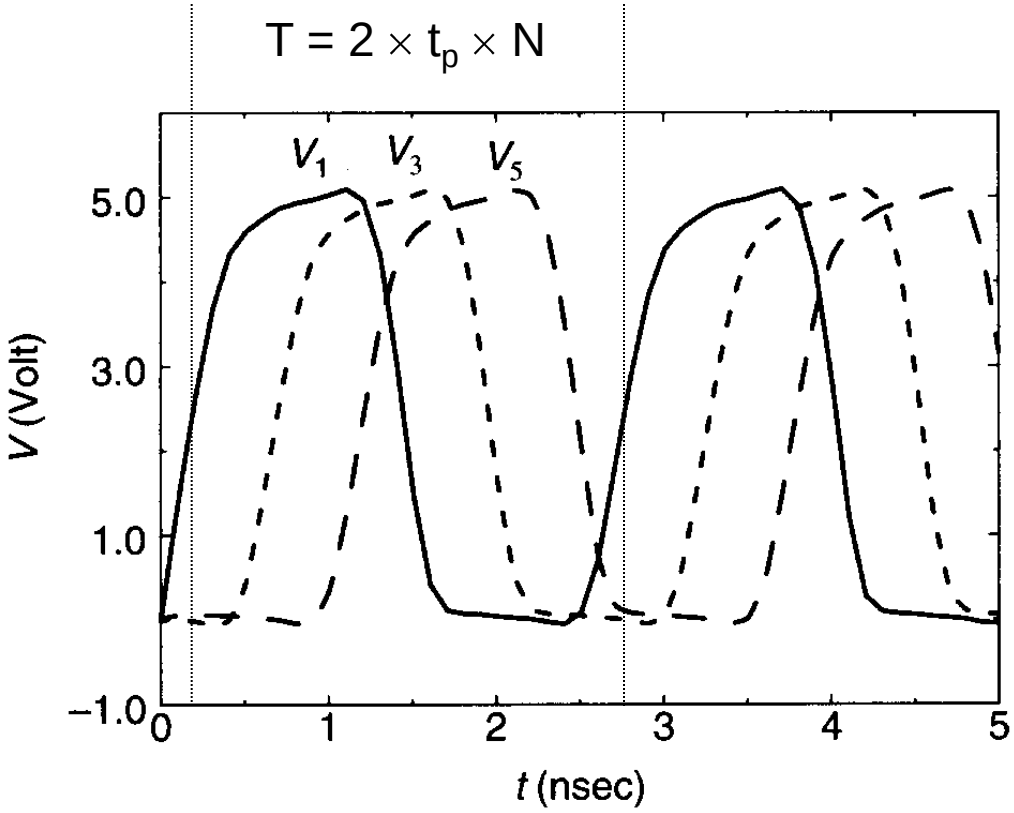
Monostable Trigger (RC-based)



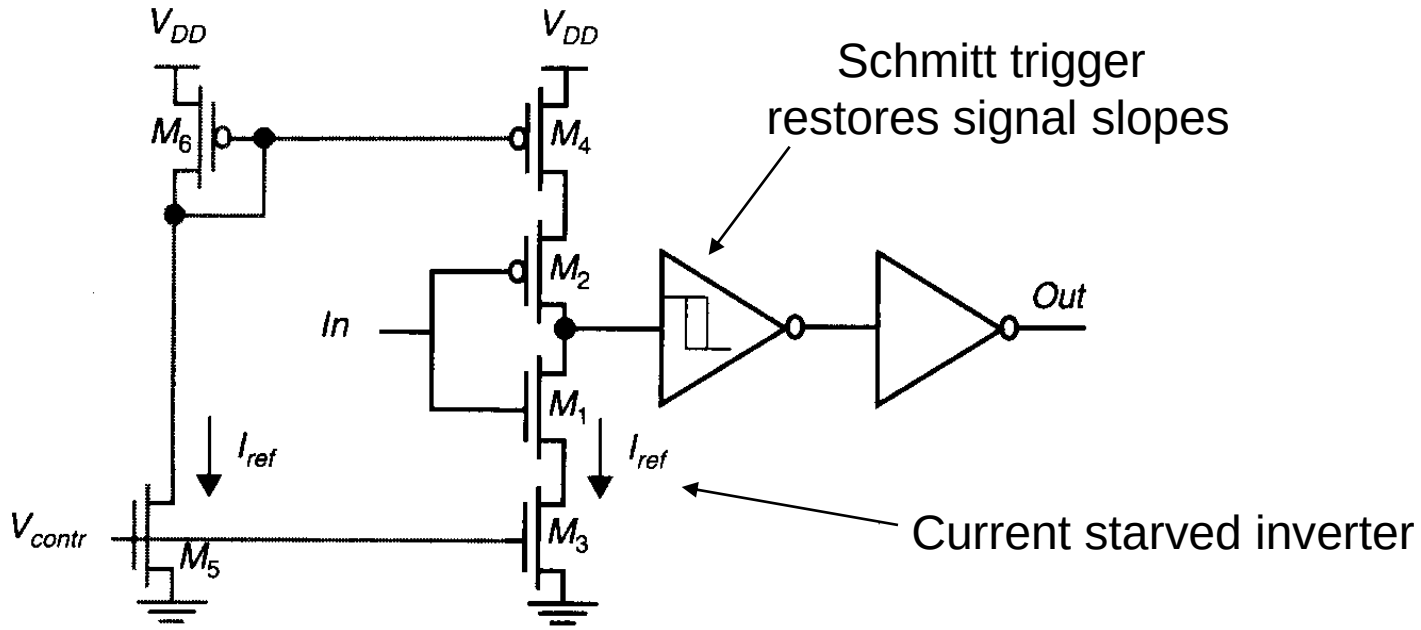


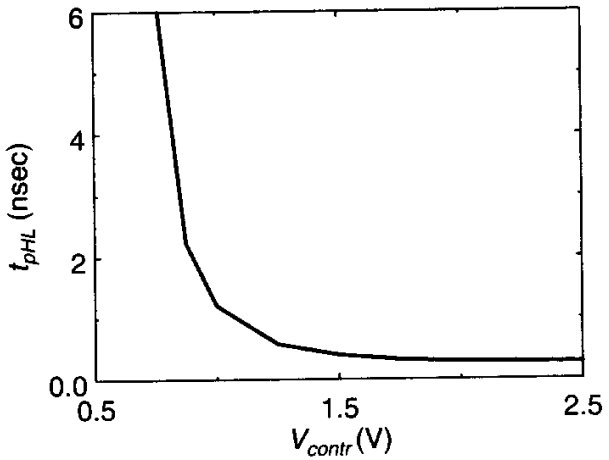
Astable Multivibrators (Oscillators)





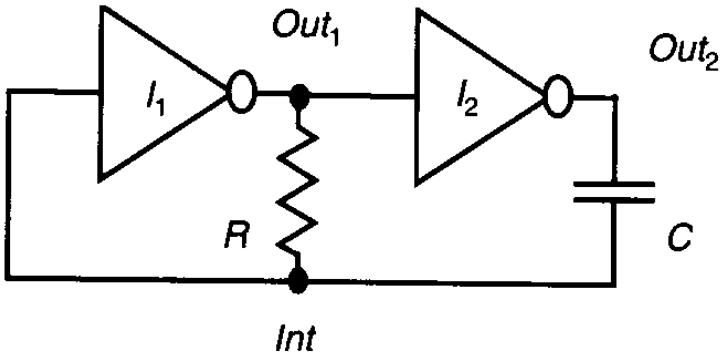
Voltage Controller Oscillator (VCO)

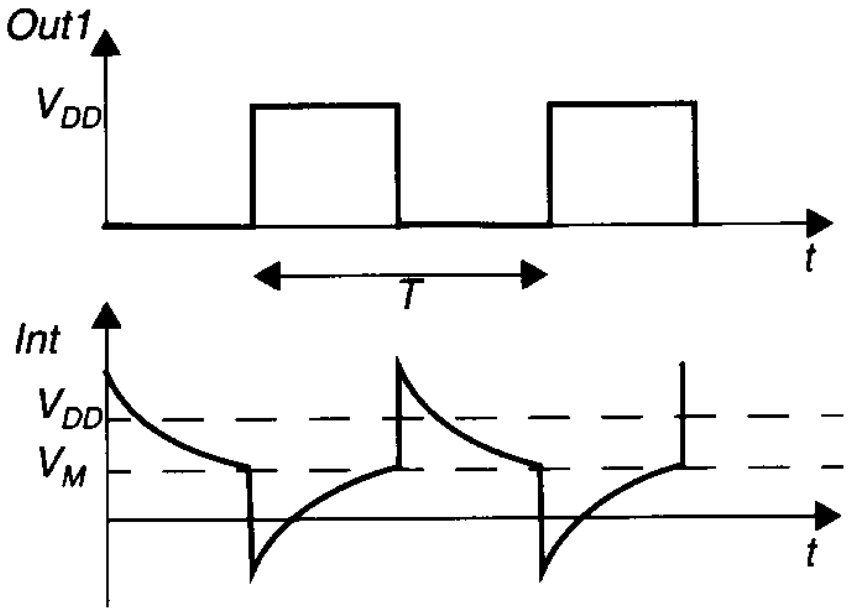




Decrease V_{contr} to reduce discharge current
⇒ increase propagation delay of inverter
⇒ decreases oscillating frequency
(quadratic dependency)

Relaxation Oscillator





$T = 2 \times (\ln 3) \times RC$