The Devices:
MOS Transistors

References:
Semiconductor Device Fundamentals,
R. F. Pierret, Addison-Wesley
Adapted from: Digital Integrated Circuits: A Design Perspective, J. Rabaey, Prentice Hall © UCB
MOS Transistor
(Metal-Oxide-Semiconductor)
NMOS Transistor

CROSS-SECTION of NMOS Transistor
Cross-Section of CMOS Technology
MOS transistors - types and symbols

- NMOS Enhancement
- NMOS Depletion
- PMOS Enhancement
- NMOS with Bulk Contact
Threshold Voltage: Concept

\[ V_T = V_{FB} + V_B + V_{ox} \]

\[ V_B = 2\phi_F \text{ Fermi potential} \]
Threshold Voltage: Concept

- **Threshold voltage due to ideal MOS structure**
  - Voltage to invert the character of the surface region from n-type to p-type and vice versa
  - Voltage drop due to gate oxide

- **Threshold voltage due to non-ideal MOS structure**
  - Difference in the work functions of metal and semiconductor
  - Charges in the gate oxide
  - Ion-implantation
  - Body effect
  - ...

Depletion Width and Electric Field

- Poisson’s equation
  \[
  \frac{dE}{dx} = \frac{\rho}{K_S \varepsilon_0} \approx -\frac{q N_A}{K_S \varepsilon_0}
  \]
  \(0 \leq x \leq W\)
  
  \(K_S\) : dielectric constant
  
  \(\varepsilon_0\) : permittivity of free space

- Electric Field
  \[
  E(x) = \frac{q N_A}{K_S \varepsilon_0} (W - x) \quad (0 \leq x \leq W)
  \]

- Depletion width
  \[
  \phi(x) = \frac{q N_A}{2 K_S \varepsilon_0} (W - x)^2 \quad (0 \leq x \leq W)
  \]
  
  \(\phi_S = \frac{q N_A}{2 K_S \varepsilon_0} W^2 \iff W = \left[ \frac{2 K_S \varepsilon_0}{q N_A} \phi_S \right]^{1/2}\)

  \[
  W_{\text{max}} = \left[ \frac{4 K_S \varepsilon_0}{q N_A} \phi_F \right]^{1/2}
  \]
  
  \(E_{S,\text{max}} = \left[ \frac{4 q N_A}{K_S \varepsilon_0} \phi_F \right]^{1/2}\)
Threshold Adjustment by Ion Implantation

- Implant a relatively small, precisely controlled number of either boron or phosphorus ions into the near-surface region of semiconductor.
- Implantation of boron causes a positive shift in threshold voltage.
- Implantation of phosphorus causes a negative shift.
- Like placing additional “fixed” charges.

\[
\Delta V = -\frac{Q_I}{C_{ox}} \quad Q_I = \pm qN_I
\]

(+): donor  (−): acceptor
Back Biasing or Body Effect

- $V_{SB}$ is normally positive for n-channel devices, negative for p-channel devices.
- Always increases the magnitude of the ideal device threshold voltage.
- Inversion occurs at $\phi_S = (2\phi_F + V_{SB})$.
- Increases the charges stored in depletion region:

$$Q_B = \sqrt{2qN_A \varepsilon_{si} (2\phi_F + V_{SB})}$$
Threshold voltage

\[ V_T = V_{FB} + V_B + V_{ox} \]

\[ V_T = \left( \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_I}{C_{ox}} \right) - 2\Phi_F - \frac{Q_B}{C_{ox}} \]
The Threshold Voltage

\[ V_T = \phi_{MS} + 2\phi_F + \frac{Q_B}{C_{ox}} - \frac{Q_I}{C_{ox}} - \frac{Q_M\gamma_M}{C_{ox}} - \frac{Q_F}{C_{ox}} - \frac{Q_{IT}(2\phi_F)}{C_{ox}} \]

- In general
  \[ V_{FB} = \phi_{MS} - \frac{Q_I}{C_{ox}} - \frac{Q_M\gamma_M}{C_{ox}} - \frac{Q_F}{C_{ox}} - \frac{Q_{IT}(0)}{C_{ox}} \]
  \[ V_T = V_{FB} + V_B + V_{ox} \]
  \[ V_B = 2\phi_F \]

- NMOS: \( V_{SB} > 0 \), PMOS: \( V_{SB} < 0 \)

\[ V_{ox} = \frac{K_s}{K_0} x_0 \sqrt{\frac{2qN_A}{K_S\varepsilon_0}} \left( 2\phi_F + V_{SB} \right) \text{ for NMOS} \]

\[ V_{ox} = -\frac{K_s}{K_0} x_0 \sqrt{\frac{2qN_D}{K_S\varepsilon_0}} \left( -2\phi_F - V_{SB} \right) \text{ for PMOS} \]
Current-Voltage Relations

At $x$, the gate to channel voltage equals $V_{GS} - V(x)$
Transistor in Linear Region

- Assume that the voltage exceeds $V_T$ all along the channel
- Induced charge/area at point $x$
  \[ Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T] \]
- Current
  \[ I_D = -v_n(x) Q_i(x) W \]
  
  $v_n(x)$: drift velocity
  \[ v_n = -\mu_n E(x) = \mu_n \frac{dV}{dx} \]

  \[ \therefore I_d \, dx = \mu_n C_{ox} W (V_{GS} - V - V_T) dV \]

- Integrating over the length of the channel $L$

  \[ I_D = K'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \]

  \[ K'_n = \mu_n C_{ox} = \mu_n \frac{C_{ox}}{T_{ox}} \]
Transistor In Saturation

\[ V_{DS} > V_{GS} - V_T \]
Transistor in Saturation

• If drain-source voltage increases, the assumption that the channel voltage is larger than $V_T$ all along the channel ceases to hold.

• When $V_{GS} - V(x) < V_T$ pinch-off occurs

• Pinch-off condition

$$V_{GS} - V_{DS} \leq V_T$$
Saturation Current

- The voltage difference over the induced channel (from pinch-off to the source) remains fixed at $V_{GS} - V_T$ and hence, the current remains constant.

- Replacing $V_{DS}$ by $V_{GS} - V_T$ in equation for $I_D$ yields

\[
I_D = \frac{K'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2
\]

- Effective length of the conductive channel is modulated by applied $V_{DS}$ - Channel Length Modulation
Current-Voltage Relations

Cut-off: $V_{GS} \leq V_T$, $I_{DS} \approx 0$

Linear Region: $V_{DS} < V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} \quad \text{Process Transconductance Parameter}$$

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

$$I_D = \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad \text{Channel Length Modulation}$$
I-V Relations

Linear: \( V_{DS} < V_{GS} - V_T \)

(a) \( I_D \) as a function of \( V_{DS} \)

(b) \( \sqrt{I_D} \) as a function of \( V_{GS} \) (for \( V_{DS} = 5V \))

NMOS Enhancement Transistor: \( W = 100 \mu m, L = 20 \mu m \)
Dynamic Behavior of MOS Transistor

Source of Cap. - Basic MOS structure
- channel charge
- depletion region of resource bias p-n junctions
The Gate Capacitance

(a) Top view

(b) Cross-section

\[ C_{\text{gate}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} WL \]

Can be decomposed into a number of elements each with a different behavior
Parasitic capacitance between gate and source (drain) called **Overlap Capacitance** (linear)

\[ C_{gsO} = C_{gdO} = C_{ox}x_d \cdot W = C_o \cdot W \]

**Channel Capacitance:** \( C_{gs}, C_{gd}, \) and \( C_{gb} \)

**Cut-Off:** no channel, total capacitance = \( C_{ox}WL_{eff} \)

appears between gate and bulk

**Triode Region:** Inversion layer - acts as conductor \( \therefore C_{gb} = 0 \)

Symmetry dictates \( C_{gs} \approx C_{gd} \approx \frac{C_{ox}WL_{eff}}{2} \)

**Saturation:** Pinch off, \( \therefore C_{gd} \approx 0, C_{gb} = 0 \)

\( C_{gs} \) averages \((2/3)C_{ox}WL_{eff}\)
Diffusion Capacitance (Junction Capacitance)

Reverse biased source-bulk and drain-bulk pn junctions
- **Bottom plate**

\[ C_{\text{bottom}} = C_j W L_s , \]

- **Side-wall junctions**  
  - formed by source \((N_D)\) and \(P^+\) channel stop \((N_A^+)\)
  - graded junction \((m=1/3)\)

\[
C_{sw} = C'_{jsw} x_j (w + 2L_s) \\
= C_{jsw} (W + 2L_s) \\
C_{jsw} = C'_{jsw} x_j , \quad x_j = \text{junction depth}
\]

- **\(C_{\text{diff}}\)**  
  
  \[
  C_{\text{diff}} = C_{\text{bottom}} + C_{sw} \\
  = C_j \times \text{Area} + C_{jsw} \times \text{Perimeter} \\
  = C_i L_s W + C_{isw} (2L_s + W)
  \]
Junction Capacitance

\[
C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}
\]
The Sub-Micron MOS Transistor

- Threshold Variations (Manufacturing tech., $V_{SB}$)
- Parasitic Resistances
- Velocity Saturation and Mobility Degradation
- Subthreshold Conduction
- Latchup
Threshold Variations

• In derivation of $V_T$ the following assumption were made:
  – charge beneath gate originates from MOS field effects
  – ignores depletion region the source and drain junctions (reverse biased)

• A part of the region below the gate is already depleted (by source & drain fields), a smaller $V_T$ suffices to cause strong inversion

• $V_T$ decreases with $L$

• Similar effect can be obtained by increasing $V_{DS}$ or $V_{DB}$ as it increases drain-junction depletion region
• $V_T$ can also drift over time (Hot-carrier effect)
  – Decreased device dimensions
  – Increase in electrical field
  – Increasing velocity of electrons, can leave Si surface and enter gate oxide
    – Electrons trapped in gate oxide change $V_T$ (increases in NMOS, decreases in PMOS)
• For a electron to be hot, electric field of $10^4$ V/cm is necessary
  – Condition easily met for sub-micron devices
Parasitic Resistances

\[ R_S = \frac{L}{W} R_{\text{[l]}} + R_C \]

Solutions: cover the diffusion regions with low-resistivity material such as titanium or tungsten, or make the transistor wider.
Velocity Saturation (1) short channel devices

(a) Velocity saturation

\[ v_{sat} = 10^7 \text{ cm/sec} \]

Constant mobility (slope = \( \mu \))

\[ E_{sat} = 1.5 \]

\[ E (\text{V/\mu m}) \]

(b) Mobility degradation

\[ \mu_n (\text{cm}^2/\text{V}s) \]

\[ \mu_{n0} \]

250

700

0

1

\[ E_t (\text{V/\mu m}) \]
Velocity Saturation (2)

\[ I_{DSAT} = v_{SAT} C_{ox} W (V_{GS} - V_{DSAT} - V_T) \]

Linear Dependence on \( V_{GS} \)

independent on \( L \) → current drive cannot be improved by decreasing \( L \)
Sub-threshold Conduction

\[ I_D = K \cdot e^{(V_{gs} - V_t)q / nkT} \left( 1 - e^{V_{ds}q / kT} \right) \]

SOI has better sub-threshold leakage

(Inverse) Rate of decrease of current:

\[ \left( \frac{d}{dV_{gs}} \ln(I_D) \right)^{-1} = \frac{KT}{q} \ln \left( 1 + \alpha \right) \]

60mV/decade At T = 300°K
Latchup

(a) Origin of latchup

(b) Equivalent circuit
Latchup

- Parasitic circuit effect
- Shorting of $V_{DD}$ and $V_{SS}$ lines resulting in chip self-destruction or system failure with requirements to power down
- To understand latchup consider: Silicon Controlled Rectifiers (SCRs)

![SCRs Diagram]

Anode A $p$ $n$ $p$ $n$ Cathode C

Gate G

$I_a$ $I_b1$ $I_c1$ $I_c2$

$I_g$ $I_b2$ $I_c$
Latchup - cont.

If \( I_g \) \( \uparrow \) \( \Rightarrow \) \( I_{c2} \) \( \uparrow \)

\( I_{c2} \) is the base current \( I_{b1} \) of the p-n-p transistor

\[ \therefore \quad I_g \uparrow \Rightarrow I_{b1} \uparrow \Rightarrow I_{c1} \uparrow \Rightarrow I_{b2} \uparrow \]  
(magnitude of current increases)

If the gain of the transistor are \( \beta_1 \) and \( \beta_2 \)

Then if \( \beta_1 \beta_2 \geq 1 \), the feedback action will turn device ON permanently and current will self destruct device.
Latchup Triggering

- Parasitic n-p-n & pin-p has to be triggered and holding state to be maintained
- Can be triggered by transient currents
  - Voltages during power-up
  - Radiation pulses
  - Voltages or current beyond operating range

\[
I_{\text{trigger}} \approx \frac{V_{\text{pnp-on}}}{\alpha_{\text{n-pn}} \cdot R_{\text{well}}}
\]

\[\alpha_{\text{n-pn}}: \text{Common base gain of n-p-n transistor}\]

Similarly, vertical triggering due to the voltage drop across \(R_{\text{substrate}}\) as current is injected into the emitter
Latchup Triggering - cont.

• Triggering occurs due to (mainly) I/O circuits where internal voltages meet external world and large currents can flow
  – When NMOS experiences undershoot by more than 0.7V, the drain is forward biased, which initiates latchup
  – When PMOS experiences overshoot by more than 0.7V, the drain is forward biased, which initiates latchup
Latchup Prevention

Analysis of the circuit shows that for latchup to occur the following inequality has to be true

\[ \beta_{npn} \beta_{pnp} > 1 + \frac{(\beta_{npn} + 1)(I_{R_{sub}} + I_{R_{well}} \cdot \beta_{pnp})}{I_{DD} - I_{R_{sub}}} \]

where

\[ I_{R_{sub}} = \frac{V_{benpn}}{R_{sub}} \]

\[ I_{R_{well}} = \frac{V_{bepnp}}{R_{well}} \]

\[ I_{DD} = \text{total supply current} \]

The feedback current flowing into n-p-n base is collector current offset by \( I_{R_{sub}} \). To cause the feedback, this current must be greater than initial n-p-n base current, \( I_b \).
Prevention of latchup

- Reduce the resistor values (substrate & well) and reduce the gain of parasitic transistors
- Latchup resistant CMOS process
- Layout techniques
Process option
- that reduces gain of parasitic transistors

• Si starting material with a thin epitaxial layer on highly doped Substrate
  – decreases substrate resistance
  – provide a sink for collector current of vertical p-n-p transistor
• as epi layer is thinned latch-up improves
• retrograde well structure
  – highly doped area at the bottom of the well
  – top lightly doped
  – reduces well-resistance deep in the well without deteriorating performance of transistors
How about $\beta_{\text{nnp}}$ or $\beta_{\text{pnp}}$?

- Hard to reduce
- For 1 $\mu$ n-well process

$$\beta_{\text{pnp}} \sim 10 - 100$$

$$\beta_{\text{nnp}} \sim 2 - 5$$
Guard Ring

$V_{SS}$
- $p^+$ diff. in p-sub
- $n^+$ diff. in n-well

$V_{DD}$

\{ to collect injected minority carriers \}
I/O Latchup Prevention

- Reduce $\beta$
  - use guard rings act as dummy collect minority currents and prevent minority carriers from being injected into respected bases
  - area expensive
  - only used in special space-borne applications where radiation is important
  - mainly used in I/O circuits only

- I/O Rules
  - separate (physically) n and p transistors
  - p+ guard rings connected to $V_{ss}$ around n-transistors
  - n+ guard rings connected to $V_{DD}$ around p-transistors
Latchup Prevention Techniques

• Every well must have a substrate contact of the appropriate type
• Substrate contact directly to metal to Supply pad (no diffusion or poly underpasses in the supply rails)
• Substrate contact as close to Source reduces $R_{\text{well}}$ and $R_{\text{sub}}$
  – Conservative rule: one supply contact for every supply connection
  – Less conservative: a substrate contact for every 5-10 transistors or every 25 to 100
• Layout n-transistors with packing of n-devices towards $V_{\text{ss}}$ & similarly for p-devices ($V_{\text{DD}}$)
  – avoid convoluted structures that intertwine n- and p-devices
Spice Models

- Level 1: Long Channel Equations - Very Simple
- Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations
- Level 3: Semi-Emperical - Based on curve fitting to measured devices
- Level 4 (BSIM): Emperical-Simple and Popular
# Main MOS Spice Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICE Model Index</td>
<td>LEVEL</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Zero-Bias Threshold Voltage</td>
<td>VT0</td>
<td>VT0</td>
<td>V</td>
<td>0</td>
</tr>
<tr>
<td>Process Transconductance</td>
<td>k'</td>
<td>KP</td>
<td>A/V2</td>
<td>2.E-5</td>
</tr>
<tr>
<td>Body-Bias Parameter</td>
<td>e</td>
<td>GAMMA</td>
<td>V0.5</td>
<td>0</td>
</tr>
<tr>
<td>Channel Modulation</td>
<td>l</td>
<td>LAMBDA</td>
<td>I/V</td>
<td>0</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>tox</td>
<td>TOX</td>
<td>m</td>
<td>1.0E-7</td>
</tr>
<tr>
<td>Lateral Diffusion</td>
<td>xd</td>
<td>LD</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Metallurgical Junction Depth</td>
<td>xj</td>
<td>XJ</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Surface Inversion Potential</td>
<td>2</td>
<td>F</td>
<td></td>
<td>PHI</td>
</tr>
<tr>
<td>Substrate Doping</td>
<td>NA, ND</td>
<td>NSUB</td>
<td>cm-3</td>
<td>0</td>
</tr>
<tr>
<td>Surface State Density</td>
<td>Qss/q</td>
<td>NSS</td>
<td>cm-3</td>
<td>0</td>
</tr>
<tr>
<td>Fast Surface State Density</td>
<td>NFS</td>
<td></td>
<td>cm-3</td>
<td>0</td>
</tr>
<tr>
<td>Total Channel Charge Coefficient</td>
<td>NEFF</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Type of Gate Material</td>
<td>TPG</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Surface Mobility</td>
<td>m0</td>
<td>U0</td>
<td>cm2/V·sec</td>
<td>600</td>
</tr>
<tr>
<td>Maximum Drift Velocity</td>
<td>vmax</td>
<td>VMAX</td>
<td>m/s</td>
<td>0</td>
</tr>
<tr>
<td>Mobility Critical Field</td>
<td>xcrit</td>
<td>UCRIT</td>
<td>V/cm</td>
<td>1.0E4</td>
</tr>
<tr>
<td>Critical Field Exponent in Mobility Degradation</td>
<td>UEXP</td>
<td>-</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Transverse Field Exponent (mobility)</td>
<td>UTRA</td>
<td>-</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
## SPICE Parameters for Parasitics

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source resistance</td>
<td>$R_S$</td>
<td>RS</td>
<td>$\Omega$</td>
<td>0</td>
</tr>
<tr>
<td>Drain resistance</td>
<td>$R_D$</td>
<td>RD</td>
<td>$\Omega$</td>
<td>0</td>
</tr>
<tr>
<td>Sheet resistance (Source/Drain)</td>
<td>$R_o$</td>
<td>RSH</td>
<td>$\Omega_o$</td>
<td>0</td>
</tr>
<tr>
<td>Zero Bias Bulk Junction Cap</td>
<td>$C_{j0}$</td>
<td>CJ</td>
<td>F/m$^2$</td>
<td>0</td>
</tr>
<tr>
<td>Bulk Junction Grading Coeff.</td>
<td>$m$</td>
<td>MJ</td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Zero Bias Side Wall Junction Cap</td>
<td>$C_{jsw0}$</td>
<td>CJSW</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Side Wall Grading Coeff.</td>
<td>$m_{sw}$</td>
<td>MJSW</td>
<td>-</td>
<td>0.3</td>
</tr>
<tr>
<td>Gate-Bulk Overlap Capacitance</td>
<td>$C_{gbo}$</td>
<td>CGBO</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Gate-Source Overlap Capacitance</td>
<td>$C_{gs0}$</td>
<td>CGSO</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Gate-Drain Overlap Capacitance</td>
<td>$C_{gdo}$</td>
<td>CGDO</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Bulk Junction Leakage Current</td>
<td>$I_S$</td>
<td>IS</td>
<td>A</td>
<td>0</td>
</tr>
<tr>
<td>Bulk Junction Leakage Current Density</td>
<td>$J_S$</td>
<td>JS</td>
<td>A/m$^2$</td>
<td>1E-8</td>
</tr>
<tr>
<td>Bulk Junction Potential</td>
<td>$\phi_0$</td>
<td>PB</td>
<td>V</td>
<td>0.8</td>
</tr>
<tr>
<td>Parameter Name</td>
<td>Symbol</td>
<td>SPICE Name</td>
<td>Units</td>
<td>Default Value</td>
</tr>
<tr>
<td>----------------------------</td>
<td>--------</td>
<td>------------</td>
<td>-------</td>
<td>---------------</td>
</tr>
<tr>
<td>Drawn Length</td>
<td>L</td>
<td>L</td>
<td>m</td>
<td>-</td>
</tr>
<tr>
<td>Effective Width</td>
<td>W</td>
<td>W</td>
<td>m</td>
<td>-</td>
</tr>
<tr>
<td>Source Area</td>
<td>AREA</td>
<td>AS</td>
<td>m²</td>
<td>0</td>
</tr>
<tr>
<td>Drain Area</td>
<td>AREA</td>
<td>AD</td>
<td>m²</td>
<td>0</td>
</tr>
<tr>
<td>Source Perimeter</td>
<td>PERIM</td>
<td>PS</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Drain Perimeter</td>
<td>PERIM</td>
<td>PD</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Squares of Source Diffusion</td>
<td>NRS</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Squares of Drain Diffusion</td>
<td>NRD</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
Matching Manual and SPICE Models

Region of Matching

$V_{GS} = 5V$

$V_{DS} = 5V$

Short Channel I-V Curve

Long Channel Approximation

$I_D$ vs $V_{DS}$
# Technology Evolution

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length (μm)</td>
<td>0.4</td>
<td>0.3</td>
<td>0.25</td>
<td>0.18</td>
<td>0.13</td>
<td>0.1</td>
</tr>
<tr>
<td>Gate oxide (nm)</td>
<td>12</td>
<td>7</td>
<td>6</td>
<td>4.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
<td>3.3</td>
<td>2.2</td>
<td>2.2</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_T$ (V)</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>NMOS $I_{Dsat}$ (mA/μm) (@ $V_{GS} = V_{DD}$)</td>
<td>0.35</td>
<td>0.27</td>
<td>0.31</td>
<td>0.21</td>
<td>0.29</td>
<td>0.33</td>
</tr>
<tr>
<td>PMOS $I_{Dsat}$ (mA/μm) (@ $V_{GS} = V_{DD}$)</td>
<td>0.16</td>
<td>0.11</td>
<td>0.14</td>
<td>0.09</td>
<td>0.13</td>
<td>0.16</td>
</tr>
</tbody>
</table>