Combinational Logic Gates in CMOS

References:
Adapted from: *Digital Integrated Circuits: A Design Perspective*, J. Rabaey, Prentice Hall © UCB

*Principles of CMOS VLSI Design: A Systems Perspective*, N. H. E. Weste, K. Eshraghian, Addison Wesley

Adapted from: EE216A Lecture Notes by Prof. K. Bult © UCLA
Ratioed Logic

Reduce the number of devices over complementary logic
Ratioed Logic

- Use PDN to implement the function (which is the negation of the network)
- Total number of devices: $n$ for the input, 1 for the static load
- Minimum load is 1 unit-gate load
- Functional sizing is required to optimize noise margin
Trade-offs to be Considered

- To reduce static power, $I_{\text{Load}}$ should be low.
- To obtain a reasonable $\text{NM}_L$, $V_{OL} = I_{\text{Load}}R_{\text{PDN}}$ should be low.
- To reduce $t_{\text{PLH}} \approx C_L V_{DD}/(2I_{\text{Load}})$, $I_{\text{Load}}$ should be high.
- To reduce $t_{\text{PHL}} \approx 0.69 R_{\text{PDN}} C_L$, $R_{\text{PDN}}$ should be kept small.
Improving DC and AC Characteristics

- Bias circuit to force VOL below threshold
- Build better load to improve VOL and switching time
- Use differential logic to eliminate static current
Forcing the Voltage Output Low

Bias Circuit
Adaptive Load

$V_{DD}$

$M_1$  $M_2$

$M_1 \gg M_2$

$A$  $B$  $C$  $D$

$F$  $C_L$
Improved Loads

(a) Basic principle

Differential Cascade Voltage Switch Logic (DCVSL)
Example

(b) XOR-NXOR gate
Pass Transistor Logic
Pass-Transistor Logic

- Reduced number of transistors
- No static power consumption
Pass Transistor Logic

\[ F = \begin{cases} 
Z & \text{if } P = 0 \\
V & \text{if } P = 1
\end{cases} \]
Basic Pass Transistor Logic Model

Control Signals

F = Sum of Products

$$F = P_1(V_1) + P_2(V_2) + \cdots + P_n(V_n)$$
XNOR Gate

Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>OUT</th>
<th>Pass Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>-A + -B</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>A + -B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-A + B</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>A + B</td>
</tr>
</tbody>
</table>

Modified Karnaugh Map
Boolean Function Unit

<table>
<thead>
<tr>
<th>Operation</th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
<th>P4</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND(A,B)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>XOR(A,B)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>OR(A,B)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>NOR(A,B)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>NAND(A,B)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Problem: $V_B$ does not pull up to $V_{DD}$, only to $V_{DD} - V_{tn(body-effect)}$

Cannot completely turn off the PMOS transistor
Causes static power consumption
Solution 1: Transmission Gate

(a) Circuit

\[ A = 5 \text{ V} \quad \overline{C} = 0 \text{ V} \quad C = 5 \text{ V} \]

\[ B \quad C_L \]
Transmission Gate Implementation
Transmission Gate XNOR

\[ \text{OUT} \rightarrow \begin{array}{c}
-A \\
\text{B} \\
\text{A}
\end{array} \]

\[ \begin{array}{c}
\text{B} \\
\text{-B} \\
\text{A}
\end{array} \]
Transmission Gate (Inverting) Multiplexer
Resistance of Transmission Gate

B is discharged originally

For NMOS, $V_{GS} = V_{DS}$, saturated or cutoff

For PMOS, $V_{GS} = -V_{DD}$, $V_{DS}$ increases from $-V_{DD}$ to 0, starts out in saturation, then transitions into non-saturation

$V_{out} < |V_{tp}| : \text{ NMOS saturated, PMOS saturated}$

$|V_{tp}| < V_{out} < V_{DD} - V_{tn} :$

NMOS saturated, PMOS linear

$V_{DD} - V_{tn} < V_{out} :$

NMOS cutoff, PMOS linear
Resistance of Transmission Gate

The graph shows the variation of resistances $R_{n}$, $R_{p}$, and $R_{eq}$ with output voltage $V_{out}$.

- $R_{n}$ is represented by a dashed line that increases with $V_{out}$.
- $R_{p}$ is represented by a dashed line that decreases with $V_{out}$.
- $R_{eq}$ is represented by a solid line that remains relatively constant with $V_{out}$.

The circuit diagram on the right illustrates the setup with 5 V and 0 V applied to the terminals, and $V_{out}$ as the output.
Approximations

• Assume both in linear region, ignore body effect

\[
G_{eq} = \frac{1}{R_{eq}} = \frac{\beta_n (V_{DD} - V_B - V_m)(V_A - V_B)}{(V_A - V_B)} + \frac{\beta_p (V_{DD} + V_{tp})(V_A - V_B)}{(V_A - V_B)}
\approx \beta_n (V_{DD} - V_m) + \beta_p (V_{DD} + V_{tp})
\]

• Assume both in saturated region

\[
G_{eq} = \frac{I_n + I_p}{V_{DD}} = \frac{\beta_n (V_{DD} - V_m)^2 + \beta_p (V_{DD} + V_{tp})^2}{2V_{DD}}
\]
When Output Closely follows Input

Region A: NMOS unsaturated, PMOS off

Region B: NMOS unsaturated, PMOS unsaturated

Region C: NMOS off, PMOS unsaturated
Delay in Transmission Gate Networks

Distributed RC network
Elmore Delay

To solve for actual delay

\[ \frac{dV_i(t)}{dt} = \frac{1}{R_{eq} C} \left[ V_{i+1}(t) + V_{i-1}(t) - 2V_i(t) \right] \]

Estimate the dominant time constant:
assume all internal nodes are pre-charged to VDD, and a step input is applied

\[ \tau_N = \sum_{k=1}^{N} C \sum_{j=k}^{N} R_{eq} = \sum_{k=1}^{N} R_{eq} \sum_{j=k}^{N} C = \frac{n(n + 1)}{2} R_{eq} C \]
Delay Optimization by Buffer Insertion

- Delay of RC chain
  \[ t_p = 0.69 \tau_N = 0.69 \frac{n(n + 1)}{2} R_{eq} C \]

- Delay of buffered chain
  \[
  t_p = 0.69 \left[ \frac{n}{m} \frac{m(m + 1)}{2} R_{eq} C \right] + \left( \frac{n}{m} - 1 \right) t_{pbfs}
  \]
  \[
  = 0.69 \left[ \frac{n(m+1)}{2} R_{eq} C \right] + \left( \frac{n}{m} - 1 \right) t_{pbfs}
  \]

- \( m_{opt} = 1.7 \sqrt{\frac{t_{pbfs}}{R_{eq} C}} \)
Transmission Gate Full Adder
### Adder Truth Table

<table>
<thead>
<tr>
<th>C</th>
<th>A</th>
<th>B</th>
<th>A.B(G)</th>
<th>A+B</th>
<th>A⊕B(P)</th>
<th>SUM</th>
<th>CARRY</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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<td>1</td>
</tr>
</tbody>
</table>

**SUM =** A ⊕ B ⊕ C  
**CARRY =** C if A ⊕ B = 1  
**CARRY =** A (or B) if A ⊕ B = 0
Solution 2:
Level Restoring Transistor for NMOS Only Logic

- Full Swing
- Disadvantage: More complex, larger capacitance
Level Restoring Transistor

(a) Output node

(b) Intermediate node X
Proper Sizing of Level Restoring Transistor

- In transient, conducting path from $M_r$ to $M_3$ via $M_n$ when $A$ is low, $B$ switches from low to high, and $X$ is high.

- $M_r$ must not be too large, otherwise, $X$ cannot be brought below threshold voltage, $V_{M_r}$ of inverter, $M_r$ cannot be turned off.
Sizing of a Level Restorer

\[ I = \beta_3 (V_{DD} - V_{tn})V_A \]
\[ = \frac{\beta^n}{2} (V_B - V_A - V_{tn})^2 \]
\[ = \beta_r \left[ (V_{DD} + V_{tp})(V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2} \right] \]
Sizing of a Level Restorer

\[ V_{DD} = 5V \]
\[ V_{tn} = -V_{tp} = 0.75V \]
\[ V_M = 2.5V \]
\[ I = \beta_r \left[ (V_{DD} + V_{tp})(V_{DD} - V_M) - \frac{(V_{DD} - V_M)^2}{2} \right] = 7.5 \beta_r \]
\[ I = \beta_3 (V_{DD} - V_{tn})V_A \]
\[ \Rightarrow V_A = 1.76 \frac{\beta_r}{\beta_n} \quad \text{if } M_3 \text{ and } M_n \text{ are of equal size} \]
\[ V_B \leq V_{DD} \]
\[ \Rightarrow V_B = 3.87 \sqrt{\frac{\beta_r}{\beta_n}} + 1.76 \frac{\beta_r}{\beta_n} + 0.75 \leq 5V \]
\[ m = \frac{\beta_n}{\beta_r} > 1.55 \]
Proper Sizes of Restorer

Making the NMOS pass-transistor and PMOS restorer the same size is reasonable.
Solution 3: Single Transistor Pass Gate with $V_T=0$

Watch out for leakage currents
Complimentary Pass Transistor Logic

(a)

(b)

AND/NAND

OR/NOR

EXOR/NEXOR

F = AB

F = A + B

F = A Æ

F = A ⊕ B Æ
Total number of transistors needed = 14 (including the final buffer)
But AND function is simultaneously present
\( t_{PHL} = 1.05\text{ns}, \ t_{PLH} = 0.45\text{ns} \)
Dynamic Logic
Dynamic Logic

2 phase operation:

• Precharge

• Evaluation
Example

- $N + 2$ transistors
- Ratioless
- No static power consumption
- Small Noise Margins ($NM_L$)
- Requires Clock
- Pull-down resistance increases due to the evaluation transistor
Transient Response

The graph illustrates the transient response of a system, showing the voltage output ($V_{out}$) over time ($t$) in nanoseconds (nsec). The response is divided into two phases: PRECHARGE and EVALUATION. The graph includes a vertical dashed line indicating a critical point at $t = 2.00 \times 10^{-9}$ nsec, which separates the two phases. The voltage levels are indicated as $0.00 \times 10^{0}$ to $6.00 \times 10^{-9}$ Volts.
Dynamic 4 Input NAND Gate

<table>
<thead>
<tr>
<th>Area</th>
<th>Static Current</th>
<th>Transistors</th>
<th>$V_{OH}$</th>
<th>$V_{OL}$</th>
<th>$V_M$</th>
<th>$NM_H$</th>
<th>$NM_L$</th>
<th>$t_{pHL}$</th>
<th>$t_{pLH}$</th>
<th>$t_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td>212 μm²</td>
<td>0 μA</td>
<td>6</td>
<td>5 V</td>
<td>0 V</td>
<td>0.75 V</td>
<td>4.25 V</td>
<td>0.75 V</td>
<td>0.74 nsec</td>
<td>0 nsec</td>
<td>0.37 nsec</td>
</tr>
</tbody>
</table>
Reliability Problems — Charge Leakage

(a) Leakage sources

(b) Effect on waveforms

Dynamic circuits require a minimal clock rate
Charge Sharing (redistribution)

\[ V_{DD} \]

\[ M_p \]

\[ M_a \]

\[ M_b \]

\[ M_e \]

\[ C_L \]

\[ C_a \]

\[ C_b \]

\[ \phi \]

\[ A \]

\[ B = 0 \]

\[ Out \]

\[ V_{out} \]

\[ V_{DD} \]

\[ V_{out}(t) \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{Tn} \]

\[ V_X \]

\[ \Delta V_{out} < V_{Tn} \]

\[ \Delta V_{out} = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L}(V_{DD} - V_{Tn}(V_X)) \]

\[ \Delta V_{out} > V_{Tn} \]

\[ \Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right) \]
Minimize Charge Sharing

• Keep the change in storage voltage below $|V_{tp}|$
  
  – the output might be connected to a static inverter as in Domino logic

\[
\frac{C_a}{C_L} < \frac{|V_{tp}|}{V_{DD} - V_m} = 0.2
\]

• $C_a$ is normally smaller than $C_L$, but if there is series connection of NMOS transistors, internal capacitances can be strung together and that can increase the voltage change
Charge Redistribution - Solutions

(a) Static bleeder

(b) Precharge of internal nodes
Clock Feedthrough

could potentially forward bias the diode

overshoot
Clock Feedthrough and Charge Sharing

output without redistribution ($M_a$ off)

internal node in PDN

$V$ (Volts)

t (nsec)
Cascading Dynamic Gates

Only 0→1 Transitions allowed at inputs!
Domino Logic

Static Inverter with Level Restorer
Domino Logic - Characteristics

- Only non-inverting logic
- Very fast - Only $1 \rightarrow 0$ transitions at input of inverter affects the next Domino
- Static inverter increases noise immunity, increase the size of PMOS to increase $V_M$
- Proper sizing of inverter to drive the fan-out in optimal way
- Add a level-restoring transistor to overcome charge sharing and charge loss
np-CMOS (Zipper CMOS)

Only 1→0 transitions allowed at inputs of PUN

Reduced noise margins: \( \text{NM}_H = |V_{tp}|, \text{NM}_L = |V_{tn}| \)
Full Adder Circuit
np CMOS Adder

Carry Path
Manchester Carry Chain Adder

V_{DD}

Total Area: 225 \, \mu m \times 48.6 \, \mu m
## Adder Truth Table

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<tbody>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\[
\text{SUM} = A \oplus B \oplus C = P \oplus C
\]

\[
\text{CARRY} = C \text{ if } P = 1
\]

\[
\text{CARRY} = AB \text{ if } P = 0
\]

\[
\text{CARRY} = G + PC
\]
## CMOS Circuit Styles - Summary

<table>
<thead>
<tr>
<th>Style</th>
<th>Ratioed</th>
<th>Static Power</th>
<th># transistors</th>
<th>Area ($\mu$m$^2$)</th>
<th>Propagation Delay (nsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complementary</td>
<td>No</td>
<td>No</td>
<td>8</td>
<td>533</td>
<td>0.61</td>
</tr>
<tr>
<td>Pseudo-NMOS</td>
<td>Yes</td>
<td>Yes</td>
<td>5</td>
<td>288</td>
<td>1.49</td>
</tr>
<tr>
<td>CPL</td>
<td>No</td>
<td>No</td>
<td>14</td>
<td>800</td>
<td>0.75</td>
</tr>
<tr>
<td>Dynamic (NP)</td>
<td>No</td>
<td>No</td>
<td>6</td>
<td>212</td>
<td>0.37</td>
</tr>
</tbody>
</table>

4-input NAND Gate