EE559: MOS VLSI Design

Instructors: K. Roy
Email: kaushik@ecn.purdue.edu
URL1: www.ece.purdue.edu/~kaushik
Office: MSEE 232
Telephone: 494-2361
Office Hours: Tuesday/Thursday 11am-12noon
or by appointments

Grading Policy

- Mid-terms + quizzes + hw will account for 75% of the grade
  - 3 mid-terms
  - Mandatory and has to be taken on the scheduled day of the exam.
- Project will account for 25% of the grade. Late projects will not be accepted.
- You are guaranteed an A if your weighted average score over exams, quizzes, and projects is 90 or above.
- Any form of cheating will be heavily penalized and reported to the Dean of students and may result in a failing grade.
- Instructor reserves right to change project requirements.

Text and References

- Text:
  - *Digital Integrated Circuits: A Design Perspective*, J. Rabaey, Prentice Hall, Second edition
- References:
  - *Principles of CMOS VLSI Design: A Systems Perspective*, 2nd Ed., N. H. E. Weste and K. Eshraghian, Addison Wesley
  - *Circuits, Interconnects, and Packaging for VLSI*, H. Bakoglu, Addison Wesley
- Class Notes:
  - http://www.ece.purdue.edu/~vlsi/ee559/20001

Conferences & Journals

- IEEE Transactions on VLSI Systems
- IEEE Transactions on CAD of IC's
- IEEE Journal of Solid State Circuits
- IEEE VLSI Circuits Symposium
- Journal of Electronic Testing
- ACM Design Automation Conference
- IEEE International Conference on CAD
- IEEE Solid State Circuits Conference
- International symposium on Low-Power Electronics & Design
- IEEE Conference on Computer Design
- IEEE International Test Conference

Course Outline

- Introduction: Historical perspective and Future Trend
- Semiconductor Devices
- CMOS Logic, Layout techniques
- MOS devices, SPICE models
- Inverters: transfer characteristics, static and dynamic behavior, power and energy consumption of static MOS inverters
- Designing combinational logic gates in CMOS
  - Static CMOS design: Complementary CMOS, ratioed logic, pass-transistor logic
  - Dynamic CMOS logic

Course Outline (Cont'd)

- Designing combinational logic gates (Cont'd)
  - Power consumption in CMOS gates
  - Low-power design
- Designing sequential circuits
- Interconnect and timing issues
- Designing memory and array structures
- Designing arithmetic building blocks
- VLSI testing and verification

VLSI CAD Lab and TA

- VLSI CAD Lab located in 360 Potter Engineering Center
  - SUN workstations running Mentor Graphics tools
  - Courtesy key for after-hour access can be obtained from front desk in Potter Engineering Library
  - Additional workstations in MSEE 186
- Lab TA: Kuntal Roy (royk@purdue.edu)
  - Facilitates the use of lab design tools.
  - Office hours: TBA
  - Lab Orientation will be held in the second week
- Lab URL
  - http://min.ecn.purdue.edu/~mgcdevel/ee559_lab.html

Course Project

- Complete design of a functional logic block or system
  - Complexity of 1000+ transistors or novelty
  - Design using the CADENCE tools and HSPICE
    - Design your own library from scratch
  - Functionality to be verified
  - Critical path timing should be verified using HSPICE
  - Project report due the last day of class
  - Project presentation by each group in the last week of class
  - Work in a group of 2 will be allowed in special cases
  - Start early!
  - Emphasis on new ideas, power dissipation, performance, reconfigurability, low voltage design

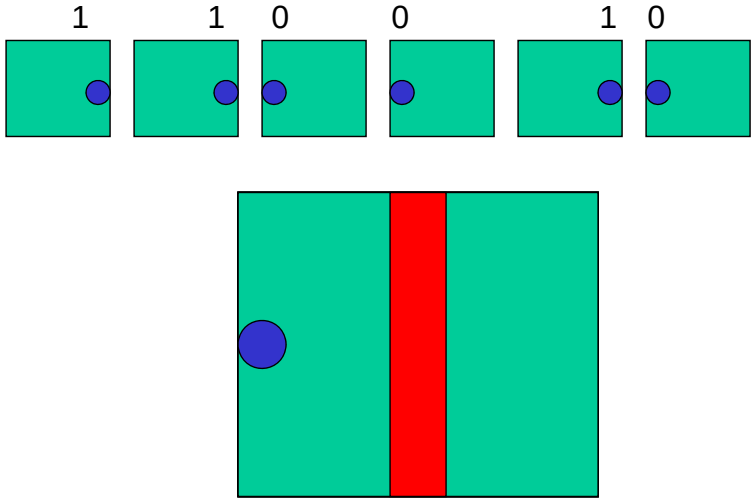
Introduction: A Historical Perspective and Future Trends

References:

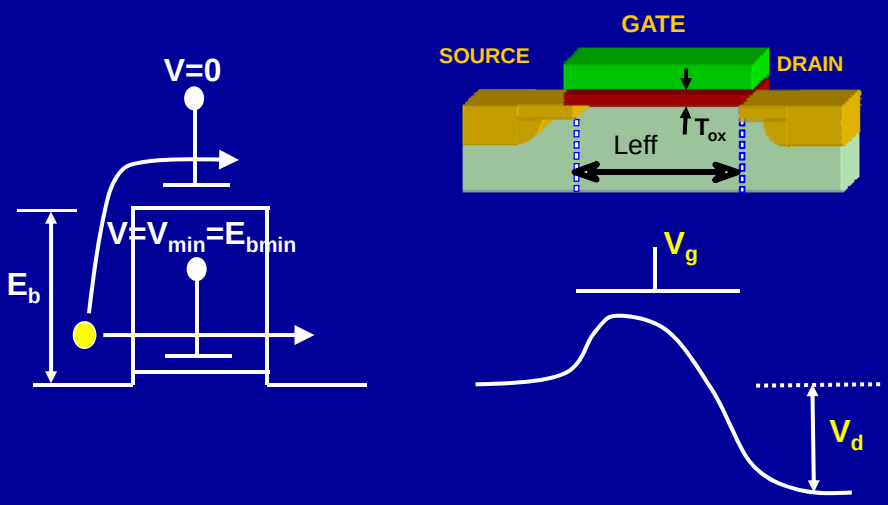
Adapted from: *Digital Integrated Circuits: A Design Perspective*, J. Rabaey © UCB

Principles of CMOS VLSI Design: A Systems Perspective, 2nd Ed., N. H. E. Weste and K. Eshraghian

Digital Computation: Particle Location is an Indicator of State



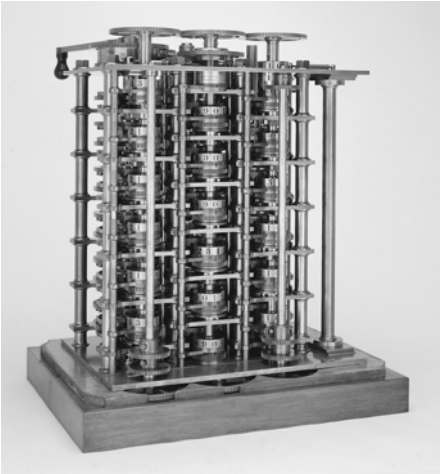
Physical Medium for Computation: Barrier Model



1. Can we operate with $V_{min} \sim K_B T \ln 2$?

2. Can we operate with $Q_{min} = q$?

The First Computer



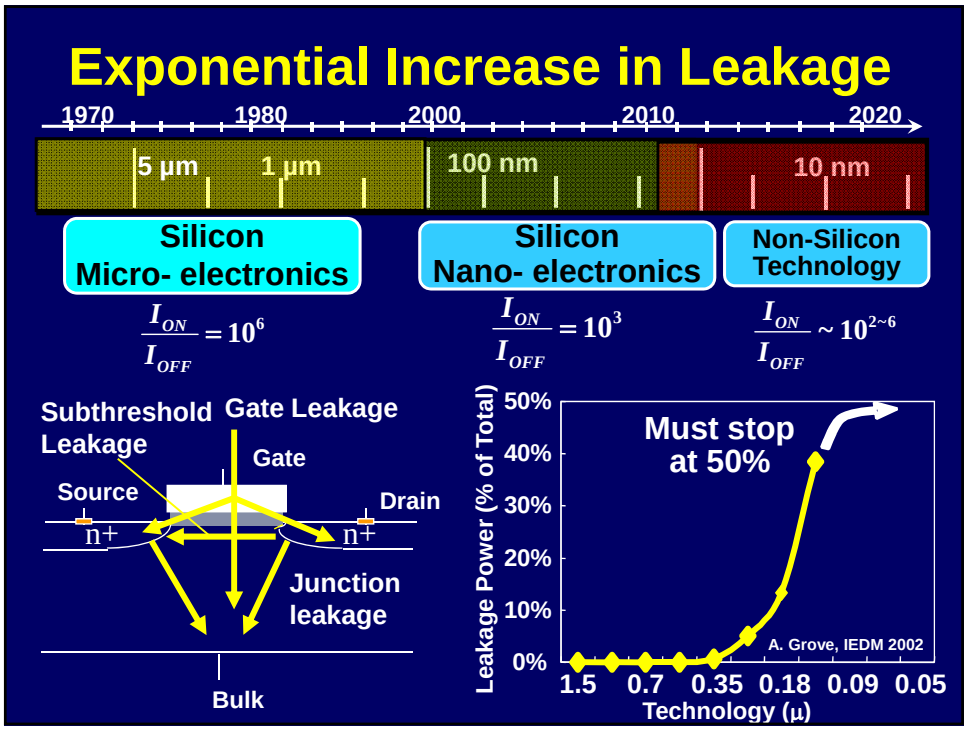
- The Babbage Differential Engine (1834)
- 25,000 mechanical parts
- Cost £17,470

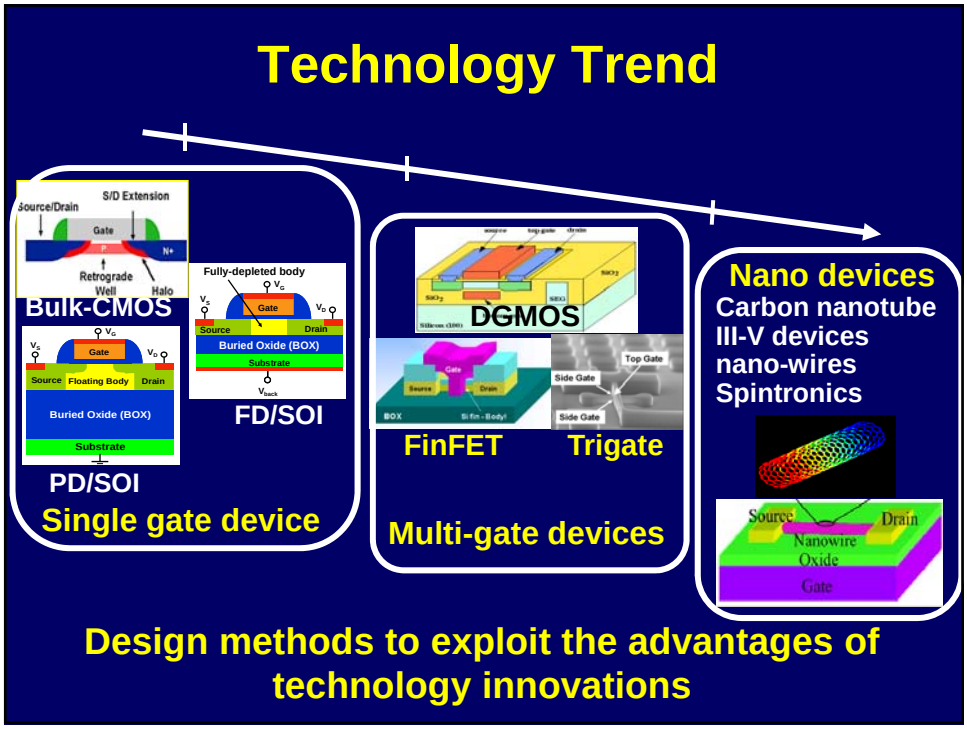
Digital Electronic Computing

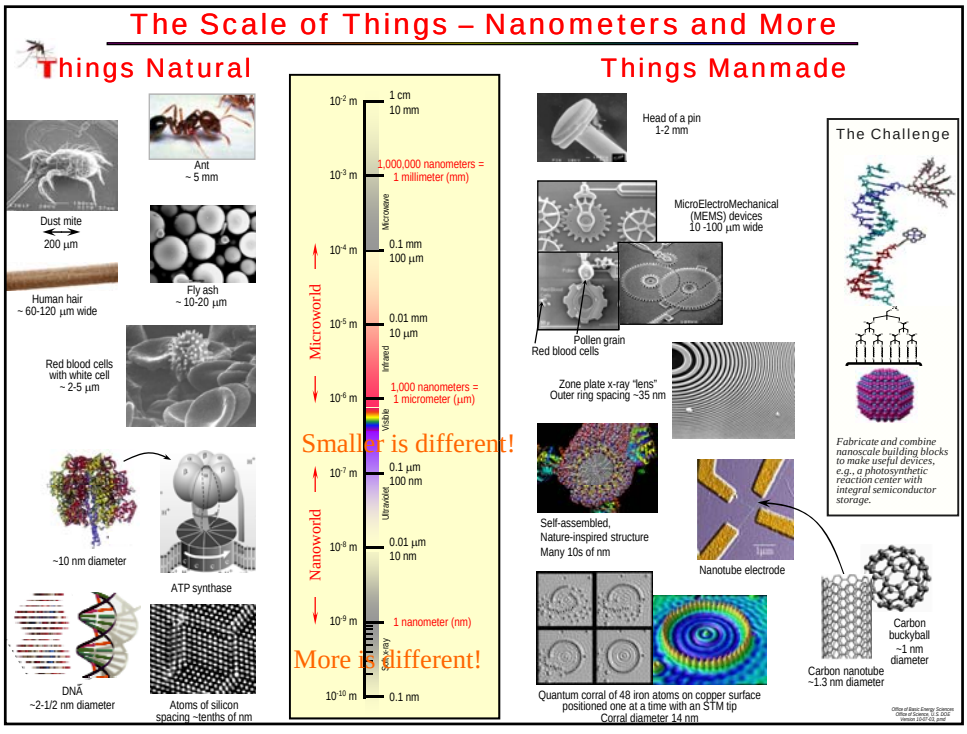
- Started with the introduction of vacuum tube
- ENIAC for computing artillery firing tables in 1946
- Integration density
  - 80 feet long, 8.5 feet high, and several feet wide
  - 18,000 vacuum tubes
- Reliability issues and excessive power consumption
- Did not go far until the invention of the transistor at Bell Lab in 1947

HISTORY

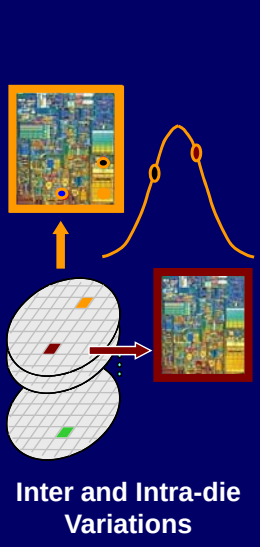
- MOS field-effect transistor: Lilienfeld (1925), Heil (1935)
- Bipolar transistors: Bardeen (1947), Schockley (1949)
- First Bipolar digital logic: Harris (1956)
  - IC Logic family:
    - Transistor-Transistor Logic (TTL) (1962)
    - Emitter-Coupled Logic (ECL) (1971)
    - Integrated Injection Logic (I^2L) (1972)
- PMOS and NMOS transistors on the same substrate: Weimer (1962), Wanlass (1965)
- PMOS-only logic until 1971 when NMOS technology emerged
- NMOS-only logic until late 1970s, when CMOS technology took over
- Later developments: BiCMOS, GaAs, low-temperator CMOS, super-conducting technologies, Nano-electronic



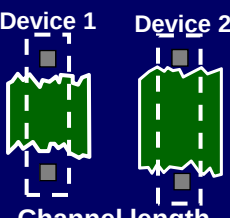

Technology Trend
S/D Extension
Source/Drain
Gate
Retrograde Well
Halo
Bulk-CMOS
Fully-depleted body
Gate
Source
Drain
Buried Oxide (BOX)
Substrate
FD/SOI
Floating Body
PD/SOI
Single gate device
DGMOS
FinFET
Trigate
Top Gate
Side Gate
Multi-gate devices
Nano devices
Carbon nanotube
III-V devices
nano-wires
Spintronics
Nanowire
Oxide
Design methods to exploit the advantages of technology innovations

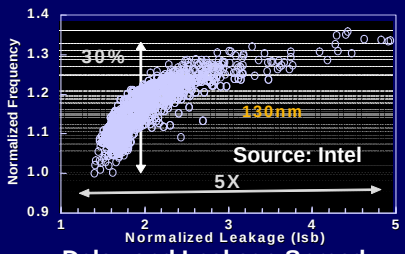

The Scale of Things – Nanometers and More
Things Natural
Things Manmade
Dust mite
200 µm
Ant
~ 5 mm
Human hair
~ 60-120 µm wide
Fly ash
~ 10-20 µm
Red blood cells with white cell
~ 2-5 µm
~10 nm diameter
ATP synthase
DNA
~2-1/2 nm diameter
Atoms of silicon
spacing ~tenths of nm
1 cm
10 mm
1,000,000 nanometers = 1 millimeter (mm)
0.1 mm
100 µm
0.01 mm
10 µm
1,000 nanometers = 1 micrometer (µm)
0.1 µm
100 nm
0.01 µm
10 nm
1 nanometer (nm)
0.1 nm
Microworld
Nanoworld
Microwave
Infrared
Visible
Ultraviolet
Soft X-ray
Smaller is different!
More is different!
Head of a pin
1-2 mm
MicroElectroMechanical (MEMS) devices
10 -100 µm wide
Pollen grain
Red blood cells
Zone plate x-ray "lens"
Outer ring spacing ~35 nm
Self-assembled, Nature-inspired structure
Many 10s of nm
Nanotube electrode
Quantum corral of 48 iron atoms on copper surface positioned one at a time with an STM tip
Corral diameter 14 nm
The Challenge
Fabricate and combine nanoscale building blocks to make useful devices, e.g., a photosynthetic reaction center with integral semiconductor storage.
Carbon buckyball
~1 nm diameter
Carbon nanotube
~1.3 nm diameter

Variation in Process Parameters

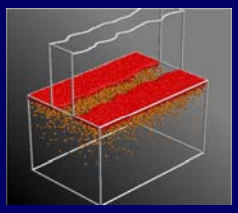


Inter and Intra-die Variations

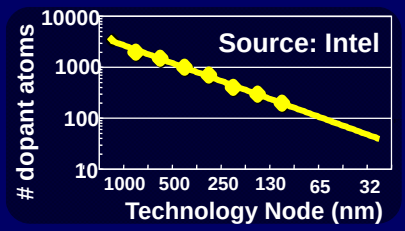




Delay and Leakage Spread



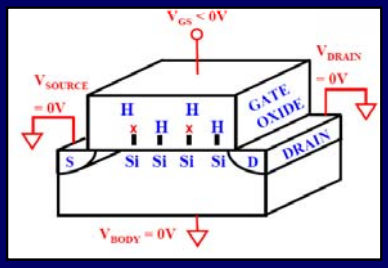
Random dopant fluctuation



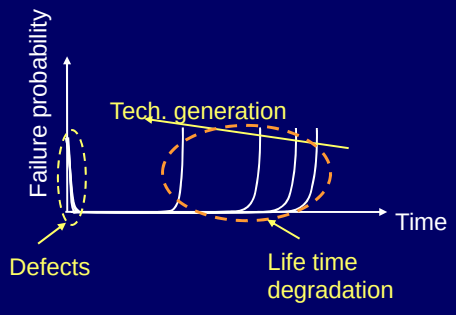
Device parameters are no longer deterministic

Reliability

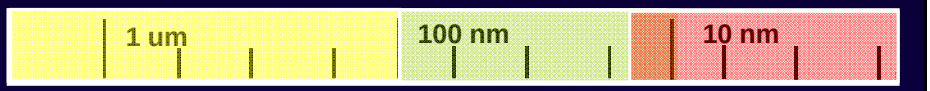
Temporal degradation of performance -- NBTI



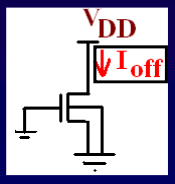
Interface trap generation over time



Scaling & Ion/Ioff



Silicon micro electronics



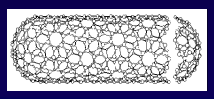
- Increasing leakage
- Increasing process variations
- Short Channel Effects

$\frac{I_{ON}}{I_{OFF}} = 10^6$

Silicon nano electronics

$\frac{I_{ON}}{I_{OFF}} = 10^3$

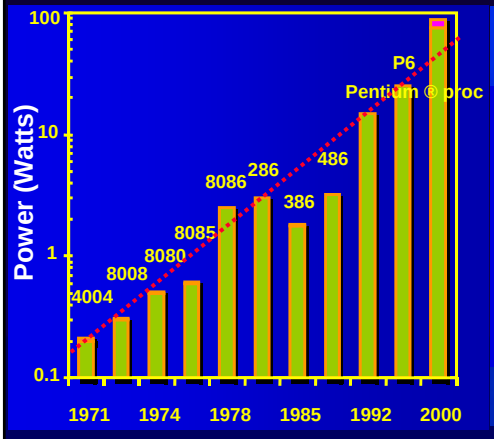
Non-Silicon technology

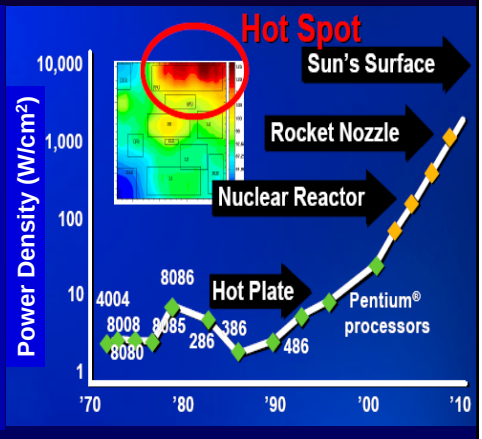


- Carbon Nanotubes
- Molecular transistors
- Molecular RTDs

$\frac{I_{ON}}{I_{OFF}} = 10^4$

2. Power & Power Density



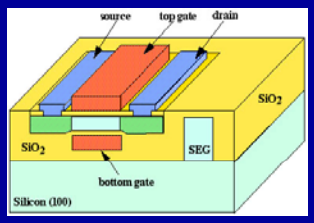


Increased Average Power
- Battery Life
- Cooling Cost

Increased Power Density
- Reliability

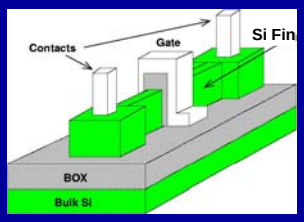
Source: Intel

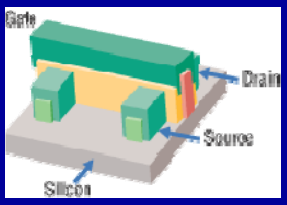
Nano-Scaled Si Devices



DGMOS

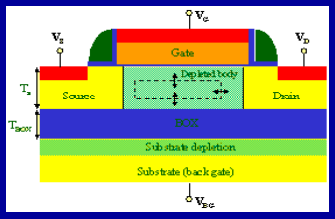
Planar double-gate structure





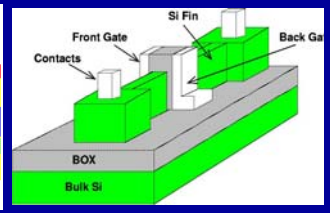
FinFET or Tri-Gate

Quasi-planar DG structure

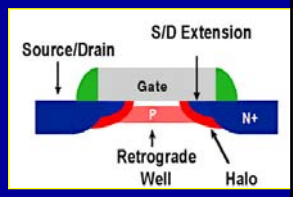


Ground PlaneSOI MOS

Shared back gate DG devices

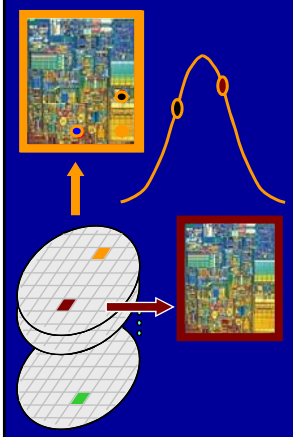


Independent gate FinFET

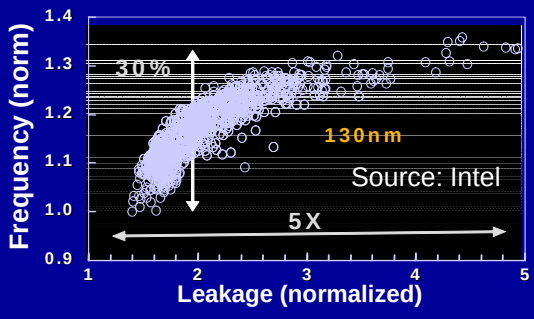


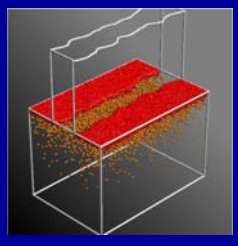
Bulk Si MOSFETs

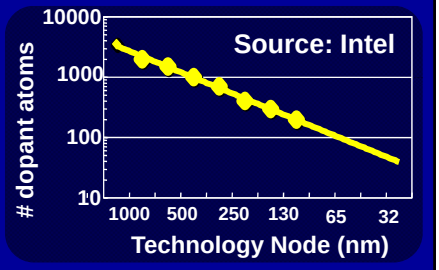
Variation in Process Parameters



Inter and
Intra-die Variations

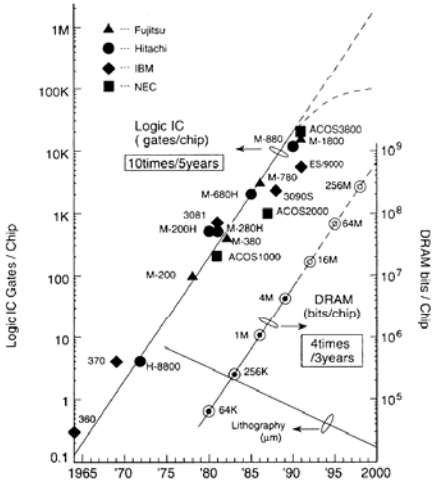




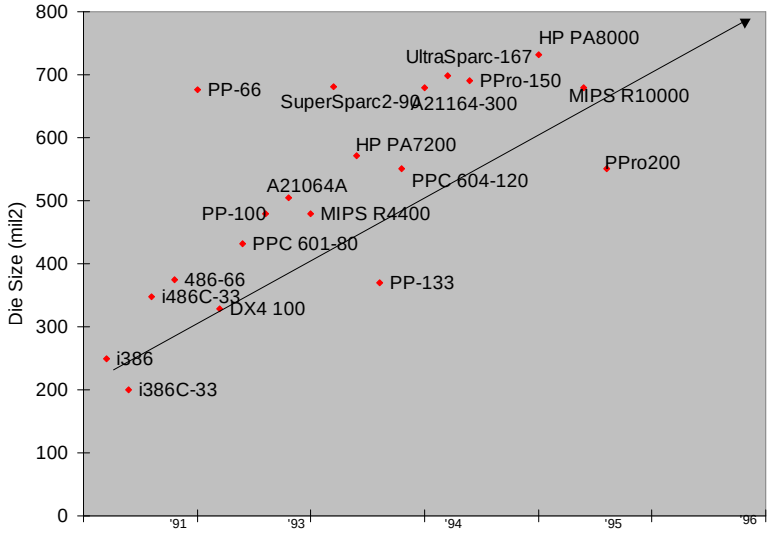


Random dopant fluctuation

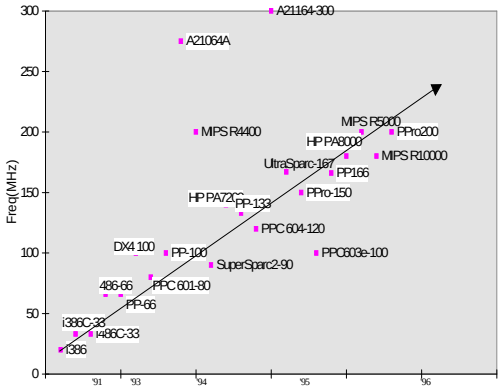
Evolution in Complexity



Processor Trends



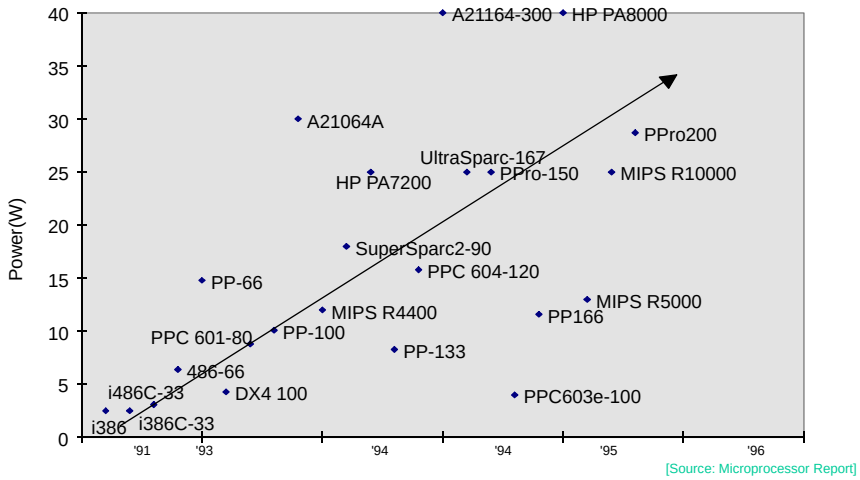
Processor Trends (cont'd)



Higher Performance:

- Higher Frequencies (2x/Generation)
- Higher Device counts (2x /Generation)

Power Trends



[Source: Microprocessor Report]

2x Performance Increase ==> 2x power increase

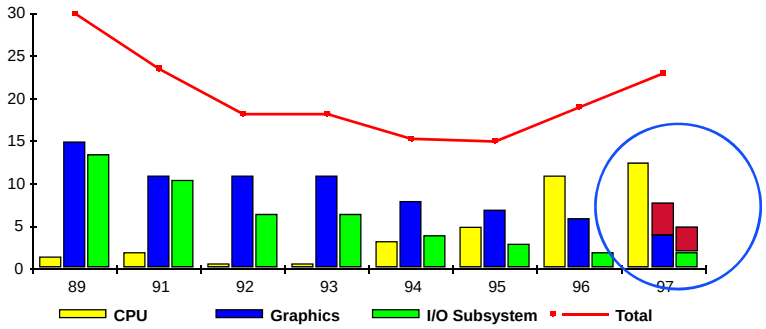
Heat Dissipation

- Chips fail when they get hot
- Need compact and cost-effective cooling solns

CPU	Thermal Soln Cost
486/33mhz	HeatSink $0.50
486DX2 66mhz	Heatsink $1.00
Pentium 66mhz	Larger Heatsink $2.00 System Fan $4.00

- Cooling Solns will become more exotic/expensive
  - Extruded Heatsinks, Heatpipes, Blowers, Noise....
- Every Watt impacts System Cost, esp. for HVM

Where is the Power Going? (Mobile PC)

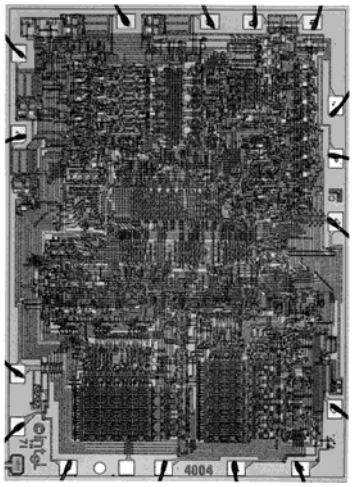


CPU Power: predicted from average device count/area growth

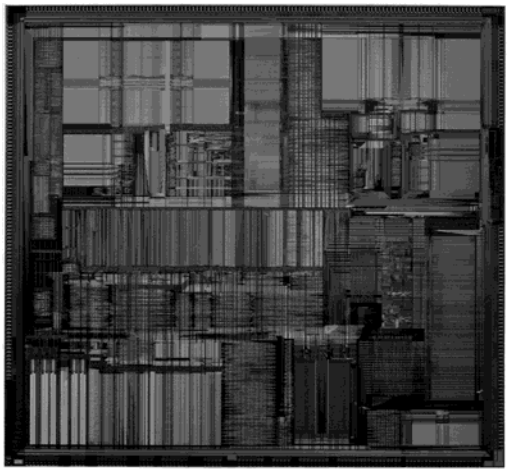
- CPU Power increasing (Predicted in 1994 Low power workshop)
- Graphics & Chipset Power increasing faster than predicted

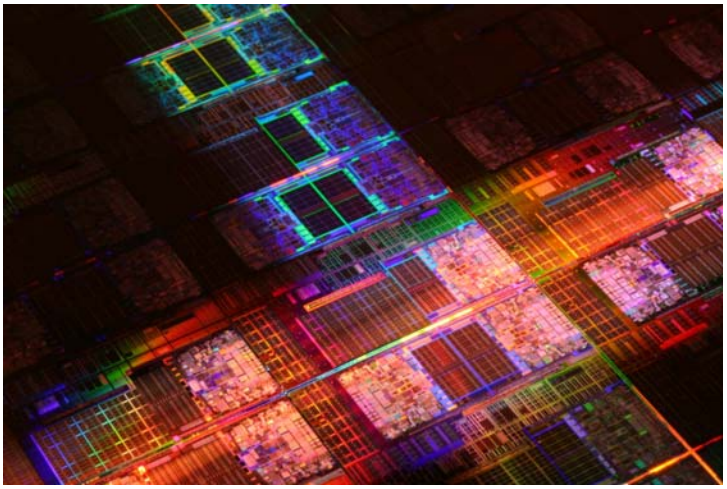
Power reduction is not only a CPU problem

Intel 4004 Microprocessor

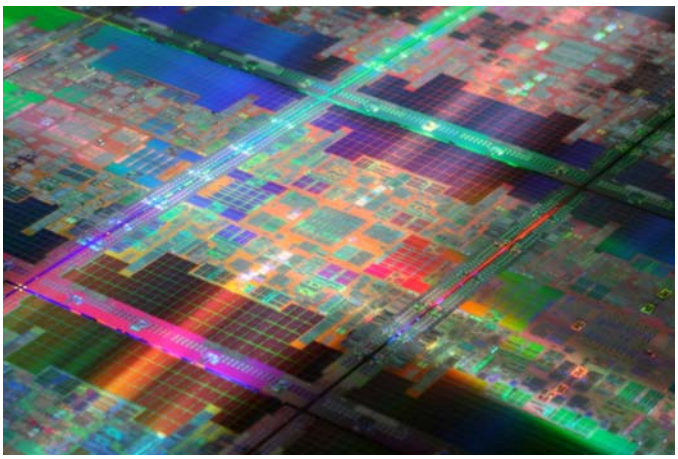


Intel Pentium (II) Microprocessor





Dunnington is the first IA (Intel Architecture) processor with 6-cores,
is based on the 45nm high-k process technology, and has large shared caches.



Tukwila, 4-cores, world's first 2 billion transistor microprocessor

National Technology Roadmap for Semiconductor (NTRS)

Technology (um)	*0.25*	*0.18*	*0.13*	*0.10*	*0.07*
Year	1998	2001	2004	2007	2010
# transistors	28M	64M	150M	350M	800M
On-Chip Clock (MHz)	450	600	800	1000	1100
Area (mm^2)	300	360	430	520	620
Wiring Levels	5	5-6	6	6-7	7-8

Interconnect Performance Trend

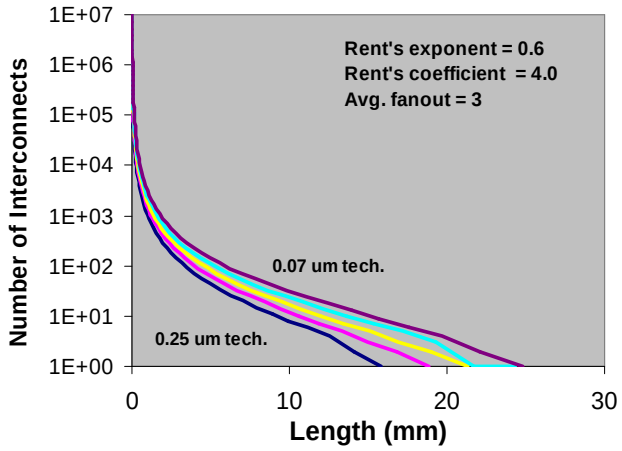
Technology (um)	*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
2cm line delay (ns)	2.589	2.480	2.650	2.620	3.730	4.670
1mm line delay (ns)	0.059	0.049	0.051	0.044	0.052	0.042
Intrinsic gate delay (ns)	0.071	0.051	0.049	0.045	0.039	0.022

Interconnect Complexity

Technology (um)	*0.25*	*0.18*	*0.13*	*0.10*	*0.07*
Length (m)	820	1,480	2,840	5,140	10,000
Wiring Levels	6	6-7	7	7-8	8-9
Opt. # buffers per net	few	→	→	→	many
Opt. # wiresizes per net	few	→	→	→	many
Opt. # buffers per chip	5K	25K	54K	230K	797K

- Performance
- Signal reliability
- Electromigration

Distributions of Wire lengths



Technology Scaling

Technology scaling improves:

- **Transistor & interconnect performance**
- **Transistor density**
- **Energy consumed per switching transition**

0.7X scaling factor (30% scaling) results in:

- **30% gate delay reduction (43% freq. ↑)**
- **2X transistor density increase (49% area ↓)**
- **Energy per transition reduction**

Technology Scaling

- Speed & Performance
  - High drive current and low parasitics
  - Low gate delay and high frequency
- Density & Area
  - Small feature size
- Power & Reliability
  - Low power supply voltage
  - Low off-state leakage

Technology Generation Scaling

$$Dimensions \xrightarrow{scale} 0.7,\ V_{dd} \xrightarrow{scales} \beta,\ V_t \xrightarrow{scales} \beta$$

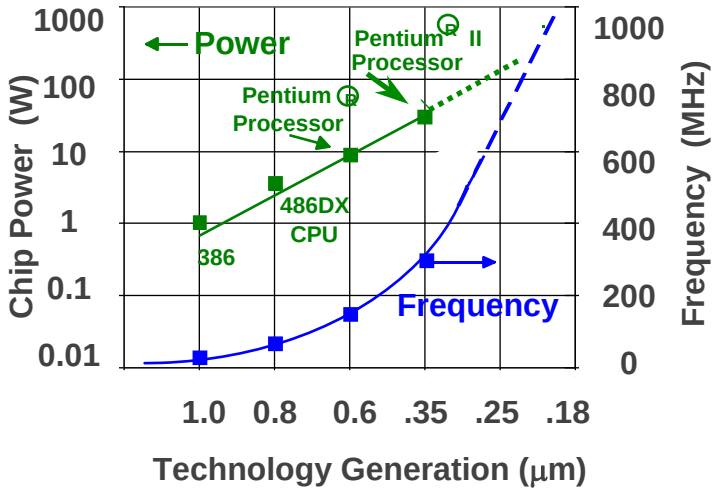
$$I = \frac{kW}{T_{ox}}(V_{dd} - V_t) \xrightarrow{scales} \frac{0.7}{0.7} \times \beta = \beta$$

$$D = \frac{CV_{dd}}{I} \xrightarrow{scales} \frac{0.7 \times \beta}{\beta} = 0.7 \quad \text{(30\% delay reduction)}$$

$$E = CV_{dd}^{\ 2} \xrightarrow{scales} 0.7\beta^{\ 2}$$

IC Frequency & Power Trends

- Clock frequency improves 50%
- Gate delay improves ~30%
- Power increases 50%
- Power = $C_L V^2 f$

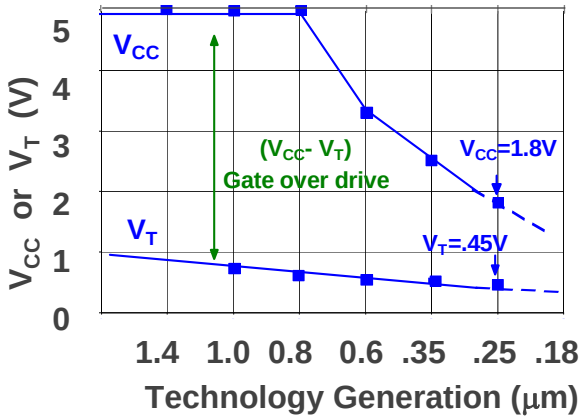


↑ Active switched capacitance "C_L" is increasing.

58

Constant Voltage vs Field Scaling

- Recently: constant e-field scaling, aka voltage scaling
- V_{CC} ⌫ 1V
- V_{CC} & modest V_T scaling
- Loss in gate overdrive (V_{CC}-V_T)



Voltage scaling is good for controlling IC's active power, but it requires aggressive V_T scaling for high performance

59

Barriers to Voltage Scaling

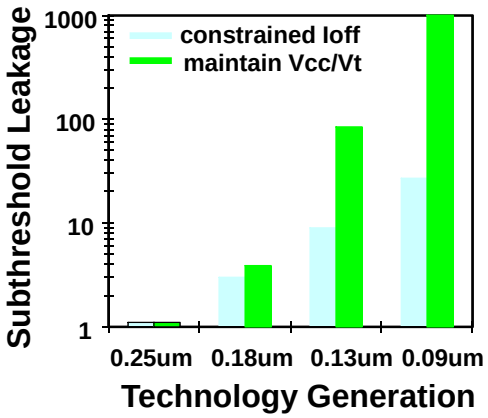
Voltage Scaling = Constant Electric Field Scaling

Voltage scaling is good for IC's active power, but degrades gate over drive. Requires V_T scaling.

- Leakage power
- Short-channel effects
- Special circuit functionality, noise
- Soft error
- Parameter variation

60

Barriers to Voltage Scaling



- Leakage power
- Short-channel effects
- Soft error
- Special circuit functionality

61

Delay

$$\tau_d = \frac{C_L V_{DD}}{I_D}$$

$$\tau_d = \frac{C_L}{(\frac{W}{2L})\mu C_{ox} V_{DD}(1-\frac{V_T}{V_{DD}})^2}$$ Long Channel MOSFET

$$\tau_d = \frac{C_L}{WC_{ox}\upsilon_{SAT}(1-\frac{V_T}{V_{DD}})}$$ Short Channel MOSFET

$$\tau = \frac{CL^{0.5}T_{ox}^{0.5}}{V_{DD}^{0.3}(0.9-V_T/V_{DD})^{1.3}}(\frac{1}{W_n}+\frac{2.2}{W_p})$$ [1]

[1] C. Hu, "Low Power Design Methodologies," Kluwer Academic Publishers, p. 25.

Performance significantly degrades when V_{DD} approaches $3V_T$.

62

V_T Scaling: V_T and I_{OFF} Trade-off

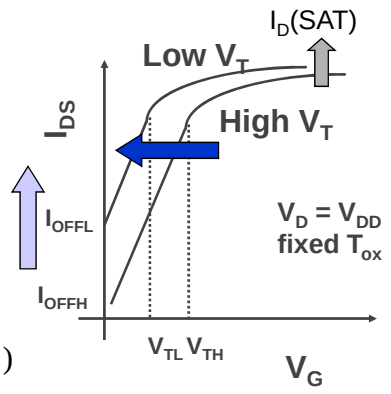
Performance vs Leakage:

$V_T \downarrow I_{OFF} \uparrow I_D(SAT) \uparrow$

$$I_{OFF} \propto I_{subth} \propto \frac{W_{eff}}{L_{eff}} K_1 e^{(V_{GS}-V_T)}$$

$$I_D(SAT) \propto \frac{W_{eff}}{L_{eff}} K_2 (V_{GS}-V_T)^2$$

$$I_D(SAT) \propto K_3 W_{eff} C_{ox} \upsilon_{SAT} (V_{GS}-V_T)$$

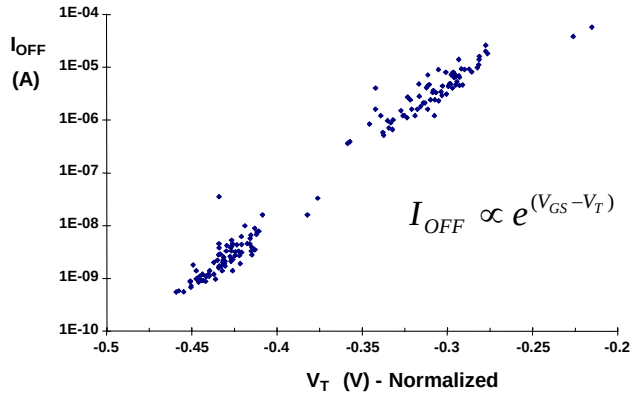


- As V_T decreases, sub-threshold leakage increases
- Leakage is a barrier to voltage scaling

63

I_{OFF} vs V_T

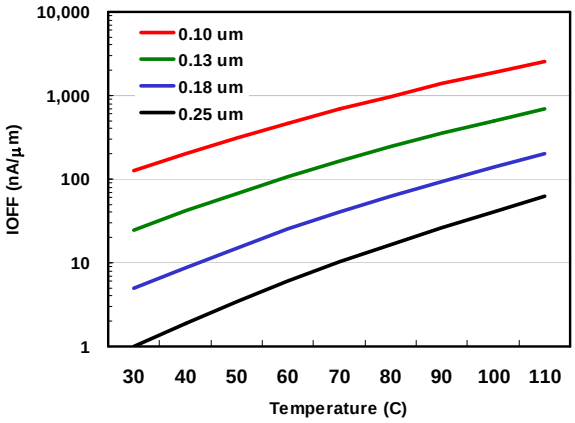
Log I_{OFF}



V_{TP} (V)

I_{OFF} is an exponential function of V_T.

Future: Projected Leakage Trends

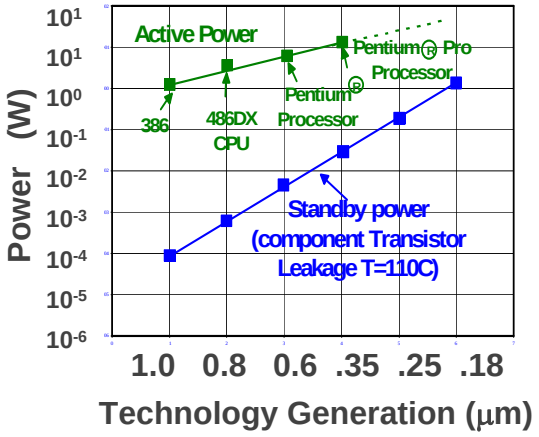


I_{OFF} (0.25um) = 1 nA/um (scales 5X)
V_T (0.25um) = 450 mV (scales by 15%)

S_t (30C) = 80 mV/dec
S_t (100C) = 100
d V_T/dT = 0.7 mV/C

Why Excessive leakage an Issue?

- Leakage component to active power becomes significant % of total powe
- Approaching ~10% in 0.18 μm technology
- Acceptable limit less than ~10%, implies serious challenge in V_T scaling!

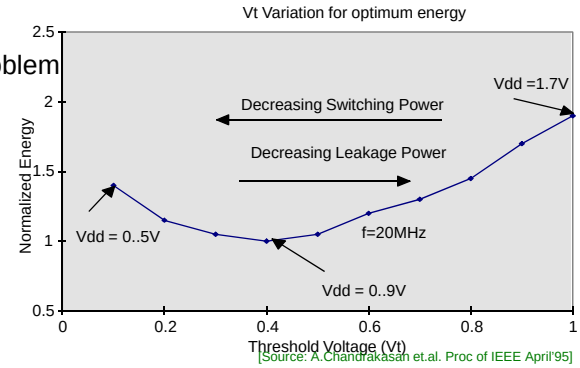


Barrier ↓ high static leakage (standby) power

67

Power Trends

- Enable development of ultra low voltage circuits
- At lower Vt,
  - leakage becomes a problem
  - Signal integrity and Noise margin



[Source: A.Chandrakasan et.al. Proc of IEEE April'95]

- Multiple on-chip Vt, dynamic Vt
- Other challenges for low voltages ?

Trends in Microelectronics

- Improvement in device technology
  - Smaller circuits
  - Faster circuits
  - More circuits on a chip
- Higher Integration
  - More complex systems
  - Lower cost of computation
  - Higher reliability
- Limitations
  - Intrinsic device scaling limits
  - Cost of fabrication
  - Interconnect limitation
  - Large scale design management

Problems of Microelectronics

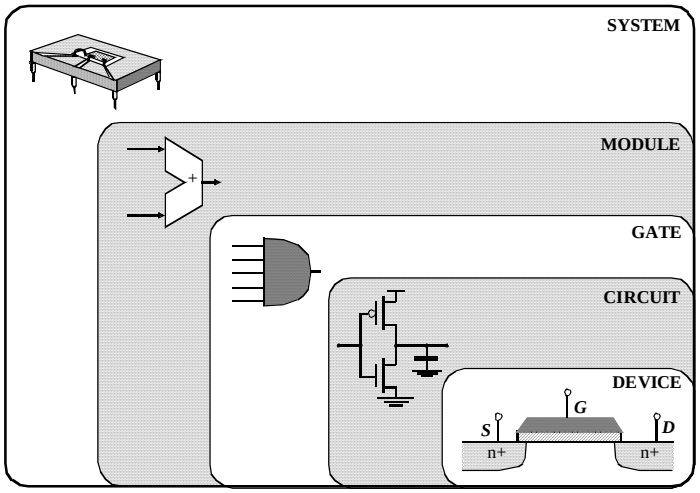
- Design Cost:
  - design time
  - fabrication time
  - impossibility to repair
  - reduce design cost to be competitive in price
- Marketing Issues:
  - use most recent technologies to stay competitive in performance
  - volume production is inexpensive
  - time-to-market is critical
  - evolving market
- Solution:
  - Hierarchical and abstraction
  - Different design styles
  - Computer-Aided-Design

Circuit and System Representations

Complex digital system ⟶ Component gates + Memory systems

- 3 design domains
  - Behavioral
    - specifies what a particular system does
  - Structural
    - how entities are connected together to effect the prescribed manner
  - Physical
    - how to actually build a structure that has the required connectivity to implement the prescribed behavior

Design Abstraction Levels



For a Digital Design

- Architecture
- Algorithm
- Module or Functional Block
- logical
- Switch
- Circuit
- Layout

Behavioral Representation Domain

- Hardware description language
  - VHDL, Verilog
- Boolean equation
- Within this domain, there are various level of abstraction
  - Algorithm
  - Register transfer level (communication between registers)

    Acc ⟵ Acc + R1
  - Boolean equations

    CO = A.B + A.C + B.C

    ↓

    carry

Behavioral Representation Domain - cont.

- Algorithm level (Verilog)

can include speed info

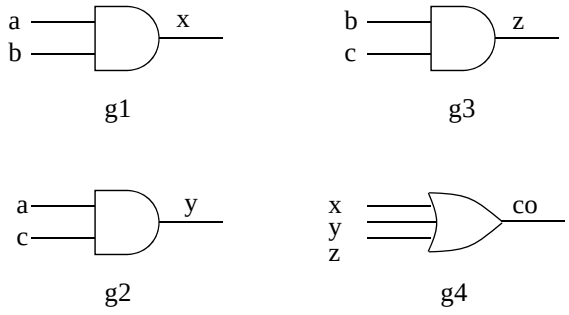
```
MODULE carry (co, a,b,c)
    output co
    input a, b, c
    assign co = (a&b)|(a&c)|(b&c);
ENDMODULE
```

Structural Domain

- The levels of abstraction include
  - module
  - gate
  - switch
  - circuit

```
MODULE   carry (co, a, b, c)
         input a, b, c;
         output co;
         wire x, y, z
              AND    g1 (x, a, b)
              AND    g2 (y, a, c)
              AND    g3 (z, b, c)
              OR     g4 (co, x, y, z);
ENDMODULE
```

Structural Domain- cont.



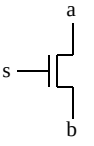
Transistor Level

```
MODULE   carry (co, a, b, c)
         input    a, b, c;
         output   co;
         wire     i1, i2, i3, i4, cn;
                  NMOS   n1(i1, vss, a)
                  NMOS   n2(i1, vss, b)
                    .
                    .
                    .
                  PMOS   p1(i3, vdd, b);
                  PMOS   p2(cn, i3, a);
                    .
                    .
                    .
ENDMODULE
```

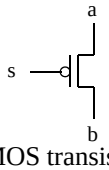
Physical Representation

```
MODULE   carry ;
         Input    a, b, c;
         output   co;
         boundary [0, 0, 100, 400]
              port a aluminum width = 1 origin = [0,2]
              port b aluminum width = 1 origin = [0,7]
              port
              .
              .
              .
              Port ci polysilicon …….
ENDMODULE
```

CMOS Logic

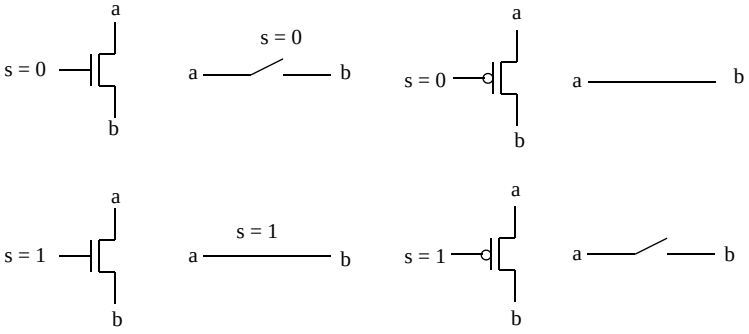


NMOS transistor

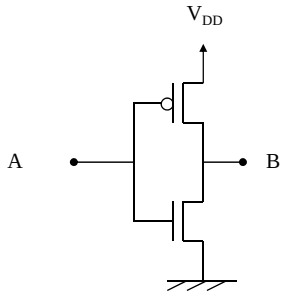


PMOS transistor

Consider them as switches

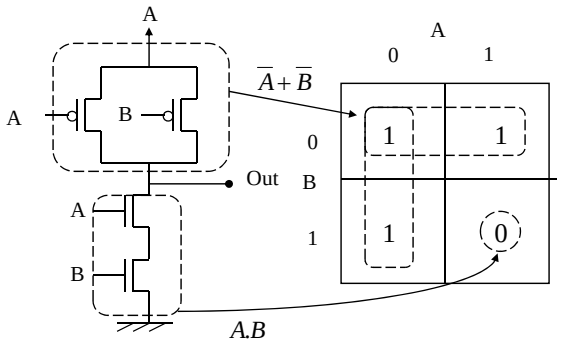


Inverter ($\overline{A}$)

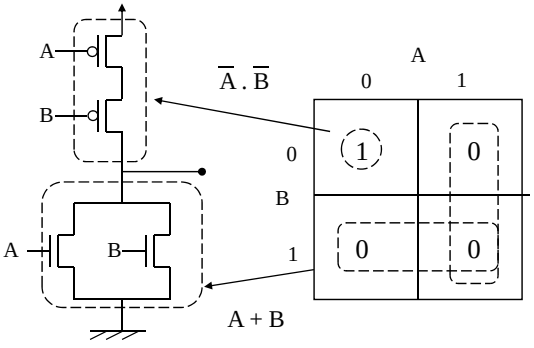


- Low power dissipation

NAND ($\overline{AB}$)



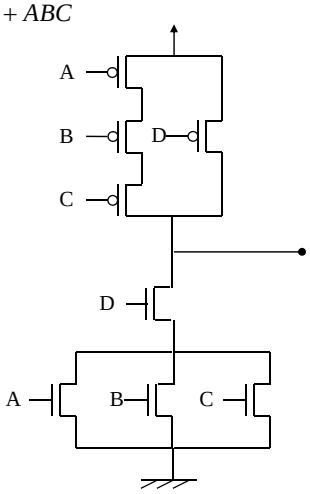
NOR ($\overline{A+B}$)



Complex Gates

$F = \overline{((A+B+C).D)} = \overline{D} + \overline{A}\overline{B}\overline{C}$

$\overline{F} = (A+B+C).D$



VLSI Design is Inter-Disciplinary

- Breadth of field
  - Semiconductor physics and technology
  - Integrated electronics
  - Systems design
  - Testing
  - Computer-Aided Design
- Depth of field
  - Complexity of fabrication technology
  - Difficulty of design problems