Homework 6 Solution

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 18-Nov-2009 Due: 24-Nov-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: Consider a standard 6-T SRAM cell. Use the following parameters.

$L = 300$ nm, $V_{DD} = 2.5$ V.

For all the NMOS transistors, allowed *minimum* and *maximum* widths are 450 nm and 1800 nm, respectively. Always size the pull-up PMOS transistors as three-times the widths of the pull-down NMOS transistors. You should consider widths in *50 nm* intervals.

Write your assumptions with clear and concise explanation for all the parts below.

Part a) Determine by hand calculation

i) *Cell ratio* (ratio of the widths of pull-down NMOS and access transistor) for read
ii) *Pull-up ratio* (ratio of the widths of pull-up PMOS and access transistor) for write

Write the regions of operation of all the transistors for both i) and ii).

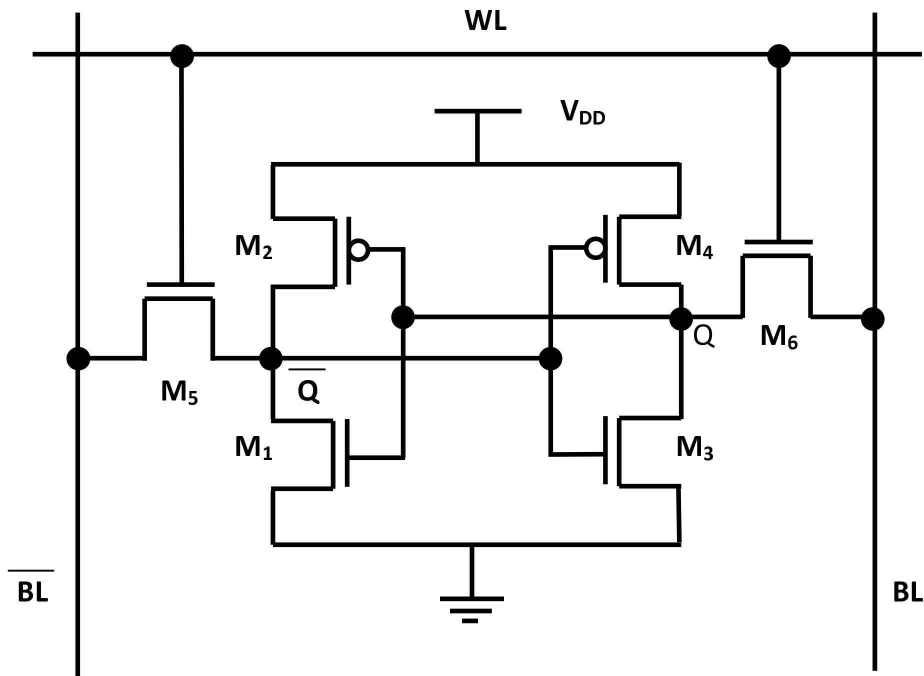
Any extra parameter that you might need, you should *extract* from the SPICE library that you are using.

Solution:

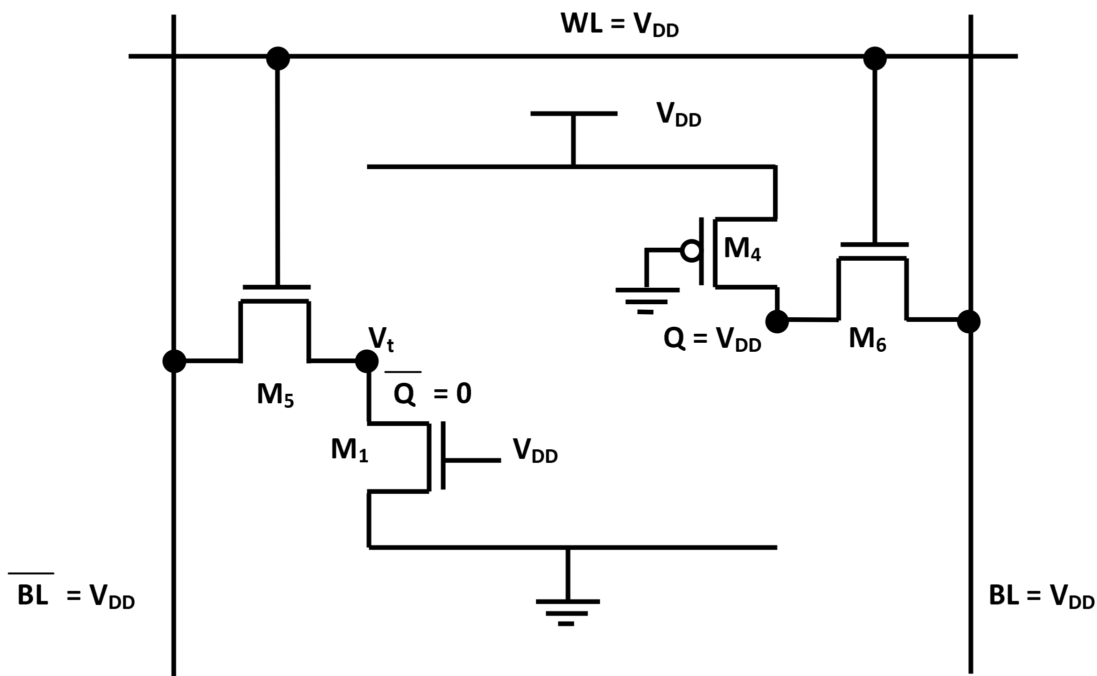
From the SPICE libraries, *tsmc25N* and *tsmc25P*, we get

$V_{tn0} = 0.431$ V, $V_{tp0} = -0.616$ V. Also, $\mu_{n0} = 455.4$ cm^2/V/S, $\mu_{p0} = 158.7$ cm^2/V/S.

A schematic diagram of a standard 6-T SRAM cell is given below.



i) During read operation with $Q = V_{DD}$, the corresponding schematic diagram is shown below. When the voltage at node $\overline{Q}$ reaches the threshold voltage of the NMOS, M_3 (see the complete 6-T cell), the voltage at node Q starts to fall and the regenerative action of the cross-coupled inverter will force the flipping of the bit in the cell.



We can get some more appropriate values of the threshold voltages for the transistors by doing operating point analysis (.OP command in SPICE). To do an operating point analysis, we need to set the terminals voltages of an MOS and use .OP command that will print different extracted parameters (e.g., vth) for the MOS.

First, we can do an operating point analysis for the NMOS, M_3 to get the voltage V_t. Then we can use the value of V_t to perform operating point analyses for the MOSs M_1 and M_5. For the access transistors we should notice that there is *body-effect* which can increase their threshold voltages.

MOS	Gate Voltage (V)	Drain Voltage (V)	Source Voltage (V)	Substrate Voltage (V)	Threshold Voltage (V)
M_3	0.491	2.5	0	0	0.491
M_1	2.5	0.491	0	0	0.511
M_5	2.5	2.5	0.491	0	0.581

Regions of operation for the transistors:

M1: Linear, **M2:** Cut-off, **M3:** Cut-off, **M4:** Linear, **M5:** Saturation, **M6:** Cut-off.

We can write the regions of operation of the transistors similarly when *Q = 0* during read operation.

To prevent read failure, the transistor M_1 should be strong enough so that the voltage at node $\overline{Q}$ does not rise more than V_t = 0.491 V. Accordingly,

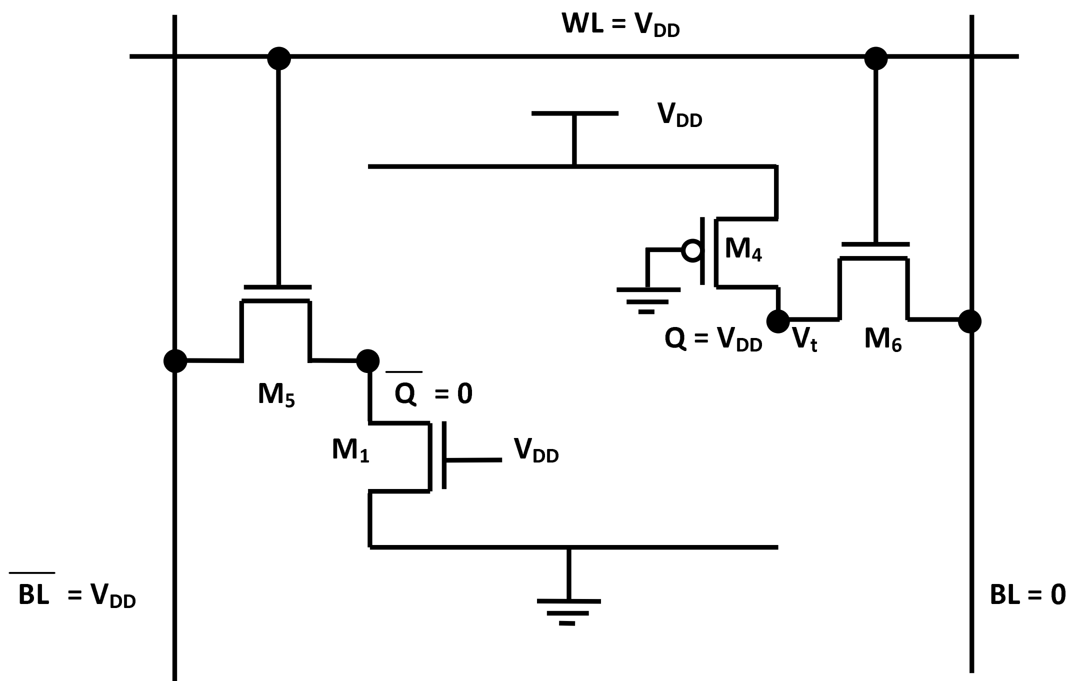
$$I_{M1} \geq I_{M5}$$

$$\Rightarrow \left(\frac{W}{L}\right)_1 \left((2.5 - 0.511) * 0.491 - \frac{0.491^2}{2} \right) \geq \left(\frac{W}{L}\right)_5 \frac{(2.5 - 0.491 - 0.581)^2}{2}$$

$$\Rightarrow \frac{W_1}{W_5} \geq \frac{1.0196}{0.8561}$$

$$\Rightarrow CR = \frac{W_1}{W_5} \geq 1.191.$$

ii) During write operation, say we are going to write $Q = 0$ while initially $Q = V_{DD}$, the corresponding schematic diagram is shown below. When the voltage at node Q reaches a voltage so that the PMOS, M_2 (see the complete 6-T cell) gets ON, the voltage at node $\overline{Q}$ starts to rise and the regenerative action of the cross-coupled inverter will force the write $Q = 0$.



First, we can do an operating point analysis for the PMOS, M_2 to get the voltage V_t. Then we can use the value of V_t to perform operating point analyses for the MOSs M_4 and M_6.

MOS	Gate Voltage (V)	Drain Voltage (V)	Source Voltage (V)	Substrate Voltage (V)	Threshold Voltage (V)
M_2	(2.5 - 0.517)	0	2.5	2.5	-0.517
M_4	0	(2.5 - 0.517)	2.5	2.5	-0.526
M_6	2.5	0	(2.5 - 0.517)	0	0.496

Regions of operation for the transistors:

M1: Linear, **M2:** Cut-off, **M3:** Cut-off, **M4:** Linear, **M5:** Saturation, **M6:** Linear.

We can write the regions of operation of the transistors similarly for writing $Q = V_{DD}$ while initially $Q = 0$.

To prevent write failure, the transistor M_6 should be strong enough so that the voltage at node Q does go below V_t = (2.5 - 0.517) V = 1.983 V. Accordingly,

$$-3*\left(\frac{W}{L}\right)_6\left(\left(2.5-1.983-0.496\right)\left(-1.983\right)-\frac{\left(-1.983\right)^2}{2}\right)$$

$$\geq\left(\frac{W}{L}\right)_4\left(\left(-2.5+0.526\right)\left(1.983-2.5\right)-\frac{\left(1.983-2.5\right)^2}{2}\right)$$

$$\Rightarrow\frac{W_4}{W_6}\leq\frac{3*0.8869}{2.0078}$$

$$\Rightarrow PR=\frac{W_4}{W_6}\leq 1.325.$$

Please note that $\mu_{n0}\approx 3*\mu_{p0}$ has been used in the above calculation. For the NMOS M_6, the terminal attached to BL has been assumed as *drain*.

Note: Both the cell ratio and pull-up ratio are restricted and endorsed by the minimum width allowable by a technology library and the requirement of having high-density of memory array (i.e., having lower widths of the transistors). Also, notice that we have assumed same L (= 300 nm) for all the transistors.

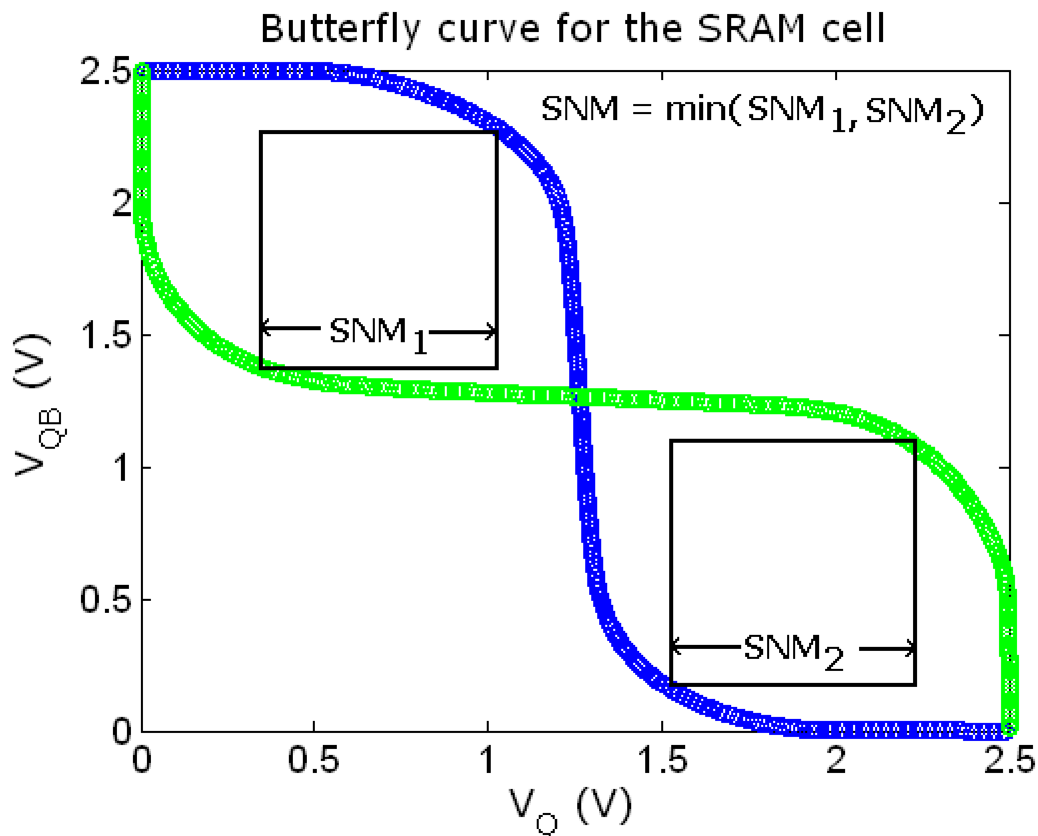
Part b) Size the transistors in the SRAM cell to have the *maximum read stability*. By SPICE simulation, determine the *static noise margin* (SNM) of the SRAM cell. (SNM is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell.) Explain the procedure you have followed.

Solution:

For maximum read stability, the *cell ratio* should be as high as possible. With the allowable values provided, we should choose the following widths of the transistors for maximum read stability.

M1/M3: 1800 nm, **M2/M4:** 5400 nm, **M5/M6:** 450 nm.

The concept of *static noise margin* (SNM) for an SRAM cell is shown the figure below. The SNM is defined as the minimum noise voltage present at *each* of the cell storage nodes necessary to flip the state of the cell. A basic understanding of the SNM is obtained by drawing and mirroring the inverter characteristics and then finding the *maximum* square between them.



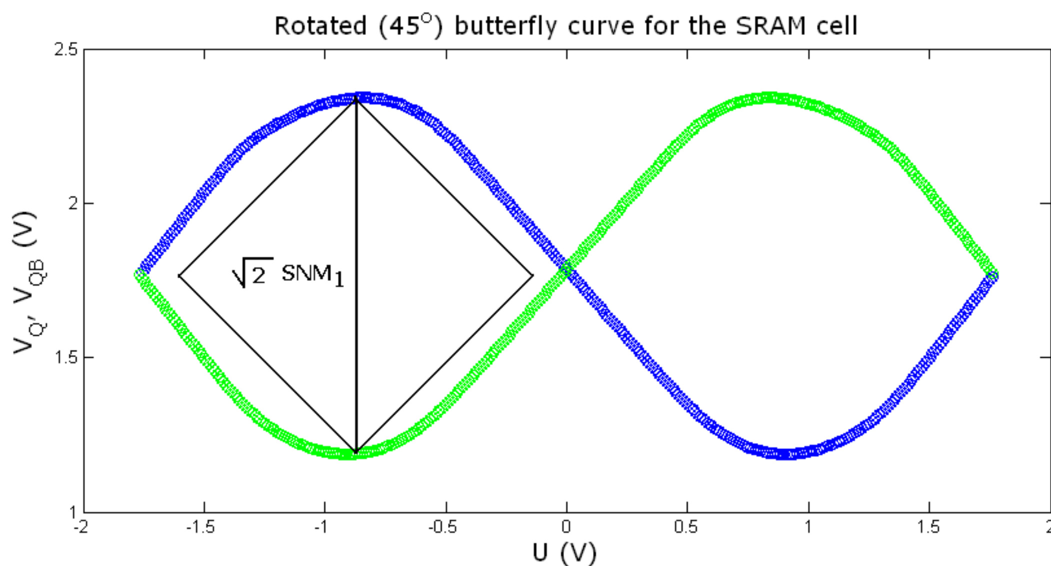
Simulation Method based on Graphical Technique:

We can determine the SNM graphically from the inverter characteristics. However, we have to perform one SPICE simulation having voltage controlled voltage sources (VCVS) that will be clear onwards. You can use the following reference for details.

Reference

Seevinck, E., List, F. J., and Lohstroh, J., "Statis-Noise Margin Analysis of MOS SRAM Cells,", IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, October, 1987.

A 45° rotated picture corresponding to the butterfly curve is shown below. The voltage *U* spans from $-V_{dd}/\sqrt{2}$ to $V_{dd}/\sqrt{2}$.



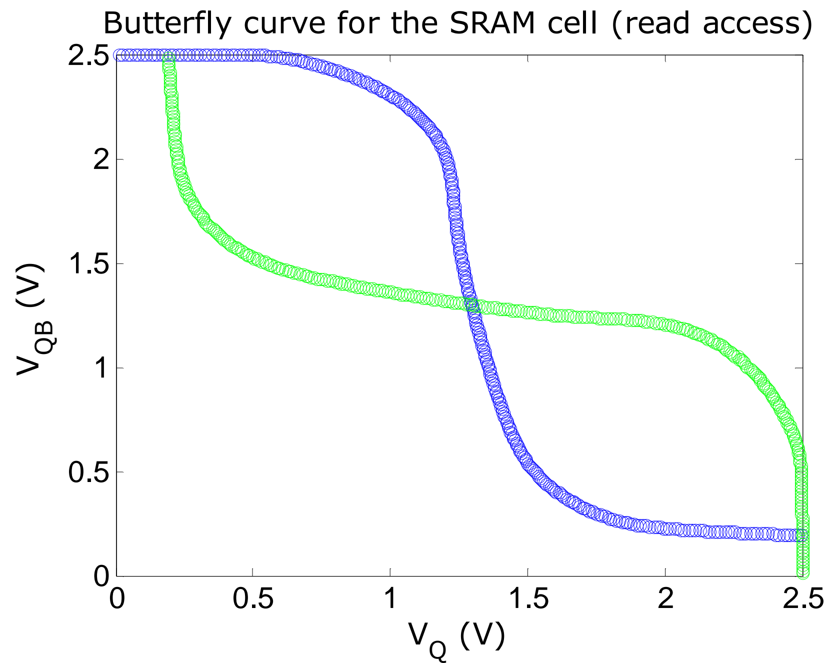
Note: Please note that both the previous figures are obtained by choosing word line, WL = 0.

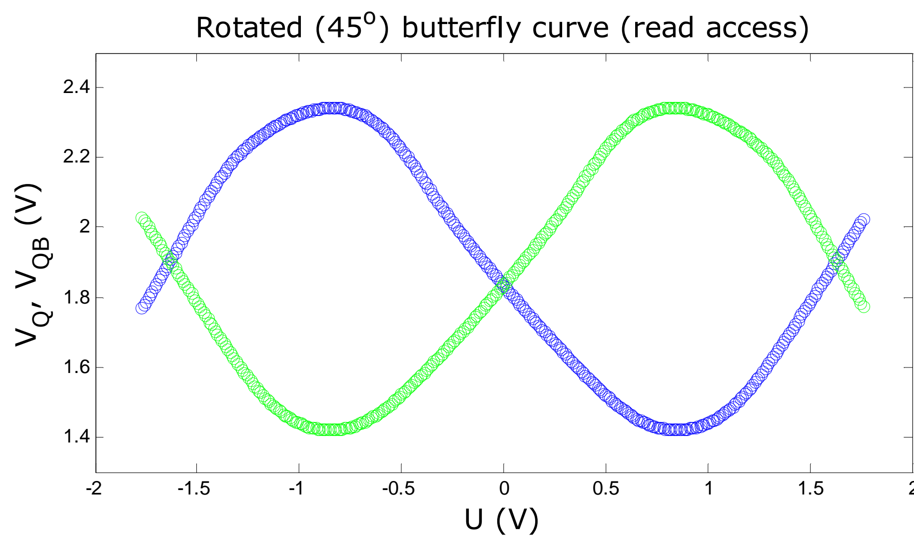
When read process is initiated, i.e., WL is made logic high, the inverter characteristics changes and hence the SRAM cell gets vulnerable to noise. We are asked to determine the SNM while it's reading.

The corresponding SPICE code to determine the SNM and the modified butterfly curves during read access are given next. **We can see that the SNM gets decreased during read access.** From the SPICE code we get the following values.

WordLine (WL)	**Static Noise Margin (SNM) (V)**
Logic 0	0.8146
Logic 1 (read)	0.6521

Please note that, 1pF of bitline capacitance has been used to simulate the effect of having a memory array.





SPICE Code (Graphical Technique)

```
* HW 6, Problem 1, Determination of SNM graphically
* ECE 559, Fall 2009, Purdue University

.TEMP    25.0000
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.GLOBAL VDD!

.PARAM VDD  = 2.5
.PARAM L    = 300n

.PARAM WN   = 1800n
.PARAM WP   = '3*WN'

.PARAM WNA  = 450n

.PARAM U   = 0
.PARAM UL  = '-VDD/sqrt(2)'
.PARAM UH  = ' VDD/sqrt(2)'

.PARAM BITCAP  = 1e-12

.OPTION POST

CBL  BLB 0 BITCAP
CBLB BL  0 BITCAP

* one inverter
MPL QD QB VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MNL QD QB 0  0    TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1
```

```
* one inverter
MPR QBD Q VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MNR QBD Q 0 0    TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1

* access transistors
MNAL BLB WL QBD     0    TSMC25N  L='L' W='WNA'
+AD='WNA*2.5*L' AS='WNA*2.5*L' PD='2*WNA+5*L' PS='2*WNA+5*L'
+M=1
MNAR BL  WL QD       0    TSMC25N  L='L' W='WNA'
+AD='WNA*2.5*L' AS='WNA*2.5*L' PD='2*WNA+5*L' PS='2*WNA+5*L'
+M=1

VVDD!   VDD! 0          DC=VDD

* when reading, use VDD
VWL    WL   0  DC=VDD

.IC V(BL)  = VDD
.IC V(BLB) = VDD

* use voltage controlled voltage sources (VCVS)

* changing the co-ordinates in 45 degree angle
EQ     Q           0          VOL=' 1/sqrt(2)*U + 1/sqrt(2)*V(V1)'
EQB  QB           0          VOL='-1/sqrt(2)*U + 1/sqrt(2)*V(V2)'

* inverter characteristics
EV1  V1 0        VOL=' U + sqrt(2)*V(QBD)'
EV2  V2 0        VOL='-U + sqrt(2)*V(QD)'

* take the absolute value for determination of SNM
EVD  VD 0        VOL='ABS(V(V1) - V(V2))'
```

```
.DC  U UL UH 0.01

.PRINT DC V(QD) V(QBD) V(V1) V(V2)

.MEASURE DC MAXVD MAX V(VD)

* measure SNM
.MEASURE DC SNM param='1/sqrt(2)*MAXVD'

.END
```

SPICE Code (Trial-and-Error Technique)

```
* HW 6, Problem 1, SNM by SPICE simulation
* ECE 559, Fall 2009, Purdue University

.TEMP    25.0000
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.GLOBAL VDD!

.PARAM VDD  = 2.5
.PARAM L    = 300n

.PARAM WN   = 1800n
.PARAM WP   = '3*WN'

.PARAM WNA  = 450n

.PARAM VNOISE  = 0.66

.PARAM BITCAP  = 1e-12

.OPTION POST

CBL  BLB 0 BITCAP
```

```
CBLB BL  0 BITCAP

* one inverter
MPL Q QBN VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MNL Q QBN 0  0    TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1

* one inverter
MPR QB QN VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MNR QB QN 0 0    TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1

* access transistors
MNAL BLB WL QB       0    TSMC25N  L='L' W='WNA'
+AD='WNA*2.5*L' AS='WNA*2.5*L' PD='2*WNA+5*L' PS='2*WNA+5*L'
+M=1
MNAR BL  WL Q         0    TSMC25N  L='L' W='WNA'
+AD='WNA*2.5*L' AS='WNA*2.5*L' PD='2*WNA+5*L' PS='2*WNA+5*L'
+M=1

VVDD!   VDD! 0          DC=VDD

VWL     WL   0  DC=VDD

VNOISEL QBN  QB DC=VNOISE
VNOISER Q    QN DC=VNOISE

.IC V(Q)  = VDD
.IC V(QB) = 0

.IC V(BL)  = VDD
.IC V(BLB) = VDD
```

```
.TRAN 0.1n 1.5n UIC
.PRINT TRAN V(QB) V(Q) V(BLB) V(BL)

.END
```

Note:

1. We can vary the voltage *VNOISE* and check in the output of the print command if the bit stored in the cell is flipping or not. We notice that when *VNOISE* changes from 0.65 V to 0.66 V, the bit stored in the cell flips. Accordingly, the SNM would be **0.65 V** which quite matches with the value that has been achieved by the graphical technique (0.6521 V).

2. Notice the polarity of the noise voltage sources at the input of each inverter. It depends on the logic value of the bit stored in the cell.

Part c) What happens to the write operation for the cell? If write operation fails, size the transistors in such a way that it's at the verge of satisfying the write operation. By SPICE simulation, determine the *static noise margin* (SNM) of the SRAM cell. Explain the procedure you have followed.

Compare SNM for this part with that of part b). Explain if the result is according to your expectation or not.

Solution:

When we check for the **write operation**, it **fails**.

As discussed in the part a), we understand that we can reduce the width of the pull-up PMOS transistors to facilitate write operation. This can be done by choosing lower widths of the pull-down NMOS transistors (as we are asked to choose always the widths of the pull-up PMOS transistors as three-times the widths the pull-down NMOS transistors). At the verge of satisfying the write operation, we find

M1/M3: 750 nm, **M2/M4:** 2250 nm, **M5/M6:** 450 nm.

The corresponding SNM has been found to be **0.5 V.** Similar procedure as in part b) is followed.

The SNM for the part c) is found to be less than that of part b). **Yes, it meets the expectation** as we are *reducing the read stability* of the cell by reducing the width of the pull-down NMOS transistors.

SPICE Code

```
* HW 6, Problem 1, Part c) Solution
* ECE 559, Fall 2009, Purdue University

.TEMP    25.0000
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.GLOBAL VDD!

.PARAM VDD  = 2.5
```

```
.PARAM L    = 300n

.PARAM WN   = 750n
.PARAM WP   = '3*WN'

.PARAM WNA  = 450n

.PARAM VNOISE  = 0

.PARAM BITCAP  = 1e-12

.OPTION POST

CBL  BLB 0 BITCAP
CBLB BL  0 BITCAP

* one inverter
MPL Q QBN VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MNL Q QBN 0  0    TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1

* one inverter
MPR QB QN VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MNR QB QN 0 0    TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1

* access transistors
MNAL BLB WL QB       0    TSMC25N  L='L' W='WNA'
+AD='WNA*2.5*L' AS='WNA*2.5*L' PD='2*WNA+5*L' PS='2*WNA+5*L'
+M=1
MNAR BL  WL Q          0    TSMC25N  L='L' W='WNA'
+AD='WNA*2.5*L' AS='WNA*2.5*L' PD='2*WNA+5*L' PS='2*WNA+5*L'
```

```
+M=1

VVDD!   VDD! 0          DC=VDD

VWL     WL   0  DC=VDD

VNOISEL QBN  QB DC=VNOISE
VNOISER Q    QN DC=VNOISE

* logic 1 is stored in the cell initially
.IC V(Q)  = VDD
.IC V(QB) = 0

* writing logic 0 in cell
.IC V(BL)  = 0
.IC V(BLB) = VDD

.TRAN 0.1n 30n UIC
.PRINT TRAN V(QB) V(Q) V(BLB) V(BL)

.END
```

Note:

1. We can vary the parameter *WN* and check in the output of the print command if the bit stored in the cell is flipping or not. We notice that when *WN* changes from 800nm to 750nm, the bit stored in the cell flips. Accordingly, when **WN = 750 nm**, the cell is at the verge of satisfying the write operation.

2. Note that we could have increased the widths of the access transistors to bring the cell at the verge of satisfying the write operation, however, it shouldn't be chosen as in that case we would have higher widths of the transistors in the cell affecting the density of memory array.