Homework 5

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 24-Oct-2009 Due: 03-Nov-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: The problem considers the *charge leakage* problem in dynamic logic based circuits. Consider a 16-input OR gate implemented in domino logic with a *PMOS keeper*. Draw and submit the schematic (on paper by hand is OK if you don't use Cadence). Use the following parameters.

L = 300 nm, V_{DD} = 2.5 V, $W_{pre\text{-}charge}$ = 900 nm, $W_{evaluate}$ = 450 nm,
Widths of NMOSs in the PDN, $W_{NMOS\text{-}PDN}$ = 9000 nm.

For any other transistors, allowed *minimum* and *maximum* widths are 450 nm and 1800 nm, respectively. You should consider widths in *50 nm* intervals.

Part a): Determine (by hand calculation) the width of the keeper PMOS ensuring the *correct functionality* of the gate. You can select the characteristics of the output inverter by your own *with explanation*. State your assumptions, if any. Use the following information.

$K_p' = \mu_p C_{ox}$ = 300e-6 A/V^2 $K_n' = \mu_n C_{ox}$ = 600e-6 A/V^2

V_{tp} = -0.5 V V_{tn} = 0.5 V.

Part b) Perform SPICE simulation to determine the width of the keeper PMOS and the widths of the output inverter MOSs that achieve the *fastest operation* of the gate, however, you should ensure the *correct functionality* of the gate. Clearly state your procedure and assumptions, if any. Use

Rise/Fall Time = 0.01 ns, Delay Time = 0.01 ns, Clock Period = 200 ns (with 50% duty cycle), the high/low state of the other input signals you can choose at your convenience.

Part c) Decrease the threshold voltages of the NMOSs in the pull-down network. You can change the effective threshold voltages of the NMOSs by adding a battery at the inputs in addition to the input voltages applied so that gate-overdrive $V_{GS} - V_T$ changes. You don't need to change the threshold voltage in the library. Use battery voltage, $V_B = 0.8$ V.

Repeat Part b). You can consider breaking down the 16-inputs in multiple cascaded stages as necessary. Explain why or why not. Draw and submit your final schematic (on paper by hand is OK if you don't use Cadence). Explain the differences in results with the Part b).