Homework 4 Solution

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 15-Oct-2009 Due: 22-Oct-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: Consider a 2-input static CMOS based NAND gate. Derive a plot of *delay-power trade-off* for the gate. Clearly present your procedure with *explanation* and state your assumptions, if any. For delay estimation you should consider the *worst case delay of a gate* and for power estimation you should consider the *time-average* dynamic power consumption. Use

V_{DD} = 2.5V, L = 300n,
Input signal period = 10n with 50% duty cycle, Rise/Fall time = 0.5n, Delay time = 1n.

Solution:

A gate has worst case rising and falling delays depending on the applied input vectors. Both the rising and falling delays are separately important as the critical path delay in a circuit is concerned that depends on the signal transitions (depending on the logic functions of the gates) along a path.

SPICE Code

```
* HW 4, Problem 1 Solution
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS
```

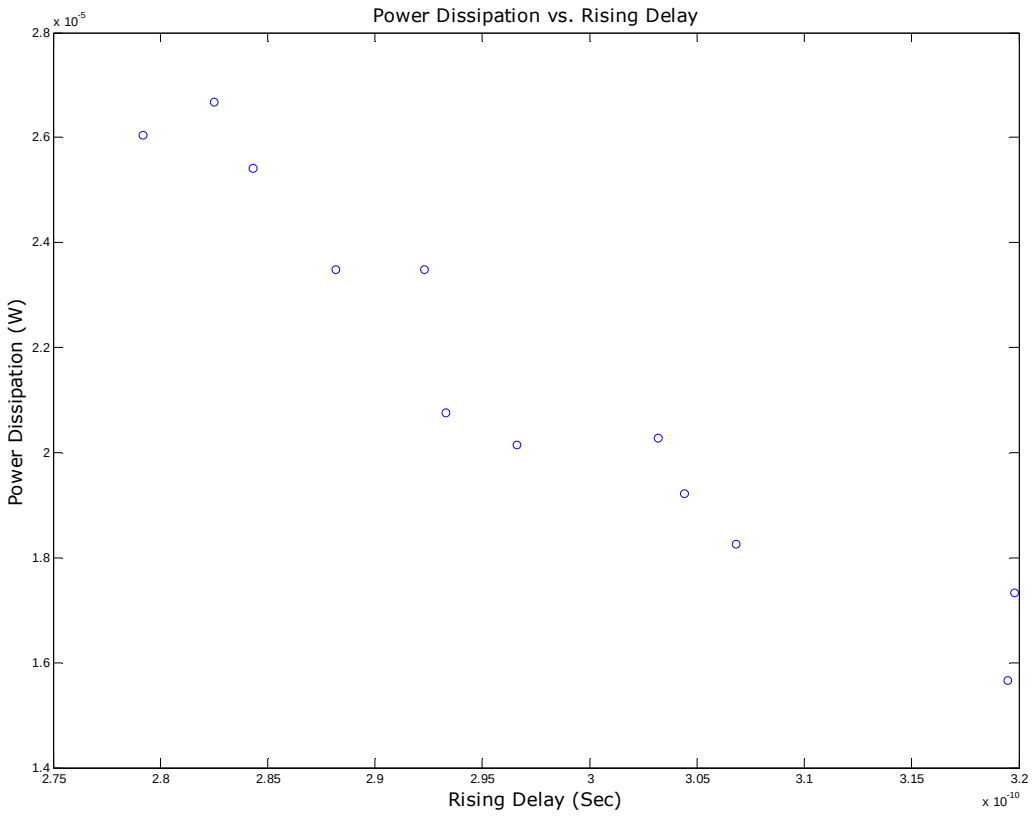
```
.PARAM VDD  = 2.5v
.PARAM VREF = 'VDD/2'
.PARAM L    = 300n

.PARAM WP   = 900n
.PARAM WN1  = 450n
.PARAM WN2  = 450n

* fanout of 4 is chosen
.PARAM WPF  = '8*WP'
.PARAM WNF  = '4*WN1'

.PARAM RT   = 0.5n
.PARAM FT   = 0.5n
.PARAM DT   = 1n
.PARAM ST   = 5n

.TEMP    25

.OPTION  POST

.DATA data1
 WN1 WN2 WP
 450n   450n    450n
 450n   450n    525n
 450n   450n    600n
 450n   450n    675n
 450n   450n    750n
 450n   450n    825n
 450n   450n    900n
 450n   450n    975n
* put all the set of data to be simulated
.ENDDATA

MP1 OUT IN1 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
```

```
MP2 OUT IN2 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1

MN1 OUT IN1 OUTX 0  TSMC25N  L='L' W='WN1'
+AD='WN1*2.5*L' AS='WN1*2.5*L' PD='2*WN1+5*L' PS='2*WN1+5*L'
+M=1

MN2 OUTX IN2 0 0  TSMC25N  L='L' W='WN2'
+AD='WN2*2.5*L' AS='WN2*2.5*L' PD='2*WN2+5*L' PS='2*WN2+5*L'
+M=1


MP3 OUT2 OUT VDD! VDD!  TSMC25P  L='L' W='WPF' AD='WPF*2.5*L' AS='WPF*2.5*L'
PD='2*WPF+5*L' PS='2*WPF+5*L' M=1
MN3 OUT2 OUT 0 0  TSMC25N  L='L' W='WNF' AD='WNF*2.5*L' AS='WNF*2.5*L'
PD='2*WNF+5*L' PS='2*WNF+5*L' M=1

* set initial condition for 00->11 transition, VDD-Vtn
.ic OUTX = 1.9882

.TRAN  1n 'ST*103' START=0 uic SWEEP DATA=data1

*.PRINT TRAN V(IN1) V(IN2) V(OUT) V(OUTX)

* 011 & 010 sequences are added at the beginning to get the worst case delays
* signal probability of 0.5 is assumed for both the inputs
VIN1  IN1  0 PAT (VDD 0 DT RT FT ST
b01110001000101010101010000000000010100000101010101000100000101000101010101
10001010001000100000000000010 r=0)
VIN2  IN2  0 PAT (VDD 0 DT RT FT ST
b01010100010101000001010000010001000001010100000000000100000101000000000101
10000000100010100010000001010 r=0)

VVDD! VDD! 0 DC=VDD

.MEASURE TRAN PROPAGATION_R
+ TRIG v(IN2)  VAL=VREF TD=DT FALL=1
```

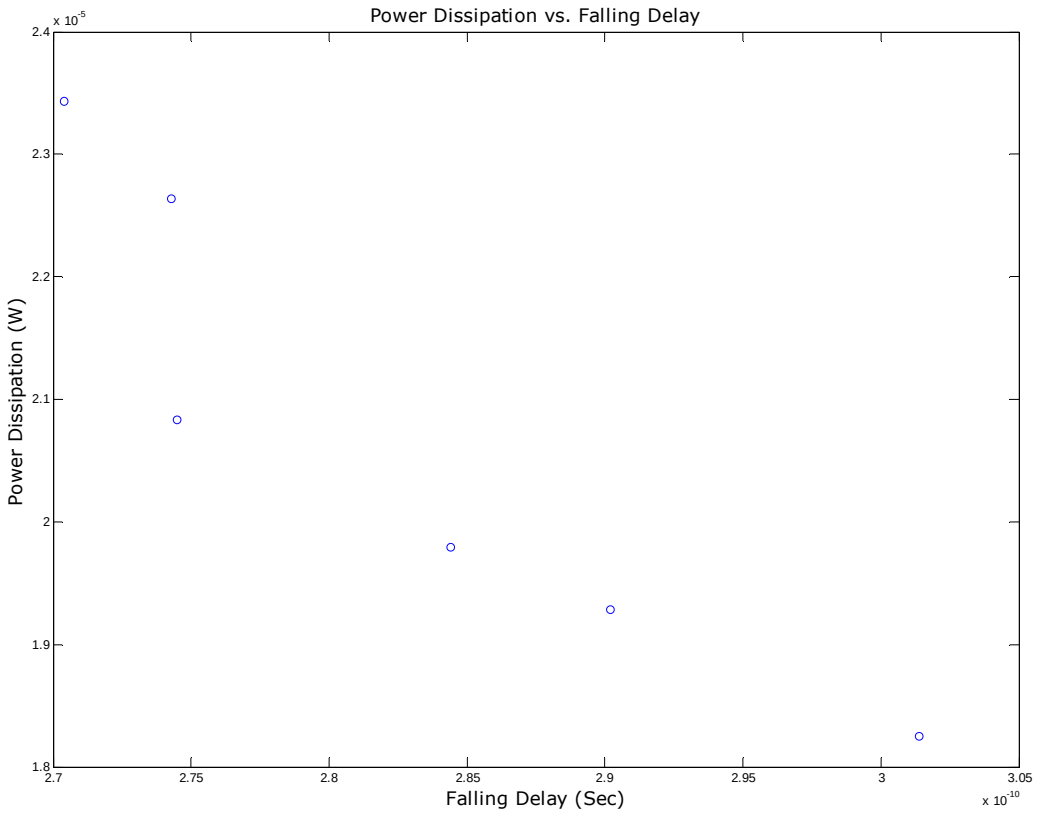
```
+ TARG v(OUT)  VAL=VREF TD=DT RISE=1

.MEASURE TRAN PROPAGATION_F
+ TRIG v(IN2)  VAL=VREF TD=DT RISE=1
+ TARG v(OUT)  VAL=VREF TD=DT FALL=1

.MEASURE TRAN MAX_PROPAGATION_DELAY
PARAM='MAX(PROPAGATION_R,PROPAGATION_F)'

.MEASURE TRAN AVG_POWER AVG POWER FROM=DT TO='ST*103'

.END
```

Results

The minimum worst case propagation delay is found for W_P=975nm, W_{N1}=450nm, W_{N2}=825nm. t_{plh}=3.068e-10 sec, t_{phl}=3.014e-10 sec, $power_{avg}$=1.825e-5 W.



In the figure above W_{N1}=450nm, W_{N2}=825nm and W_P is varied between 825nm to 1650nm in interval of 75nm. The values are chosen so that we don't have any huge asymmetry in the rising and falling delays reducing the noise margin of operation for a circuit. The points show the trade-off between delay and power as we see that if we have higher delay, we have lower power dissipation and vice-versa.



In the figure above W_P=975nm, W_{N2}=825nm and W_{N1} is varied between 450nm to 825nm in interval of 75nm. The values are chosen so that we don't have any huge asymmetry in the rising and falling delays reducing the noise margin of operation for a circuit. The points show the trade-off between delay and power as we see that if we have higher delay, we have lower power dissipation and vice-versa.

With the transistor widths and the rise/fall times given, we expect sharp changes in the transfer characteristics and hence the short-circuit power dissipation can be ignored compared to the dynamic power consumption. Since we are using 300 nm technology library, the leakage power also can be considered small enough compared to the dynamic power consumption.

Problem 2: Consider a 2-input static CMOS based NAND gate and a *dynamic* NAND gate (precharge-evaluation based). Perform a SPICE simulation to calculate the dynamic power consumption for both. State your assumptions, if any and *explain* your results comparatively discussing if it meets your expectation or not. Use

V_{DD} = 2.5V, L = 300n,
Wp = 900n, Wn = 450n (same Wp/Wn are also applicable for precharge/evaluate MOSs),
Input/Clock signal period = 10n with 50% duty cycle, Rise/Fall time = 0.5n, Delay time = 1n,
Signal probabilities: $p_{A=1}$= 0.6, $p_{B=1}$ = 0.6 (A is the input closer to the output).

Solution:

For dynamic logic based NAND2 gate we have less output node capacitance than that of the static NAND2 gate as we have one less PMOS transistor connected at the output node. Also since we have less output node capacitance for dynamic logic based NAND2 gate, we also expect it to drive less fanout gates' input capacitances. Accordingly, we may think of expecting less switching power dissipation for dynamic NAND2 gate than that of the static NAND2 gate.

However, for dynamic logic based gates, the signal transition probability at the output node does not depend on the history of the inputs, but rather on the signal probabilities.

For dynamic NAND2 gate, the switching activity,

$$\alpha_{1\to 0,dynamic} = \alpha_{0\to 1,dynamic} = p_{out=0} = p_{A=1} * p_{B=1} = 0.36$$

For static NAND2 gate, the switching activity

$$\alpha_{1\to 0,static} = \alpha_{0\to 1,static} = p_{out=0} * p_{out=1} = p_{A=1} * p_{B=1} * (1 - p_{A=1} * p_{B=1}) = 0.2304$$

Accordingly, the static NAND2 gate has quite lower switching activity than that of the corresponding dynamic counterpart. The input signals are assumed to be uncorrelated.

Based on the following discussion, we are not quite sure about the comparative nature of the power dissipations for static and dynamic NAND2 gates.

SPICE Code (Static NAND2 Gate)

```
* HW 4, Problem 2 Solution, static NAND2 gate
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!
```

```
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.PARAM VDD  = 2.5v
.PARAM L    = 300n

.PARAM WP   = 900n
.PARAM WN1  = 450n
.PARAM WN2  = 450n

* fanout of 4 is chosen
.PARAM WPF  = '8*WP'
.PARAM WNF  = '4*WN1'

.PARAM RT   = 0.5n
.PARAM FT   = 0.5n
.PARAM DT   = 1n
.PARAM ST   = 5n

.TEMP    25
.OPTION  POST

MP1 OUT IN1 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1

MP2 OUT IN2 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1

MN1 OUT IN1 OUTX 0  TSMC25N  L='L' W='WN1'
+AD='WN1*2.5*L' AS='WN1*2.5*L' PD='2*WN1+5*L' PS='2*WN1+5*L'
+M=1

MN2 OUTX IN2 0 0  TSMC25N  L='L' W='WN2'
+AD='WN2*2.5*L' AS='WN2*2.5*L' PD='2*WN2+5*L' PS='2*WN2+5*L'
+M=1
```

```
MP3 OUT2 OUT VDD! VDD! TSMC25P L='L' W='WPF' AD='WPF*2.5*L' AS='WPF*2.5*L' PD='2*WPF+5*L' PS='2*WPF+5*L' M=1
MN3 OUT2 OUT 0 0 TSMC25N L='L' W='WNF' AD='WNF*2.5*L' AS='WNF*2.5*L' PD='2*WNF+5*L' PS='2*WNF+5*L' M=1

.TRAN 1n 'ST*200' START=0

* 50% duty cycle inputs for ON period are used
* p(IN1=1)=0.6, p(IN2=1)=0.6
VIN1 IN1 0 PAT (VDD 0 DT RT FT ST
b1010001000101010001010001010100010001010101010001010100000100000101010100000100010100010001000100010101010001010001000101010001010000010100010000000000000001000100000001010101010000000001010101000101 0 r=0)
VIN2 IN2 0 PAT (VDD 0 DT RT FT ST
b0010101010101010001010100000100010101000001000101000101010101010101000100010101010100010100010101000101000101010001000101010101010101010100010001010101000101000101010001010100010100010101000101010100010101 0 r=0)

VVDD! VDD! 0 DC=VDD

.MEASURE TRAN AVG_POWER AVG POWER FROM=DT TO='ST*200'

.END
```

SPICE Code (Dynamic NAND2 Gate)

```
* HW 4, Problem 2 Solution, dynamic NAND2 gate
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.PARAM VDD = 2.5v
.PARAM L = 300n

.PARAM WPP = 900n
```

```
.PARAM WN1  = 450n
.PARAM WN2  = 450n
.PARAM WNE  = 450n

* fanout of 4 is chosen
.PARAM WPF  = '4*WPP'
.PARAM WNF  = '4*WN1'

.PARAM RT   = 0.5n
.PARAM FT   = 0.5n
.PARAM DT   = 1n
.PARAM ST   = 5n

.TEMP    25
.OPTION  POST

MPP OUT CLK VDD! VDD!  TSMC25P  L='L' W='WPP'
+AD='WPP*2.5*L' AS='WPP*2.5*L' PD='2*WPP+5*L' PS='2*WPP+5*L'
+M=1

MN1 OUT IN1 OUTX 0  TSMC25N  L='L' W='WN1'
+AD='WN1*2.5*L' AS='WN1*2.5*L' PD='2*WN1+5*L' PS='2*WN1+5*L'
+M=1

MN2 OUTX IN2 OUTXE 0  TSMC25N  L='L' W='WN2'
+AD='WN2*2.5*L' AS='WN2*2.5*L' PD='2*WN2+5*L' PS='2*WN2+5*L'
+M=1

MNE OUTXE CLK 0 0  TSMC25N  L='L' W='WNE'
+AD='WNE*2.5*L' AS='WNE*2.5*L' PD='2*WNE+5*L' PS='2*WNE+5*L'
+M=1

MP3  OUT2  OUT  VDD!  VDD!   TSMC25P   L='L'  W='WPF'  AD='WPF*2.5*L'  AS='WPF*2.5*L'
PD='2*WPF+5*L' PS='2*WPF+5*L' M=1
MN3  OUT2  OUT  0  0    TSMC25N    L='L'  W='WNF'  AD='WNF*2.5*L'  AS='WNF*2.5*L'
PD='2*WNF+5*L' PS='2*WNF+5*L' M=1

.TRAN  1n 'ST*200' START=0
```

```
VCLK  CLK  0 PAT (VDD 0 DT RT FT ST b10 r=100)

* 50% duty cycle inputs for ON period are used
* p(IN1=1)=0.6, p(IN2=1)=0.6
VIN1  IN1  0 PAT (VDD 0 DT RT FT ST
b1010001000101010001010001010100010001010101010001010100000100000101010100000
0100010100010001000100010101010001010001000101010001010000010100010000000000
0000010001000000010101010100000000010101010001010 r=0)
VIN2  IN2  0 PAT (VDD 0 DT RT FT ST
b0010101010101010001010100000100010101000001000101000101010101010101000100101
0001010100010101010001000101010101010101010100010001010101010001010001010100
0101000100010001010001010101010001010101000101010 r=0)

VVDD! VDD! 0 DC=VDD

.MEASURE TRAN AVG_POWER AVG POWER FROM=DT TO='ST*200'

.END
```

Results

For static case, we have average power dissipation: **2.2778E-05 W**
For dynamic case, we have average power dissipation: **1.7034E-05 W**

So, lower capacitance at the output node for the dynamic case is winning here. However, if we use the same fanout for the dynamic case as of the static counterpart, we have power dissipation for dynamic case: **2.8565E-05 W** that is higher than that of the static case. Accordingly, the trade-off between the *switching activity* and the *capacitance* is quite visible. So *switching capacitance* is after all important for considering the dynamic power consumption.

With the transistor widths and the rise/fall times given, we expect sharp changes in the transfer characteristics and hence the short-circuit power dissipation can be ignored compared to the dynamic power consumption. Since we are using 300 nm technology library, the leakage power also can be considered small enough compared to the dynamic power consumption.

Problem 3: Perform a DC analysis in SPICE for both an NMOS and a PMOS transistor to get their output characteristics (V_{DS} vs. I_D as a function of V_{GS}). From these two characteristics, derive the corresponding CMOS inverter's transfer characteristics and identify the regions of operation for each NMOS and PMOS along the input voltage range. Use V_{DD} = 2.5V, $V_{TH} = V_{TH0}$, L = 300n, Wp = 900n, Wn = 450n.

Solution:

The source is grounded for NMOS and the source for PMOS is connected to V_{DD}.

For NMOS, as V_G increases, the current through the device, I_{DN} increases. For PMOS, as V_G increases, V_{SG} decreases (as source is connected to V_{DD}) and hence the current through the device, $|I_{DP}|$ decreases.

HSPICE Code (for NMOS characteristics)

```
* HW 4, Problem 3, NMOS
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.PARAM VDD  = 2.5v
.PARAM L    = 300n
.PARAM WN   = 450n
.TEMP    25.00

.OPTION  NOMOD POST

MN1 D G 0 0  TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1

VD      D       0       VDD
VG      G       0       VDD
```

```
.DC VD 0 VDD 0.01 VG 0 VDD 0.01
.print DC V(G) I(MN1)

.END
```

HSPICE Code (for PMOS characteristics)

```
* HW 4, Problem 3, PMOS
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.PARAM VDD  = 2.5v
.PARAM L    = 300n
.PARAM WP   = 900n
.TEMP    25.00

.OPTION  NOMOD POST

MP1 D G VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1

VD      D       0       VDD
VG      G       0       VDD

VDD VDD! 0  VDD

.DC VD 0 VDD 0.01 VG 0 VDD 0.01
.print DC V(G) I(MP1)

.END
```

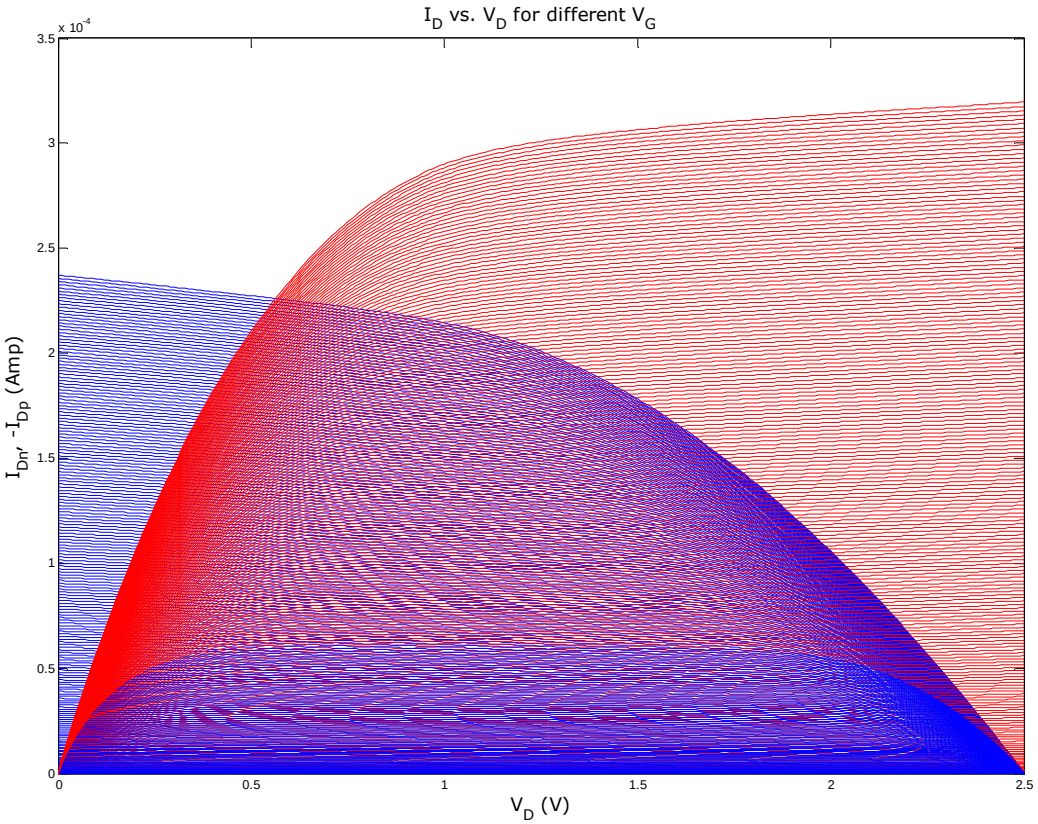
MATLAB Code (for parsing SPICE output)

```
%=====================================
% HW4, Problem 3
% by Kuntal Roy
% ECE 557, Fall 2009, Purdue University
% 30-Oct-2009
%=====================================
close all
clear all

VD=0:0.01:2.5;
VG=0:0.01:2.5;

IDn = MOSCharacteristics('nmos.out', VG, VD, 134);
IDp = -MOSCharacteristics('pmos.out', VG, VD, 136);

% plot the output characteristics
figure
for vgi=1:length(VG)
    plot(VD, IDn(vgi, :), 'r');
    plot(VD, IDp(vgi, :), 'b');
    hold on;
end

% plot the transfer characteristics
figure
for vgi=1:length(VG)
    IDd = abs(IDn(vgi,:) - IDp(vgi,:));
    index = find(IDd == min(IDd));
    plot(VG(vgi), VD(index), 'o');
    hold on
end
```

MATLAB Code (MOSCharacteristics.m)

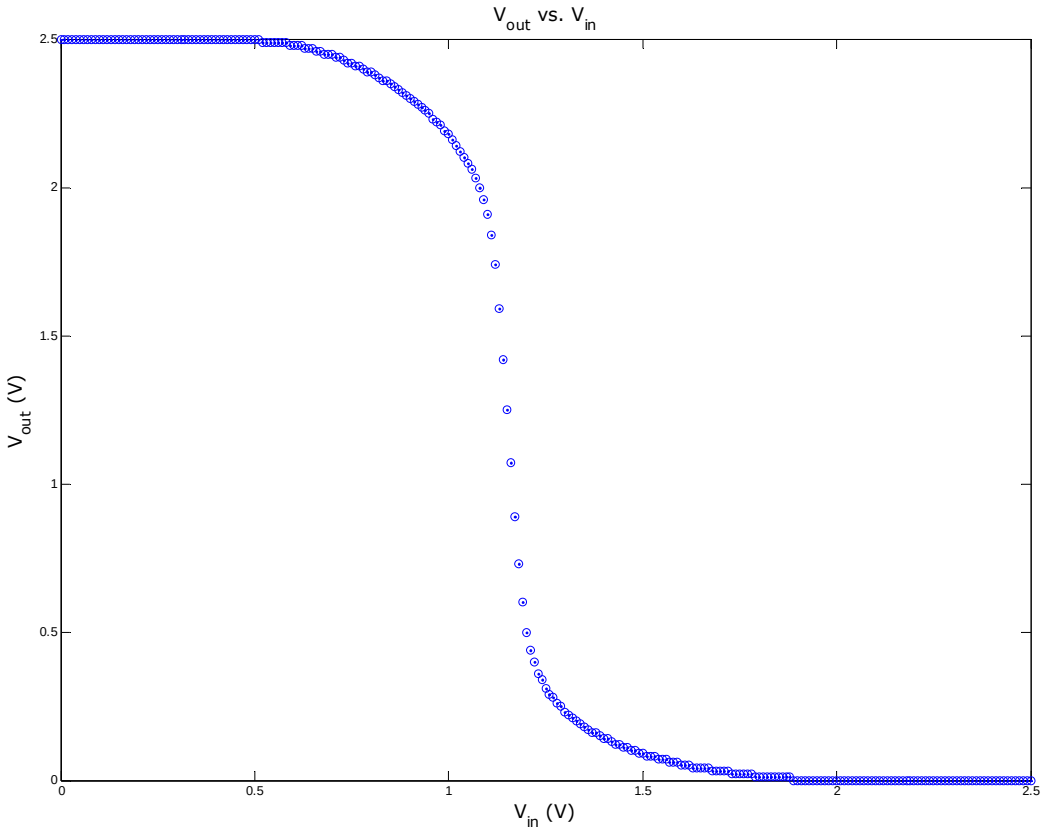
```
%=====================================
% HW4, Problem 3, MOSCharacteristics.m
% Parses the SPICE output file and
% returns the current through the device
% by Kuntal Roy
% ECE 557, Fall 2009, Purdue University
% 30-Oct-2009
%=====================================

function ID = MOSCharacteristics(filename, VG, VD, headerlines)

fid = fopen(filename, 'r');

% read the initial lines before starting of the simulation
for i=1:headerlines
```

```
    fgets(fid);
end

ID = zeros(length(VG), length(VD));

for vgi=1:length(VG)

    % read the initial lines for each simulation
    for i=1:11
        fgets(fid);
    end

    % read the simulation results
    for vdi=1:length(VD)
        fscanf(fid, '%s', 1); % vd values, we know it alread from VD
        fscanf(fid, '%s', 1); % vg values, we know it alread from VG
        ss = fscanf(fid, '%s', 1);

        multiplier = 1;
        switch ss(length(ss):length(ss)) % get the last character
            case  'm'
                multiplier = 1e-3;
            case  'u'
                multiplier = 1e-6;
            case  'n'
                multiplier = 1e-9;
            case  'p'
                multiplier = 1e-12;
            case  'f'
                multiplier = 1e-15;
            case  'a'
                multiplier = 1e-18;
        end

        ID(vgi, vdi) = str2double(ss(1:length(ss)-1))*multiplier;
    end

    % read the last lines for each simulation
    for i=1:4
        fgets(fid);
    end
end

fclose(fid);
```



The “red” curves (or the curves for which we have more current) are for the NMOS transistor while the “blue” curves (or the curves for which we have less current) are for the PMOS transistor.

Note that the family of curves for PMOS device does not quite correspond to the PMOS output characteristics as the curves are plotted with respect to V_D instead of V_{DS}. However as the source is connected to V_{DD}, the output characteristics would be just a shifted version of what is shown. Since we need to derive the transfer characteristics of an inverter, we need to equate the currents through the NMOS and the PMOS for same V_{in} and then we need to find out the corresponding V_{out} (i.e., V_D).



From the PMOS and NMOS models that we are using, we can get (from tsmc25N, tsmc25P – VTH0 parameter)

$V_{TH0,\ NMOS}$ = 0.4308936 V.
$V_{TH0,\ PMOS}$ = -0.6158735 V.

Also, for mobility values, from the U0 parameters for PMOS and NMOS models, we get

mun0 = 455.3 cm^2/V-S.
mup0 = 158.7 cm^2/V-S.

We are using some easy-to-get first order approximated values for the aforesaid parameters.

Solving by MATLAB when both the transistors are in saturation, we get V_{in} = **1.0921 V.**

MATLAB Code

```
mun0 = 455.3;
mup0 = 158.7;

wp = 900;
wn = 450;

vtn0 = 0.4308936;
vtp0 = -0.6158735

vin_ss = fsolve(@(x) mup0*wp*((x-2.5-vtp0)^2) - mun0*wn*((x-vtn0)^2), 1.25)
```

The regions of operation for the PMOS and NMOS along the voltage range are given below.

Condition	PMOS	NMOS
$0 \le V_{in} \le 0.4309$	linear	cut-off
$0.4309 \le V_{in} \le 1.0921$	linear	saturated
$V_{in} = 1.0921$	saturated	saturated
$1.0921 \le V_{in} \le 1.8841$	saturated	linear
$1.8841 \le V_{in} \le 2.5$	cut-off	linear