Homework 4

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 15-Oct-2009 Due: 22-Oct-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: Consider a 2-input static CMOS based NAND gate. Derive a plot of *delay-power trade-off* for the gate. Clearly present your procedure with *explanation* and state your assumptions, if any. For delay estimation you should consider the *worst case delay of a gate* and for power estimation you should consider the *time-average* dynamic power consumption. Use

V_{DD} = 2.5V, L = 300n,
Input signal period = 10n with 50% duty cycle, Rise/Fall time = 0.5n, Delay time = 1n.

Problem 2: Consider a 2-input static CMOS based NAND gate and a *dynamic* NAND gate (precharge-evaluation based). Perform a SPICE simulation to calculate the dynamic power consumption for both. State your assumptions, if any and *explain* your results comparatively discussing if it meets your expectation or not. Use

V_{DD} = 2.5V, L = 300n,
Wp = 900n, Wn = 450n (same Wp/Wn are also applicable for precharge/evaluate MOSs),
Input/Clock signal period = 10n with 50% duty cycle, Rise/Fall time = 0.5n, Delay time = 1n,
Signal probabilities: $p_{A=1}$= 0.6, $p_{B=1}$ = 0.6 (A is the input closer to the output).

Problem 3: Perform a DC analysis in SPICE for both an NMOS and a PMOS transistor to get their output characteristics (V_{DS} vs. I_D as a function of V_{GS}). From these two characteristics, derive the corresponding CMOS inverter's transfer characteristics and identify the regions of operation for each NMOS and PMOS along the input voltage range. Use V_{DD} = 2.5V, V_{TH} = V_{TH0}, L = 300n, Wp = 900n, Wn = 450n.