Homework 3 Solution

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 06-Oct-2009 Due: 15-Oct-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: For a gate if we increase the widths of the transistors, the corresponding propagation delays get decreased first but if you continue to increase the widths, you will find that the propagation delays get increased eventually.

Part a) Explain why does it happen.

Perform SPICE simulations for a simple CMOS inverter with the libraries that you have used in lab, i.e., *tsmc25N* and *tsmc25P* to confirm your answer. Use L = 300 nm, V_{DD} = 2.5 V.

Part b) A gate has *rising* and *falling* propagation delays. Also a gate with more than one input can have different rising and falling propagation delays depending on different input vector combinations applied to the inputs of the gate. Consider a 2-input NAND gate. Explain for which input combinations, the *maximum rising* and the *maximum falling* delays occur.

Perform SPICE simulation with the libraries that you have used in lab, i.e., *tsmc25N* and *tsmc25P* to confirm your answer. Use L = 300 nm, V_{DD} = 2.5 V.

Part c) Find out the *optimum widths of the transistors* so that the *maximum input-to-output propagation delay for a 2-input NAND gate* is *minimized*. Clearly explain the procedure you have followed. Submit the necessary plots showing the trade-off between propagation delays and transistor widths.

Solution

Part a)

As the width of a transistor in a gate is increased, the corresponding ON current increases. Accordingly, the corresponding propagation delay decreases. But the capacitance also increases

proportionally with the increase of the transistor width at the output node (as well as at the internal nodes, if any). Increase of capacitance attributes to the increase of propagation delay (for an inverter both the high-to-low and low-to-high propagation delays are increased as the output node capacitance increases). However, for example, for an inverter if PMOS transistor width is increased, the increase of low-to-high propagation delay due to the increase of output node capacitance *can* get compensated due to the increase of ON current and the trend will depend on the libraries/models you are using. Accordingly, a trade-off is expected to happen for some configuration of the transistors widths in a gate beyond which the propagation delay decreases with the increase of transistor widths due to the increase of ON current and over which the propagation delay increases because of the increase of capacitances. We can use the average of the high-to-low and low-to-high propagation delays since it captures both the increase of ON current and the increase of capacitance with the increase of transistor widths.

The cadence technology library that we are using restricts us to keep a 75 nm difference between two consecutive widths. So we need to choose the set of values in the .DATA statement (in the HSPICE netlist) accordingly.

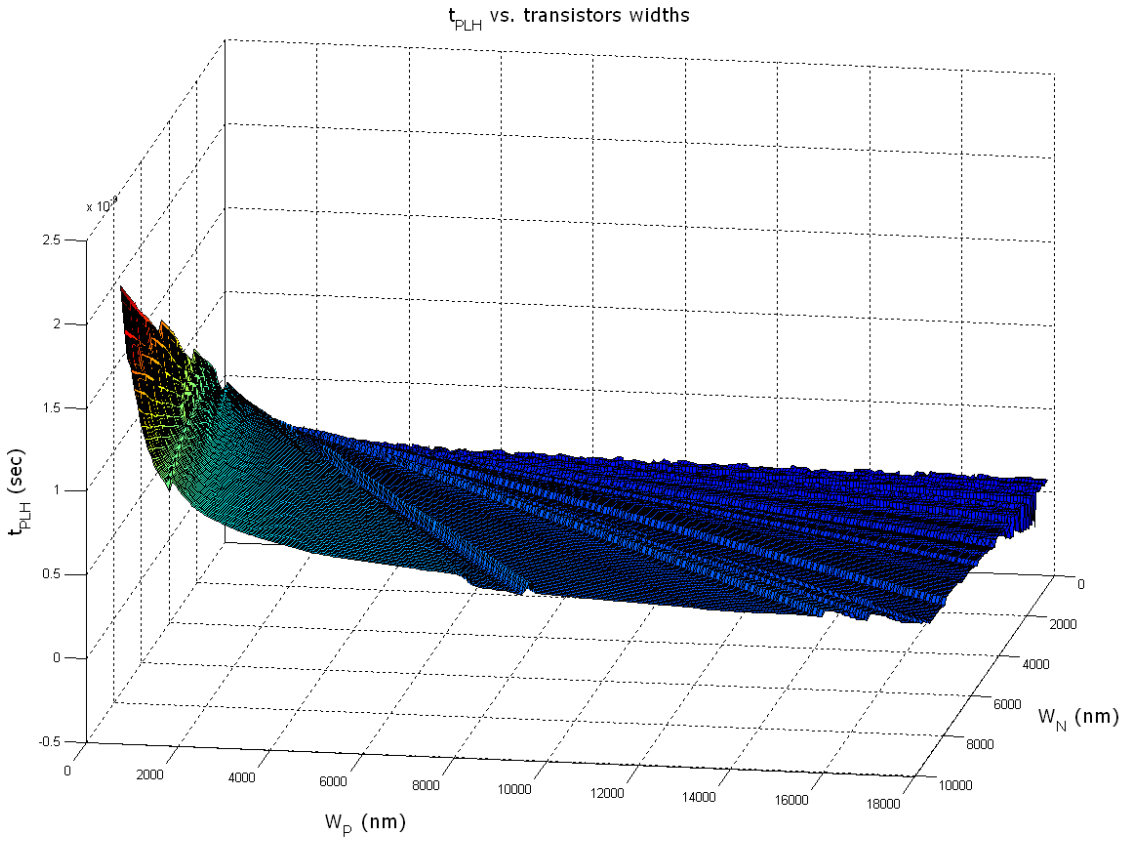
HSPICE Code

```
* HW 3, Problem 1 Part a) Solution
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.PARAM VDD  = 2.5v
.PARAM VREF = 1.25v
.PARAM L    = 300n

.PARAM WP   = 450n
.PARAM WN   = 450n

* fanout of 4 is chosen
.PARAM WPF  = '4*WP'
.PARAM WNF  = '4*WN'

.TEMP    25.0000
```

```
.OPTION  POST

* set of data for simulation
.DATA data1
 WN WP
 450n   450n
 450n   525n
 450n   600n
 450n   675n
* put all set of values that you want to simulate
.ENDDATA

MP1 OUT IN VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L' M=1
MN1 OUT IN 0 0  TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L' M=1
MP2  OUT2  OUT  VDD!  VDD!  TSMC25P  L='L'  W='WPF'  AD='WPF*2.5*L'  AS='WPF*2.5*L'
PD='2*WPF+5*L' PS='2*WPF+5*L' M=1
MN2  OUT2  OUT  0  0  TSMC25N  L='L'  W='WNF'  AD='WNF*2.5*L'  AS='WNF*2.5*L'
PD='2*WNF+5*L' PS='2*WNF+5*L' M=1

.TRAN  1n 40n START=0 SWEEP DATA=data1
VIN IN 0 PULSE 0 2.5v  1n 1n 1n 20n 40n
VVDD! VDD! 0 DC=VDD

.MEASURE TRAN PROPAGATION_R
+ TRIG v(IN)   VAL=VREF TD=1n FALL=1
+ TARG v(OUT)  VAL=VREF TD=1n RISE=1

.MEASURE TRAN PROPAGATION_F
+ TRIG v(IN)   VAL=VREF TD=1n RISE=1
+ TARG v(OUT)  VAL=VREF TD=1n FALL=1

.MEASURE TRAN PROPAGATION_DELAY PARAM='(PROPAGATION_R+PROPAGATION_F)/2'
.END
```

Note:

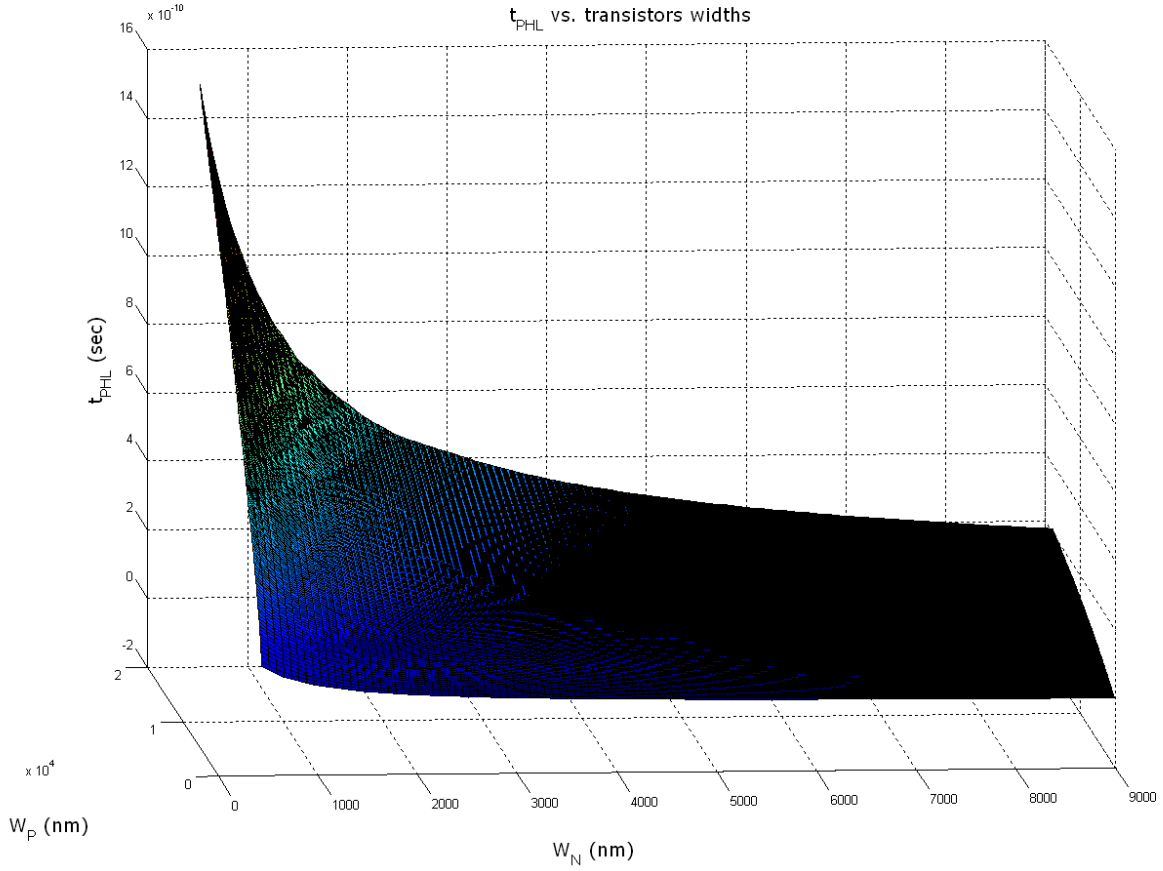
The simulation output will be stored in the *<spice filename>.mt0* file in a tabular format. You can use MATLAB's *surf* function to draw your plots.



The figure above shows the variation of low-to-high propagation delay (t_{PLH}) for an inverter as a function of Wp and Wn both. We can observe that with the increase of Wp, the t_{PLH} decreases as expected because of the increase of ON current.

We can also observe that as Wn increases, t_{PLH} also increases. The reason behind is that with the increase of Wn, the output node capacitance increases and during the low-to-high transition, the increased capacitance results in an increased propagation delay.

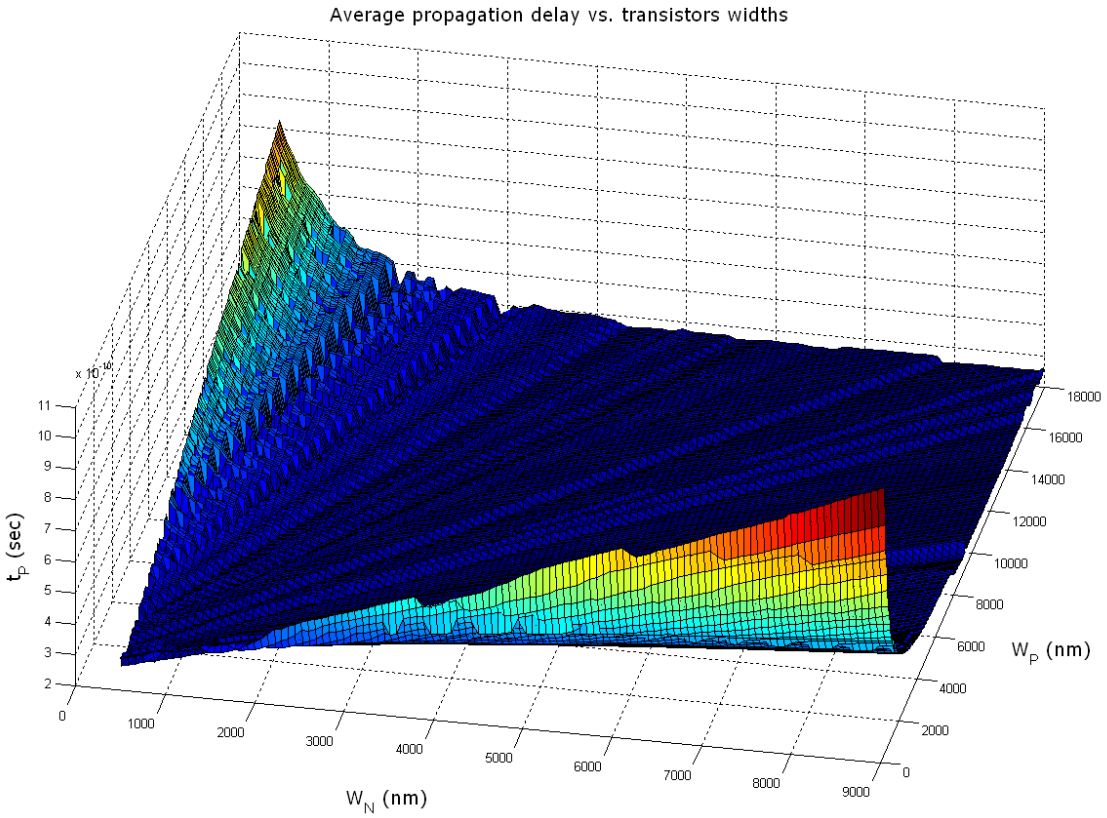
So it quite looks like that both the increased ON current and increased capacitance are playing a role for the determination of low-to-high propagation delay (t_{PLH}).



The figure above shows the variation of high-to-low propagation delay (t_{PHL}) for an inverter as a function of Wp and Wn both. We can observe that with the increase of Wn, the t_{PHL} decreases as expected because of the increase of ON current.

We can also observe that as Wp increases, t_{PHL} also increases. The reason behind is that with the increase of Wp, the output node capacitance increases and during the high-to-low transition, the increased capacitance results in an increased propagation delay.

So it quite looks like that both the increased ON current and increased capacitance are playing a role for the determination of low-to-high propagation delay (t_{PHL}).



The figure above shows the variation of average propagation delay, $(t_{PHL} + t_{PLH})/2$ for an inverter as a function of Wp and Wn both. We will consider the following four cases.

1) *Wp and Wn both are small*: In this case we have lower ON current but also the capacitances are small. So we expect lower propagation delays.

2) *Wp and Wn both are high*: In this case we have higher ON current but also the capacitances are higher. So we expect lower propagation delays.

3) *Wp is high and Wn is small*: In this case we will have lower t_{PLH} but higher t_{PHL}. The average value will depend on the exact values of Wn and Wp.

4) *Wp is low and Wn is high*: In this case we will have higher t_{PLH} but lower t_{PHL}. The average value will depend on the exact values of Wn and Wp.

Part b)

Let us consider a 2-input NAND gate with inputs A and B. *A is the input to the transistor that is closer to the output of the gate*.

For low-to-high propagation delay, we can have three scenarios as follows.

1) *B = 1, A makes transition from high-to-low:* The pull up PMOS device has to charge only the output node capacitance.

2) *A = 1, B makes transition from high-to-low:* The pull up PMOS device has to charge both the output node capacitance and the internal node capacitance.

3) *Both inputs make transition from high-to-low:* The effective resistance of the two parallel ON PMOS devices is halved than that of the cases when only one PMOS device is ON. So the corresponding propagation delay is expected to reduce around half-times.

According to the above discussion, the 2nd case when *A = 1, B makes transition from high-to-low* is expected to incur a higher low-to-high propagation delay.

For high-to-low propagation delay, we can have three scenarios as follows.

1) *B = 1, A makes transition from low-to-high:* The pull up PMOS device has to discharge only the output node capacitance.

2) *A = 1, B makes transition from low-to-high:* The pull up PMOS device has to discharge both the output node capacitance and the internal node capacitance.

3) *Both inputs make transition from low-to-high:* In this case it is necessary to consider the state of the internal node in the NMOS network. The worst case happens when the internal node charges up to V_{DD} - V_{Tn} that has to be ensured by setting an initial condition of the internal node during simulation. Also when initially both the inputs are at *low* values, the *output high value* is expected to be at higher value than that of the cases when only one input is at *low* values, so a higher voltage at the output node has to be brought down to *low*.

According to the above discussion, the 3rd case when b*oth inputs make transition from low-to-high* is expected to incur a higher high-to-low propagation delay.

HSPICE Code

```
**** NAND2 maximum rising and falling delays *****
* HW 3, Problem 1, Part b) Solution
* ECE 559, Fall 2009, Purdue University

.TEMP    25.0000
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.GLOBAL VDD!

.PARAM VDD  = 2.5
.PARAM VREF = VDD/2
.PARAM L    = 300n
.PARAM WP   = 900n
.PARAM WN   = 450n

* using FO4
.PARAM WPF  = '8*WP'
.PARAM WNF  = '4*WN'

.PARAM RT   = 0.1n
.PARAM FT   = 0.1n

.OPTION POST

MP1 OUT  IN1 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MP2 OUT  IN2 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1
MN1 OUT  IN1 OUTX 0           TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
+M=1
MN2 OUTX IN2 0          0       TSMC25N  L='L' W='WN'
+AD='WN*2.5*L' AS='WN*2.5*L' PD='2*WN+5*L' PS='2*WN+5*L'
```

```
+M=1

MP3 OUT2 OUT VDD! VDD!  TSMC25P  L='L' W='WPF'
+AD='WPF*2.5*L' AS='WPF*2.5*L' PD='2*WPF+5*L' PS='2*WPF+5*L'
+M=1
MN3 OUT2 OUT 0 0  TSMC25N  L='L' W='WNF'
+AD='WNF*2.5*L' AS='WNF*2.5*L' PD='2*WNF+5*L' PS='2*WNF+5*L'
+M=1

VVDD! VDD! 0 DC=VDD
VIN1  IN1  0 PAT (VDD 0 1n RT FT 5n b0101110 r=0)
VIN2  IN2  0 PAT (VDD 0 1n RT FT 5n b0111010 r=0)

* expected values
VIO    IO  0 PAT (VDD 0 1n RT FT 5n b1010101 r=0)

* set initial condition for 00->11 transition, VDD-Vtn
.ic OUTX = 1.9882

.tran 1n 35n uic
.print tran v(IN1) v(IN2) v(IO) v(OUT) v(OUTX)

* measuring the rising delays
.measure tran propagation_r_11_01
+ TRIG v(IO)   VAL=VREF TD=1n RISE=1
+ TARG v(OUT)  VAL=VREF TD=1n RISE=1

.measure tran propagation_r_11_10
+ TRIG v(IO)   VAL=VREF TD=1n RISE=2
+ TARG v(OUT)  VAL=VREF TD=1n RISE=2

.measure tran propagation_r_11_00
+ TRIG v(IO)   VAL=VREF TD=1n RISE=3
+ TARG v(OUT)  VAL=VREF TD=1n RISE=3

* measuring the falling delays
.measure tran propagation_f_00_11
+ TRIG v(IO)   VAL=VREF TD=1n FALL=1
```

```
+ TARG v(OUT)  VAL=VREF TD=1n FALL=1

.measure tran propagation_f_01_11
+ TRIG v(IO)   VAL=VREF TD=1n FALL=2
+ TARG v(OUT)  VAL=VREF TD=1n FALL=2

.measure tran propagation_f_10_11
+ TRIG v(IO)   VAL=VREF TD=1n FALL=3
+ TARG v(OUT)  VAL=VREF TD=1n FALL=3

.END
```

Results

Rising Delays

propagation_r_11_01 (A = 1→0, B = 1) : 2.1521E-10

propagation_r_11_10 (A = 1, B = 1→0) : 2.4040E-10 **(maximum)**

propagation_r_11_00 (A = B = 1→0) : 1.1053E-10

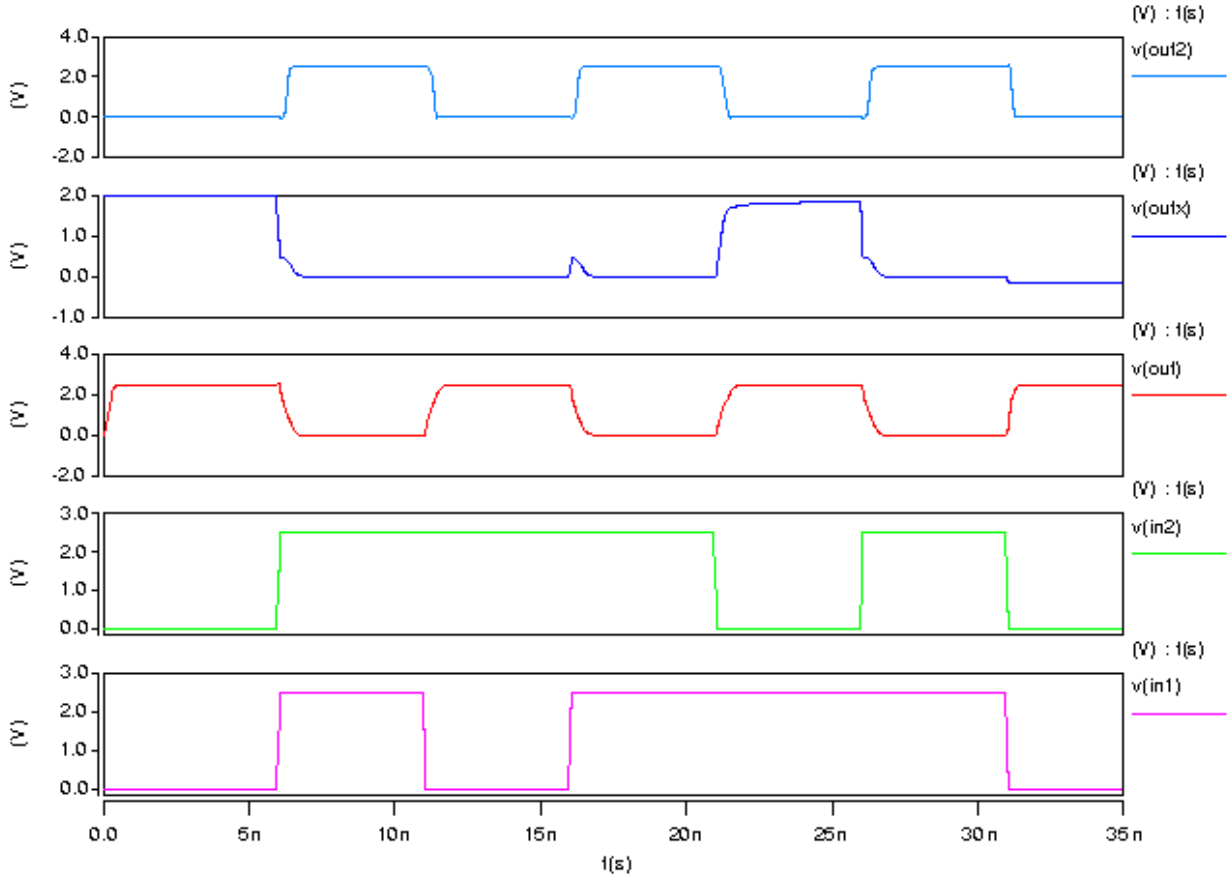
Falling Delays

propagation_f_00_11 (A = B = 0→1) : 2.4176E-10 **(maximum)**

propagation_f_01_11 (A = 0→1, B = 1) : 2.0978E-10

propagation_f_10_11 (A = 1, B = 0→1) : 2.2598E-10

Waveform



Part c)

In this case we have a 2-input NAND gate and correspondingly we have *four* parameters (corresponding to *four* transistors) in the design space. We can use the same widths for the two PMOS transistors as the two are connected in parallel. However, since the two NMOS transistors in the pull-down network are connected in series, we cannot quite choose the same widths for the two NMOS transistors. So we end up in choosing three parameters in design space.

From the part b) answer we know the worst case input vector transitions for the rising and falling delays. So we can consider only the worst case input vectors during simulation. We need to choose the *maximum* of the rising and falling propagation delays for all the simulated points. At last it needs to get the *minimum* value of the maximum propagation delays that will correspond to some configuration of the transistor widths in the NAND gate.

The cadence technology library that we are using restricts us to keep a 75 nm difference between two consecutive widths. So we need to choose the set of values in the .DATA statement (in the HSPICE netlist) accordingly.

HSPICE Code

```
* HW 3, Problem 1, part c) Solution
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

.PARAM VDD  = 2.5v
.PARAM VREF = 1.25v
.PARAM L    = 300n

.PARAM WP   = 450n
.PARAM WN1  = 450n
.PARAM WN2  = 450n

* fanout of 4 is chosen
.PARAM WPF  = '8*WP'
.PARAM WNF  = '4*WN1'

.PARAM RT   = 1n
.PARAM FT   = 1n

.TEMP    25.0000

.OPTION  POST

.DATA data1
 WN1 WN2 WP
450n    450n    450n
450n    450n    525n
```

```
450n    450n    600n
450n    450n    675n
450n    450n    750n
450n    450n    825n
450n    450n    900n
450n    450n    975n
* put all set of values that you want to simulate
.ENDDATA

MP1 OUT IN1 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1

MP2 OUT IN2 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD='WP*2.5*L' AS='WP*2.5*L' PD='2*WP+5*L' PS='2*WP+5*L'
+M=1

MN1 OUT IN1 OUTX 0  TSMC25N  L='L' W='WN1'
+AD='WN1*2.5*L' AS='WN1*2.5*L' PD='2*WN1+5*L' PS='2*WN1+5*L'
+M=1

MN2 OUTX IN2 0 0  TSMC25N  L='L' W='WN2'
+AD='WN2*2.5*L' AS='WN2*2.5*L' PD='2*WN2+5*L' PS='2*WN2+5*L'
+M=1

MP3 OUT2 OUT VDD! VDD!  TSMC25P  L='L' W='WPF' AD='WPF*2.5*L' AS='WPF*2.5*L'
PD='2*WPF+5*L' PS='2*WPF+5*L' M=1
MN3 OUT2 OUT 0 0  TSMC25N  L='L' W='WNF' AD='WNF*2.5*L' AS='WNF*2.5*L'
PD='2*WNF+5*L' PS='2*WNF+5*L' M=1

* set initial condition for 00->11 transition, VDD-Vtn
.ic OUTX = 1.9882

.TRAN  1n 30n START=0 uic SWEEP DATA=data1

*.PRINT TRAN V(IN1) V(IN2) V(OUT) V(OUTX)

VIN1  IN1  0 PAT (VDD 0 0n RT FT 10n b011 r=0)
```

```
VIN2  IN2  0 PAT (VDD 0 0n RT FT 10n b010 r=0)

VVDD! VDD! 0 DC=VDD

.MEASURE TRAN PROPAGATION_R
+ TRIG v(IN2)  VAL=VREF TD=1n FALL=1
+ TARG v(OUT)  VAL=VREF TD=1n RISE=1

.MEASURE TRAN PROPAGATION_F
+ TRIG v(IN2)  VAL=VREF TD=1n RISE=1
+ TARG v(OUT)  VAL=VREF TD=1n FALL=1

.MEASURE TRAN MAX_PROPAGATION_DELAY
PARAM='MAX(PROPAGATION_R,PROPAGATION_F)'

.END
```

Results

W_{N1} = 450 nm (N1 is the transistor closer to the output of the gate)

W_{N2} = 975 nm

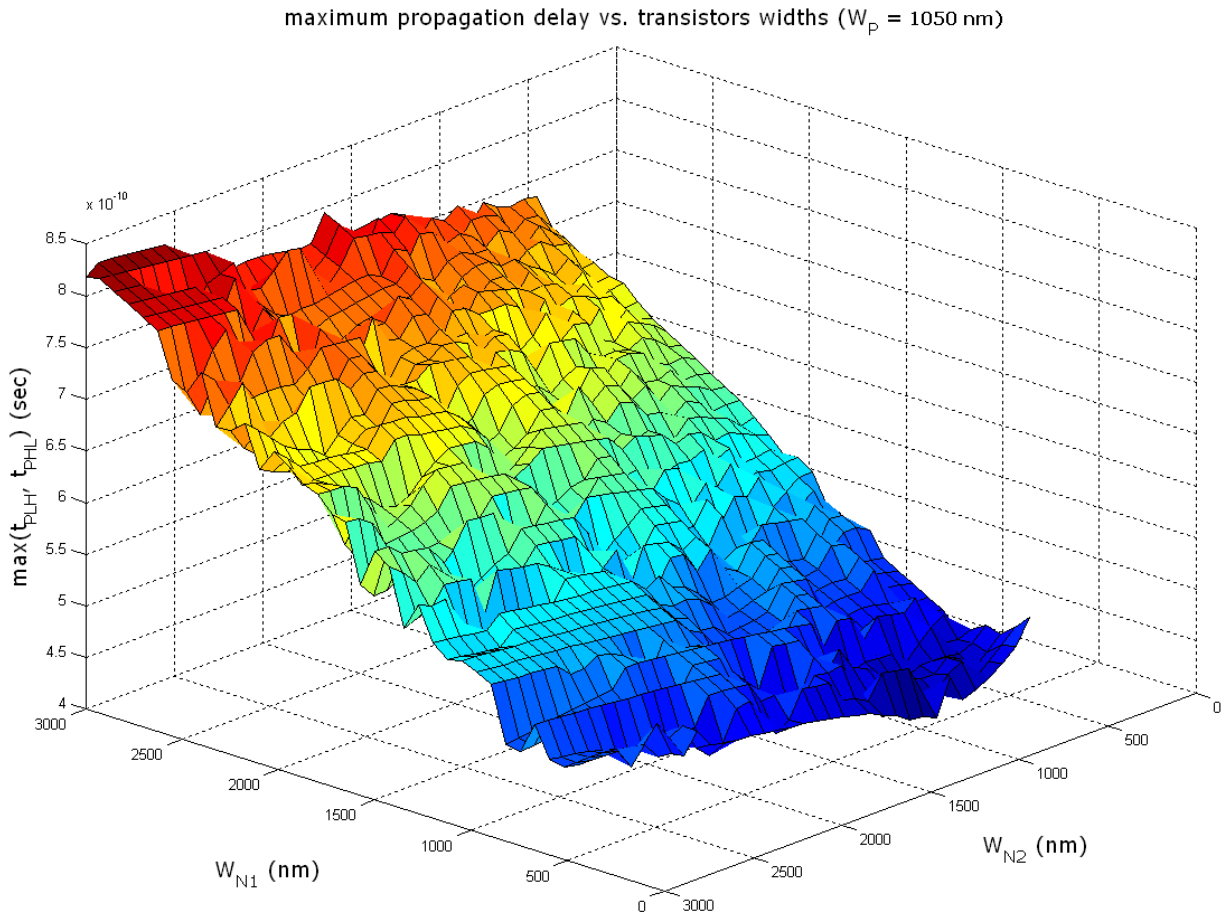
W_P = 1050 nm

t_{PLH} = 4.0920e-010 sec

t_{PHL} = 4.1110e-010 sec

$t_{P.max}$ = max(t_{PLH}, t_{PHL}) = 4.1110e-010 sec

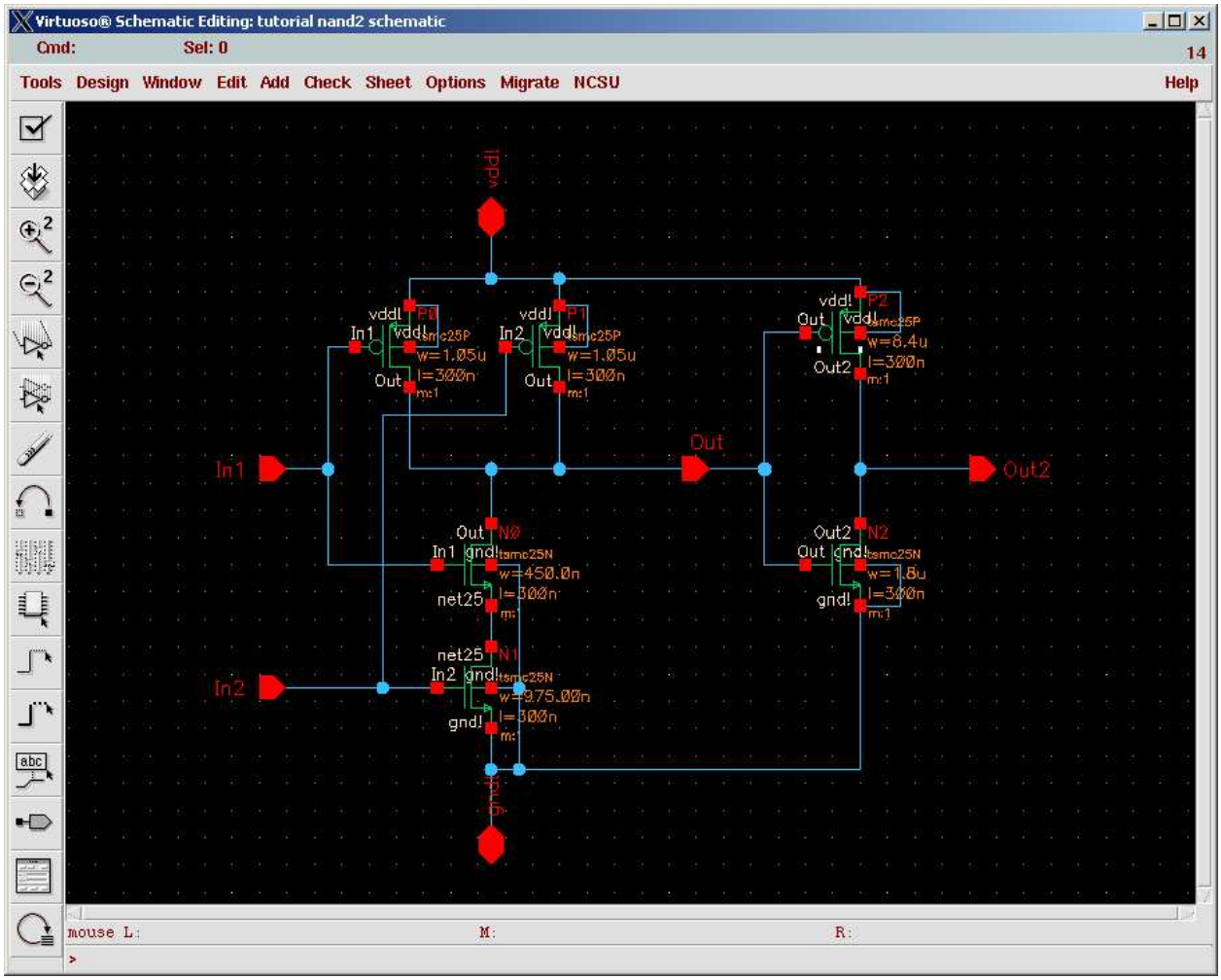
The reason behind having $W_{N2} > W_{N1}$ is quite prominent. If we consider the Elmore delay model for the pull-down network, we can easily see that the resistance of the bottom transistor comes multiple times in the delay expression. Minimizing the resistance (increasing its width) of the bottom transistor hence facilitates a lower delay that has been reflected in the SPICE simulation.



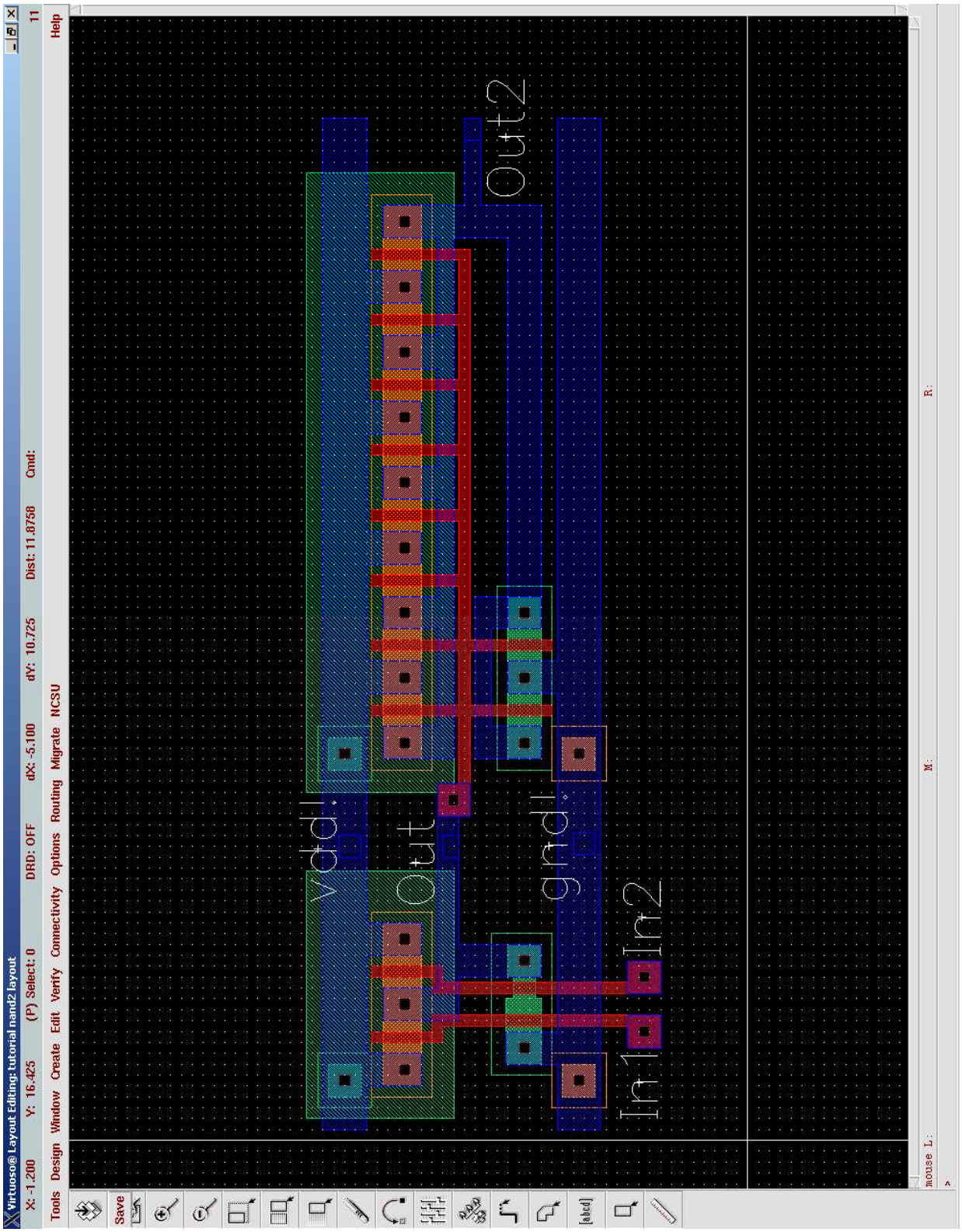
The figure above shows the maximum propagation delay as a function of W_{N1} and W_{N2} of the simulated NAND gate for Wp = 1050 nm. We can observe that when W_{N1} = W_{N2} = 450 nm, the delay is higher than that of the case of when W_{N1} = 450nm, W_{N2} = 975 nm. We should note that increasing the width of the transistor N2 decreases its resistance but consequently increases the capacitance. So again we can visualize the trade-off and we can choose the optimal transistor widths for propagation delay/performance accordingly.

Problem 2: Draw a layout of a 2-input NAND gate with the optimized widths that you have got for the problem 1. You can round the widths of the transistors as allowed by the technology library that you have used in lab. Perform DRC, extract layout, do layout vs. schematic check, and at last simulate your extracted netlist to verify its functionality. Submit the plots of schematic and layout of your design.

Schematic Diagram

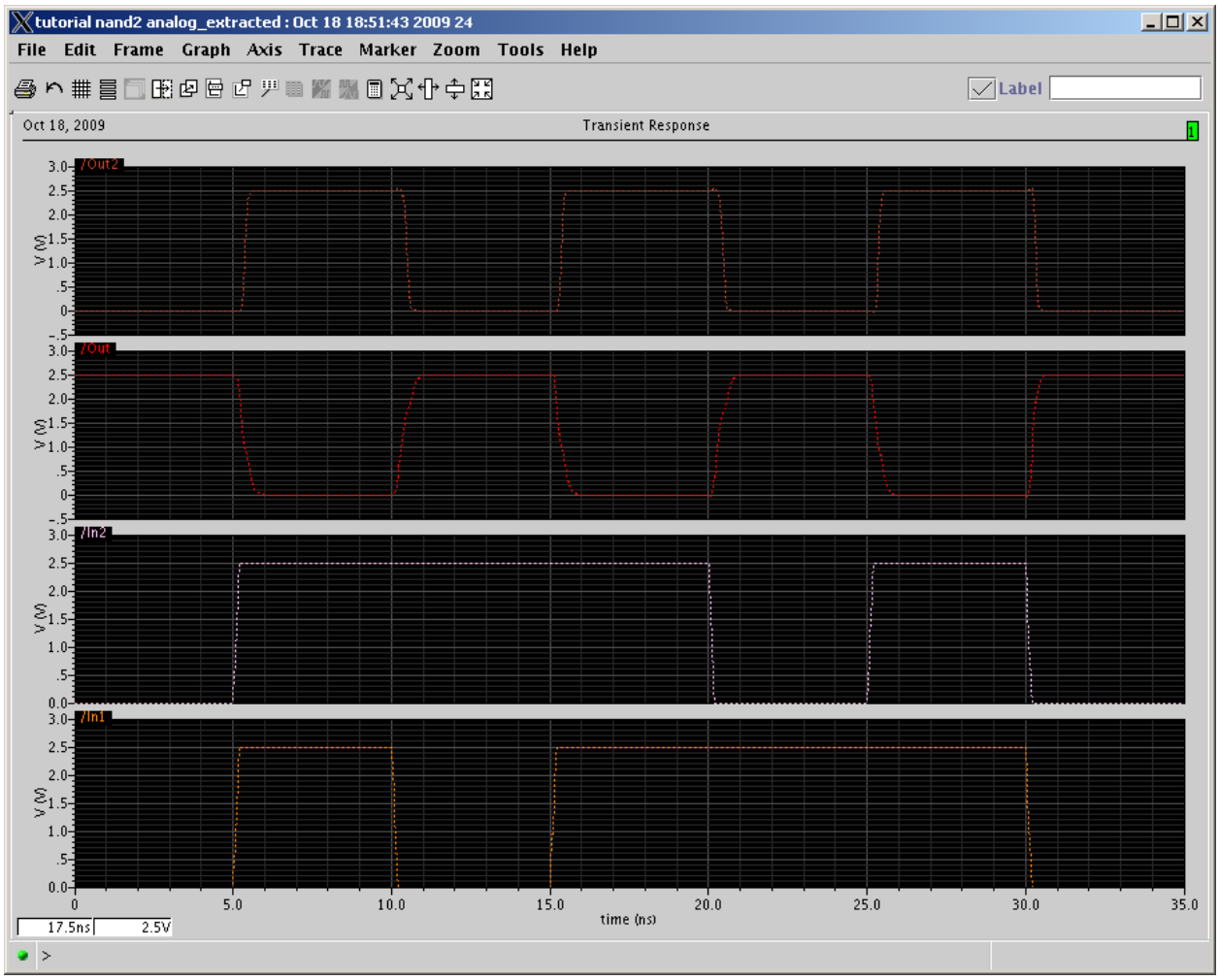


Layout

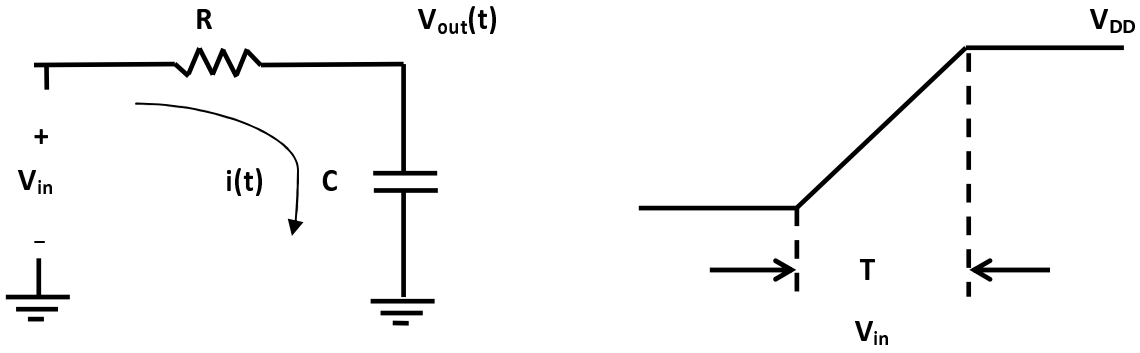

Virtuoso® Layout Editing: tutorial nand2 layout
X: -1.200 Y: 16.425 (P) Select: 0 DRD: OFF dX: -5.100 dY: 10.725 Dist: 11.8758 Cmd:
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate NCSU Help
Save
Out2
vdd!
Out
gnd!
In1
In2
Mouse L:
M:
R:

Note: We can do layout of the higher width transistors in a *multi-finger structure* as is done for the fanout inverter. It facilitates us to keep same spacing between VDD and GND in a row-based layout structure.

Post layout simulation and waveform



Problem 3: In the circuit given below, the input voltage, V_{in} varies as shown. Determine the energy dissipation when 1) RC >> T and 2) T >> RC, respectively.



$$V_{in} = 0 \qquad t \le 0$$
$$= \frac{V_{DD}}{T} t \qquad 0 \le t \le T$$
$$= V_{DD} \qquad t \ge T$$

To determine the total energy dissipation we have to consider the rise time of the input signal ($0 \le t \le T$) and the ON-period of the input signal separately as we will have different expressions for $V_{out}(t)$ and i(t) for the two cases.

Using KCL
$$C\frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R} = 0$$

Taking Laplace transform

$$RC\left(SV_{out}(s) - V_{out,init}\right) + V_{out}(s) - V_{in}(s) = 0$$
$$\Rightarrow (1 + SRC)V_{out}(s) = V_{in}(s) + RCV_{out,init}$$
$$\Rightarrow V_{out}(s) = \frac{V_{in}(s) + RCV_{out,init}}{(1 + SRC)}$$

$$For\ 0 \le t \le T,\ \ V_{out,init} = 0$$

$$V_{out}(s) = \frac{V_{in}(s)}{(1+SRC)} = \frac{V_{DD}}{T}\frac{1}{S^2(1+SRC)}$$

$$= \frac{V_{DD}}{T}\frac{1}{S}\left(\frac{1}{S} - \frac{1}{\left(S+\frac{1}{RC}\right)}\right) = \frac{V_{DD}}{T}\left(\frac{1}{S^2} - RC\left(\frac{1}{S} - \frac{1}{\left(S+\frac{1}{RC}\right)}\right)\right)$$

Taking inverse Laplace transform,

$$V_{out}(t) = \frac{V_{DD}}{T}\left(t - RC\left(1 - e^{-\frac{t}{RC}}\right)\right) \qquad for\ 0 \le t \le T$$

$$i(t) = C\frac{dV_{out}(t)}{dt} = C\frac{V_{DD}}{T}\left(1 - e^{-\frac{t}{RC}}\right) \qquad for\ 0 \le t \le T$$

$$For\ t \ge T,\ \ V_{out,init} = V_{out}(T) = V_{DD} - \frac{RC}{T}V_{DD}\left(1 - e^{-\frac{T}{RC}}\right)$$

$$V_{out}(s) = \frac{\frac{V_{DD}}{S} + RC\left(V_{DD} - \frac{RC}{T}V_{DD}\left(1 - e^{-\frac{T}{RC}}\right)\right)}{(1+SRC)}$$

$$= V_{DD}\left(\frac{1}{S} - \frac{1}{\left(S+\frac{1}{RC}\right)}\right) + \frac{V_{DD} - \frac{RC}{T}V_{DD}\left(1 - e^{-\frac{T}{RC}}\right)}{\left(S+\frac{1}{RC}\right)}$$

We have not considered any term like e^{-ST} for u(t-T), instead we would be using (t-T) in place of only 't' to signify the fact.

Taking inverse Laplace transform,

$$V_{out}(t) = V_{DD}\left(1-e^{-\frac{t-T}{RC}}\right)+\left(V_{DD}-\frac{RC}{T}V_{DD}\left(1-e^{-\frac{T}{RC}}\right)\right)e^{-\frac{t-T}{RC}}$$

$$= V_{DD}-\frac{RC}{T}V_{DD}\left(1-e^{-\frac{T}{RC}}\right)e^{-\frac{t-T}{RC}} \qquad for\ t \geq T$$

$$i(t) = C\frac{dV_{out}(t)}{dt} = C\frac{V_{DD}}{T}\left(1-e^{-\frac{T}{RC}}\right)e^{-\frac{t-T}{RC}} \qquad for\ t \geq T$$

$$E_{dissipated} = E_{supply} - E_{stored}$$

$$= \int_0^\infty i(t)v_{in}(t)dt - \int_0^\infty i(t)v_{out}(t)dt = \int_0^\infty i(t)\left(v_{in}(t)-v_{out}(t)\right)dt$$

$$= \int_0^T i(t)\left(v_{in}(t)-v_{out}(t)\right)dt + \int_T^\infty i(t)\left(v_{in}(t)-v_{out}(t)\right)dt$$

$$= \int_0^T i(t)V_{DD}\frac{RC}{T}\left(1-e^{-\frac{t}{RC}}\right)dt + \int_T^\infty i(t)V_{DD}\frac{RC}{T}\left(1-e^{-\frac{T}{RC}}\right)e^{-\frac{t-T}{RC}}dt$$

$$= \left(\frac{CV_{DD}}{T}\right)^2 R\left[\int_0^T\left(1-e^{-\frac{t}{RC}}\right)^2 dt + \left(1-e^{-\frac{T}{RC}}\right)^2\int_T^\infty e^{-\frac{2(t-T)}{RC}}dt\right]$$

$$= \left(\frac{CV_{DD}}{T}\right)^2 R\left\{\left[1+2RCe^{-\frac{t}{RC}}-\frac{RC}{2}e^{-\frac{2t}{RC}}\right]_0^T + \left(1-e^{-\frac{T}{RC}}\right)^2\left[-\frac{RC}{2}e^{-\frac{2(t-T)}{RC}}\right]_T^\infty\right\}$$

$$= \left(\frac{CV_{DD}}{T}\right)^2 R\left\{T-2RC\left(1-e^{-\frac{T}{RC}}\right)+\frac{RC}{2}\left(1-e^{-\frac{2T}{RC}}\right)+\left(1-e^{-\frac{T}{RC}}\right)^2\frac{RC}{2}\right\}$$

$$E_{dissipated}$$

$$= \left(\frac{CV_{DD}}{T}\right)^2 R\left\{T - 2RC\left(1 - e^{-\frac{T}{RC}}\right) + \frac{RC}{2}\left(1 - e^{-\frac{2T}{RC}}\right) + \left(1 - e^{-\frac{T}{RC}}\right)^2 \frac{RC}{2}\right\}$$

$$= \left(\frac{CV_{DD}}{T}\right)^2 R\left\{T - 2RC\left(1 - e^{-\frac{T}{RC}}\right) + RC - RCe^{-\frac{T}{RC}}\right\}$$

$$= \left(\frac{CV_{DD}}{T}\right)^2 R\left\{T - RC + RCe^{-\frac{T}{RC}}\right\}$$

$$= CV_{DD}{}^2\left(\frac{RC}{T}\right)\left\{1 - \frac{RC}{T} + \frac{RC}{T}e^{-\frac{T}{RC}}\right\}$$

When $T >> RC\,(T \to \infty)$

$$E_{dissipated} = CV_{DD}{}^2\left(\frac{RC}{T}\right) \simeq 0.$$

When $T << RC\,(T \to 0)$

$$E_{dissipated} \simeq CV_{DD}{}^2\left(\frac{RC}{T}\right)\left\{1 - \frac{RC}{T} + \frac{RC}{T}\left(1 - \frac{T}{RC} + \frac{1}{2}\left(\frac{T}{RC}\right)^2\right)\right\}$$

$$= CV_{DD}{}^2\left(\frac{RC}{T}\right)\left(\frac{1}{2}\frac{T}{RC}\right) = \frac{1}{2}CV_{DD}{}^2$$

We can explain the results intuitively. When the rise time of V_{in} is low (T << RC), we can assume V_{in}= V_{DD} for the entire transition period and hence the capacitor will charge up to V_{DD} at some time provided V_{in} remains at V_{DD} for sufficient time. So the energy stored in capacitor will be $(1/2)CV_{DD}{}^2$ and the rest of the energy $(1/2)CV_{DD}{}^2$ will be dissipated across the resistor.

When the rise time of V_{in} is high (T >> RC), the output signal, V_{out} can follow the input signal V_{in}, i.e., $V_{out}(t) = V_{in}(t)$. Hence, the energy dissipation ~ $(V_{in}(t) - V_{out}(t))$ ~ 0.