Homework 2 Solution

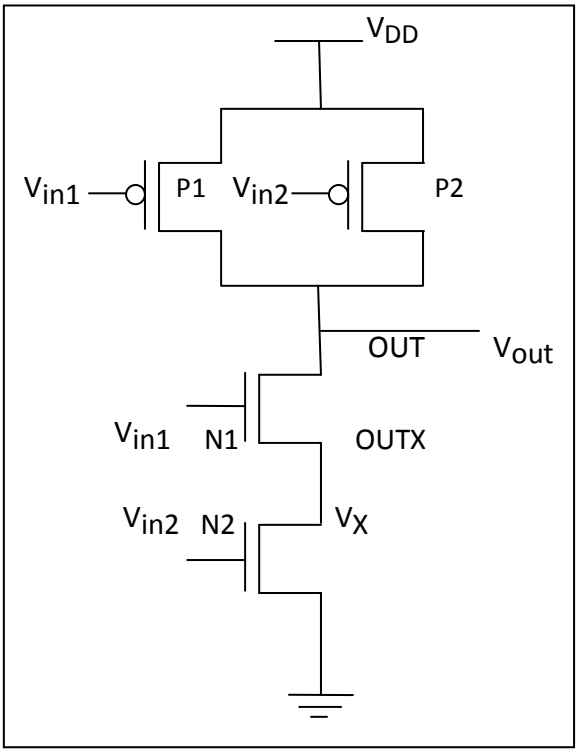
ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 24-Sep-2009 Due: 06-Oct-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: Consider a 2-input NAND gate as below.



a) Assume the following two different cases of input transitions

1) V_{in1} is fixed at logic '1' and V_{in2} is making transition from 0→1.
2) V_{in2} is fixed at logic '1' and V_{in1} is making transition from 0→1.

Which case will incur a higher falling delay at the output? Explain clearly the reason.

b) Do a SPICE simulation with the libraries that you have used in Tutorial 2, i.e., *tsmc25N* and *tsmc25P* to confirm the result. Assume the following parameters

L=240nm, W_p =1250nm, W_n =450nm, V_{DD} = 2.5 V.

Also, connect a 20f F capacitance at both the nodes *OUT* and *OUTX*.

Solution:

a)

When V_{in1} is fixed at logic '1' and V_{in2} is making transition from 0→1, initially (V_{in1}=1, V_{in2}=0), the intermediate node OUTX is set to some voltage level (depending on the strengths of the NMOSs N1 and N2). For similar strengths of the transistors N1 and N2, this voltage level will be closer to V_{DD} as the NMOS N2 is at cut-off and thus a higher voltage drop is expected to happen across the transistor N2. Accordingly, the intermediate node (OUTX) capacitance has to be discharged in addition to the output node capacitance while NMOS network gets ON during the transition of V_{in2} from 0→1.

But when V_{in2} is fixed at logic '1' and V_{in1} is making transition from 0→1, initially (V_{in1}=0, V_{in2}=1), the intermediate node OUTX is set to some voltage level (depending on the strengths of the NMOSs N1 and N2). For similar strengths of the transistors N1 and N2, this voltage level will be quite closer to 0 as the NMOS N2 is ON and thus a very low voltage drop is expected to happen across the transistor N2. Accordingly, only the output node capacitance has to be discharged while NMOS network gets ON during the transition of V_{in1} from 0→1.

Thus, the falling delay would be higher for the first case (V_{in1} is fixed at logic '1' and V_{in2} is making transition from 0→1) than that of the second case.

b)

V_{in1} is fixed at logic '1' and V_{in2} is making transition from 0→1 **= 3.3198E-10 Sec**

V_{in2} is fixed at logic '1' and V_{in1} is making transition from 0→1 **= 2.5658E-10 Sec**

SPICE Code

```
* HW 2, Problem 1, Part b) Solution
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.PARAM VDD  = 2.5v
.PARAM VREF = 1.25v
.PARAM L    = 240n
.PARAM WP   = 1250n
.PARAM WN   = 450n

.TEMP    25.0000
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25N" NMOS
.lib "$CDK_DIR/models/hspice/public/publicModel/tsmc25P" PMOS

C0 OUT 0  20E-15 M=1.0
C1 OUTX 0  20E-15 M=1.0
MP1 OUT IN1 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1
MP2 OUT IN2 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1
MN1 OUT IN1 OUTX 0  TSMC25N  L='L' W='WN'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1
MN2 OUTX IN2 0 0  TSMC25N  L='L' W='WN'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1
* END OF NETLIST

* specify voltages
VIN1 IN1 0 PULSE 0 2.5v 10n 1n 1n 40n 80n
VIN2 IN2 0 PULSE 0 2.5v   0n 1n 1n 20n 40n
VVDD! VDD! 0 DC=VDD
```

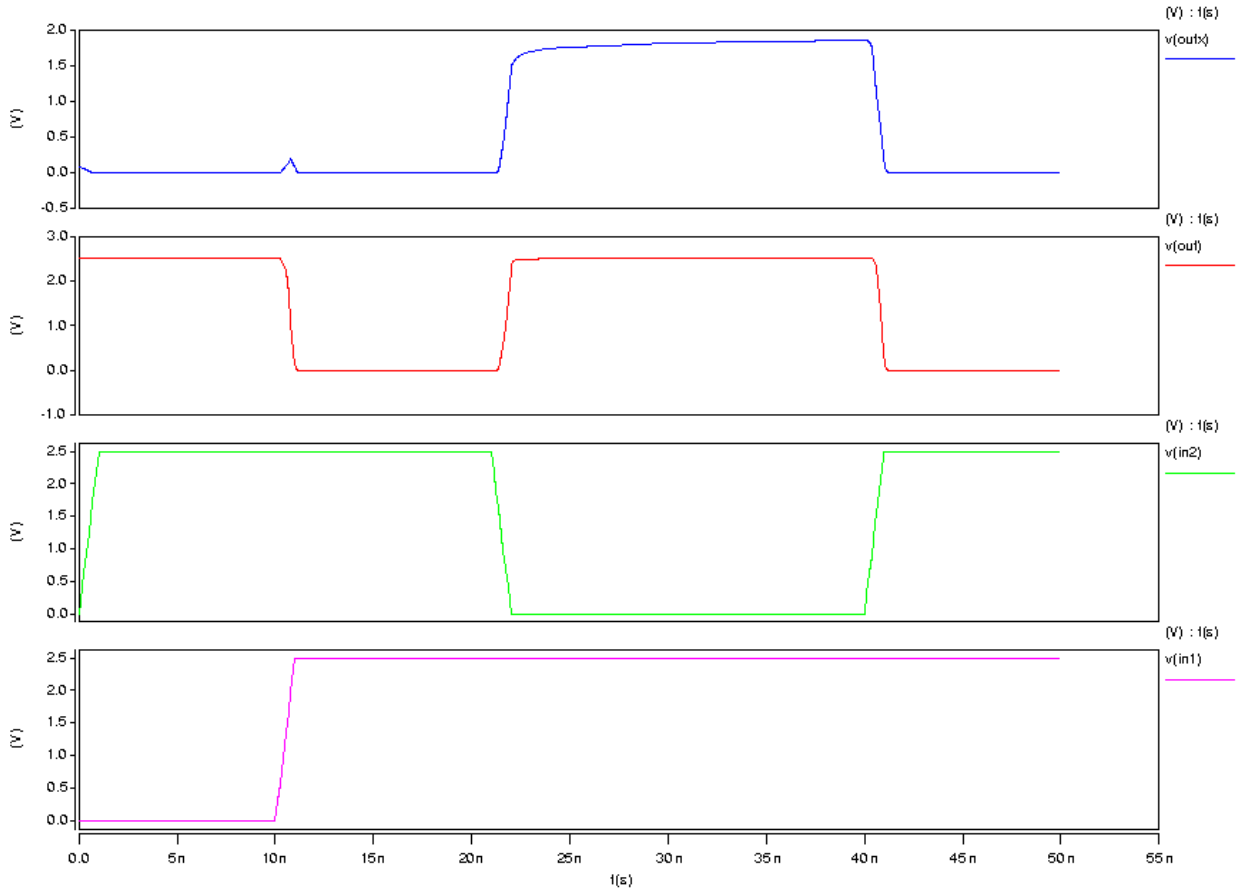
```
* transient analysis
.TRAN  1n 50n START=0
.OP
.SAVE
.OPTION  POST

.PRINT TRAN V(IN1) V(IN2) V(OUT)

* measure delays
.MEASURE TPHL1 TRIG V(IN1) VAL=VREF RISE=1 TARG V(OUT) VAL=VREF FALL=1
*measure at the 2nd rising edge of VIN2, see the waveforms
.MEASURE TPHL2 TRIG V(IN2) VAL=VREF RISE=2 TARG V(OUT) VAL=VREF FALL=2

.END
```

Waveforms



Problem 2: Consider the same 2-input NAND gate as in the problem 1. Assume that the substrates for all the PMOSs and NMOSs are connected to V_{DD} and ground, respectively.

a) You do not need to consider the capacitances at the nodes *OUT* and *OUTX* for this part. Assume the following.

$V_{DD} = 1$ V	$V_{in1} = V_{in2} = 0.5$ V
$K_p' = \mu_p C_{ox} = 30e\text{-}6$ A/V^2	$K_n' = \mu_n C_{ox} = 60e\text{-}6$ A/V^2
$V_{tp} = -0.3$ V	$V_{tn} = 0.3$ V (without body effect)
$\lvert 2\phi_f \rvert = 0.6$ V	$\gamma = 0.4$ V$^{0.5}$
$W_p/L_p = 2$	$W_n/L_n = 2$.

Determine the output voltage, V_{out}

i. Without body effect
ii. With body effect

You may think of using *matlab* to solve your equations.

b) Do a SPICE simulation with the libraries that you have used in Tutorial 2, i.e., *tsmc25N* and *tsmc25P*. Assume the following parameters

L=240nm, W_p =1250nm, W_n =450nm, V_{DD} = 2.5 V, $V_{in1} = V_{in2}$ = 1.25 V.

Also, connect a 20f F capacitance at both the nodes *OUT* and *OUTX*.

The body-effect is modeled in SPICE as follows.

$$\Delta V_{T,body\_effect} = k1.\left(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}\right) - k2.V_{BS}$$

where *k1* and *k2* are fitting coefficients. So if we don't want to consider the body effect, we need to make these two coefficients zero in the corresponding libraries *tsmc25N* and *tsmc25P*. The location of the library files is

\package\eda\cells\ncsu-cdk-1.5.1\local\models\hspice\public\publicModel\.

Solution:

a) i. With $V_{in1} = V_{in2} = 0.5$ V, we will assume that output, V_{out} is still at some higher value (toward V_{DD}). We will verify if our assumption is correct or not. Accordingly, the PMOSs would be in *linear* region. Since, quite a lot of voltage will be dropped across the NMOS with input V_{in1}, the NMOS N1 can be assumed to be in *saturation* region. Accordingly, since the voltage across the drain and source terminal of the NMSO N2 is small, it can be assumed in *linear* region.

$$I_{D,P1} = I_{D,P1} = 30*10^{-6}*2*\left((0.5-1+0.3)*(vout-1) - \frac{(vout-1)^2}{2} \right).$$

$$I_{D,P} = I_{D,P1} + I_{D,P2}.$$

$$I_{D,N1} = 60*10^{-6}*2*\left(\frac{(0.5-0.3-vx)^2}{2} \right).$$

$$I_{D,N2} = 60*10^{-6}*2*\left((0.5-0.3)*vx - \frac{vx^2}{2} \right).$$

Solving for $I_{D,N1} = I_{D,N2}$ we get vx = 0.0586.

MATLAB Code

```
fsolve(@(x) (0.5-0.3-x)^2/2 - ((0.5-0.3)*x - x^2/2), 0.1)
```

Then using $I_{D,P} = I_{D,N2}$ we get vout = 0.9414.

MATLAB Code

```
fsolve(@(x) (0.5-1+0.3)*(x-1)- (x-1)^2/2 - 0.01, 0.9)
```

We can now verify that the regions of operation that were assumed are indeed correct. So the results are

P1, P2: linear
N1: saturation
N2: linear

$V_X = 0.0586$ V

$V_{out} = 0.9414$ V.

a) ii. With $V_{in1} = V_{in2} = 0.5$ V, we will first assume that output, V_{out} is still at some higher value (toward V_{DD}). We will verify if our assumption is correct or not. Accordingly, the PMOSs would be in *linear* region. Since, quite a lot of voltage will be dropped across the NMOS with input V_{in1}, the NMOS N1 can be assumed to be in *saturation* region. Accordingly, since the voltage across the drain and source terminal of the NMSO N2 is small, it can be assumed in *linear* region.

$$I_{D,P1} = I_{D,P1} = 30*10^{-6}*2*\left((0.5-1+0.3)*(vout-1) - \frac{(vout-1)^2}{2} \right).$$

$$I_{D,P} = I_{D,P1} + I_{D,P2}.$$

$$I_{D,N1} = 60*10^{-6}*2*\left(\frac{\left(0.5-\left(0.3+0.4*\left(\sqrt{0.6+vx}-\sqrt{0.6}\right)\right)-vx\right)^2}{2} \right).$$

$$I_{D,N2} = 60*10^{-6}*2*\left((0.5-0.3)*vx - \frac{vx^2}{2} \right).$$

Solving for $I_{D,N1} = I_{D,N2}$ we get vx = 0.0521.

MATLAB Code

```
fsolve(@(x) (0.5-0.3-0.4*(sqrt(0.6+x)-sqrt(0.6))-x)^2/2 - ((0.5-0.3)*x - x^2/2), 0.1)
```

Then using $I_{D,P} = I_{D,N2}$ we get vout = 0.9476.

MATLAB Code

```
fsolve(@(x) (0.5-1+0.3)*(x-1)- (x-1)^2/2 - 0.0091, 0.9)
```

We can now verify that the regions of operation that were assumed are indeed correct. So the results are

P1, P2: linear
N1: saturation
N2: linear

$V_X = 0.0521$ V

$V_{out} = 0.9476$V.

You can also approximate the body effect part assuming $V_X << 0.6$ as follows and solve by hand.

$$\sqrt{0.6+vx}-\sqrt{0.6}=\sqrt{0.6*\left(1+\frac{vx}{0.6}\right)}-\sqrt{0.6}=\sqrt{0.6}*\left(\left(1+\frac{vx}{0.6}\right)^{1/2}-1\right)$$

$$=\sqrt{0.6}*\left(\left(1+\frac{1}{2}\frac{vx}{0.6}\right)-1\right)=\sqrt{0.6}*\frac{1}{2}\frac{vx}{0.6}.$$

b)

Without Body Effect, **V_{out} = 2.3212 V**
With Body Effect, **V_{out} = 2.3752 V**

SPICE Code

```
* HW 2, Problem 2, Part b) Solution
* ECE 559, Fall 2009, Purdue University

.GLOBAL VDD!

.PARAM VDD  = 2.5v
.PARAM VREF = 1.25v
.PARAM L    = 240n
.PARAM WP   = 1250n
.PARAM WN   = 450n

.TEMP  25.0000

* With Body Effect
.lib "tsmc25N" NMOS
.lib "tsmc25P" PMOS

* Without Body Effect
*.lib "tsmc25N_no_body_effect" NMOS  * k1, k2 = 0 in tsmc25N
*.lib "tsmc25P_no_body_effect" PMOS  * k1, k2 = 0 in tsmc25P
```

```
C0 OUT 0  20E-15 M=1.0
C1 OUTX 0  20E-15 M=1.0
MP1 OUT IN1 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1
MP2 OUT IN2 VDD! VDD!  TSMC25P  L='L' W='WP'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1
MN1 OUT IN1 OUTX 0  TSMC25N  L='L' W='WN'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1
MN2 OUTX IN2 0 0  TSMC25N  L='L' W='WN'
+AD=+3.00000000E-13 AS=+3.00000000E-13 PD=+2.30000000E-06 PS=+2.30000000E-06
+M=1

* END OF NETLIST

.OP
.SAVE
.OPTION  POST

VVDD! VDD! 0 DC=VDD

VIN1 IN1 0 VREF
VIN2 IN2 0 VREF

.END
```

Comment

We are getting a higher output voltage with body effect as it would have required more gate voltage to have a lower output voltage similar to the case of without body effect.

Problem 3: Consider a pass-transistor network as shown in the below figure. Assume the following. Assume that the substrates of all the NMOSs are connected ground.

$V_{DD} = 1$ V

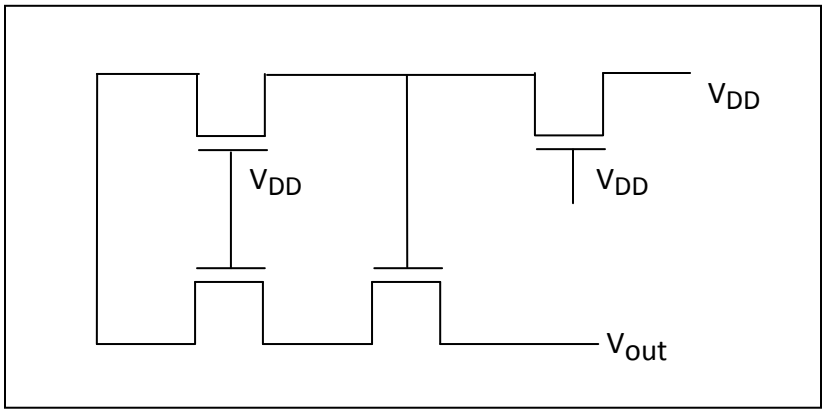
$K_n' = \mu_n C_{ox} = 60e\text{-}6$ A/V^2

$V_{tn} = 0.3$ V (without body effect)

$|2\phi_f| = 0.6$ V

$\gamma = 0.4\ V^{0.5}$

$W_n/L_n = 1.$

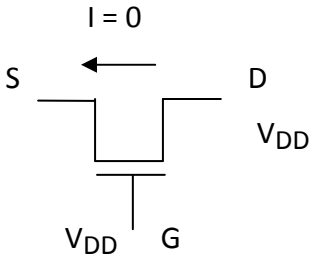


Determine the output voltage, V_{out}

i. Without body effect
ii. With body effect

You may think of using *matlab* to solve your equations.

Solution: We will first compute the source voltage of a transistor when it's gate and drain voltages both are V_{DD}.



The source voltage of the transistor will set to some value V_x at which point no more current will flow through the transistor. Note that the transistor is in saturation as

$$\begin{aligned} &V_{DS} > V_{GS} - V_{tn} \\ &\Rightarrow V_D - V_S > V_G - V_S - V_{tn} \\ &\Rightarrow V_D > V_G - V_{tn} \\ &\Rightarrow V_{DD} > V_{DD} - V_{tn} \\ &\Rightarrow V_{tn} > 0 \end{aligned}$$

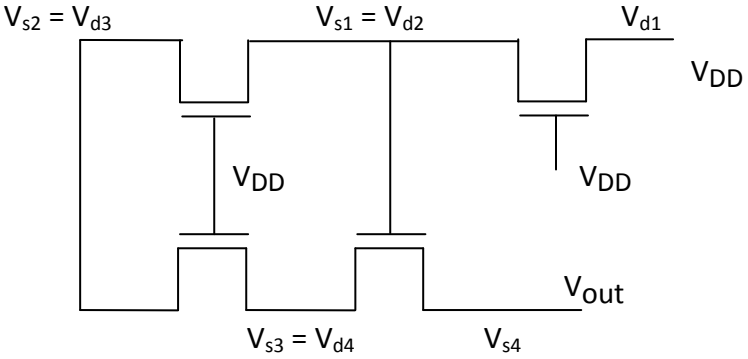
provided

$$\begin{aligned} &V_{GS} > V_{tn} \\ &\Rightarrow V_{DD} - V_x > V_{tn} \\ &\Rightarrow V_x < V_{DD} - V_{tn}. \end{aligned}$$

When the current through the transistor will be zero,

$$\begin{aligned} &I \sim (V_{GS} - V_{tn})^2 = 0 \\ &\Rightarrow V_{GS} = V_{tn} \\ &\Rightarrow V_G - V_S = V_{tn} \\ &\Rightarrow V_G - V_x = V_{tn} \\ &\Rightarrow V_x = V_{DD} - V_{tn} \end{aligned}$$

So the transistor is *at the boundary* of cutoff and saturation regions when I = 0. Initially when V_{DD} will be applied at the drain of the transistor, the transistor will be in saturation and over time the source voltage will be set at $V_{DD} - V_{tn}$. At last the transistor will be at the boundary of cutoff and saturation regions. Similarly, we can calculate the source voltages of the other transistors subsequently as we would have the drain and gate voltages of the transistors.



Accordingly,

$$V_{s1} = V_{d2} = V_{DD} - V_{tn}$$
$$V_{s2} = V_{d3} = V_{DD} - V_{tn}$$
$$V_{s3} = V_{d4} = V_{DD} - V_{tn}$$
$$V_{s4} = V_{out} = V_{DD} - 2V_{tn}$$

We can also follow the node voltages using the reasoning for *pass transistor* logic as well.

For including body effect we need to put the source voltage dependent threshold voltage term in the equation and solve it. A matlab program is given below that determines the source voltages for each NMOS in a subsequent mannerand also the regions of operation for the transistors.

MATLAB Code

```
%
% HW 2, Problem 3
% ECE 559, Fall 2009, Purdue University
% Kuntal Roy (royk@purdue.edu)
% Date: 08-Oct-2009
%

clear all
clc

N = 4;          % no. of transistors

vdd = 1;
tphif = 0.6;    % 2*phi_f
vtn0 = 0.3;

gamma = .4;
%gamma = 0;      % no body effect

% To change the varaibles to integer so that any problem due to floating
% point number matching does not arise
dec_precision = 3;
precision_mult = power(10,3);

vd = zeros(4,1);
vg = zeros(4,1);
vs = zeros(4,1);
vt = zeros(4,1);

saturation  = zeros(4,1);
```

```
linear      = zeros(4,1);
cutoff      = zeros(4,1);

vd(1) = vdd;

vg(1) = vdd;
vg(2) = vdd;
vg(3) = vdd;

% 1st transistor is in saturation as vg1 = vd1, also in cutoff as vgs = vtn
vs(1) = fsolve(@(x) vg(1)-x-vtn0-gamma*(sqrt(tphif+x)-sqrt(tphif)), 0.7);
vg(4) = vs(1);
saturation(1) = 1;
cutoff(1) = 1;
vt(1) = vtn0 + gamma*(sqrt(tphif+vs(1))-sqrt(tphif));

% solving subsequently for the next three transistors
for i = 2:N

    vd(i) = vs(i-1);

    % check if it is in linear region or in saturation region
    vs_lin = fsolve(@(x) (vg(i)-x-vtn0-gamma*(sqrt(tphif+x)-
sqrt(tphif)))*(vd(i)-x) - (vd(i)-x)^2/2, 0.5, optimset('TolFun',1e-20));
    vs_sat = fsolve(@(x) (vg(i)-x-vtn0-gamma*(sqrt(tphif+x)-
sqrt(tphif)))^2/2, 0.5, optimset('TolFun',1e-20));

    % threshold voltages corresponding to linear or saturation regions
    vtn_lin = vtn0 + gamma*(sqrt(tphif+vs_lin)-sqrt(tphif));
    vtn_sat = vtn0 + gamma*(sqrt(tphif+vs_sat)-sqrt(tphif));

    % change the varaibles to integer so that any problem due to floating
    % point number matching does not arise
    vs_lin = int16(str2double(sprintf('%5d',vs_lin*precision_mult)));
    vs_sat = int16(str2double(sprintf('%5d',vs_sat*precision_mult)));
    vtn_lin = int16(str2double(sprintf('%5d',vtn_lin*precision_mult)));
    vtn_sat = int16(str2double(sprintf('%5d',vtn_sat*precision_mult)));

    vgi = int16(str2double(sprintf('%5d',vg(i)*precision_mult)));
    vsi = int16(str2double(sprintf('%5d',vs(i)*precision_mult)));
    vdi = int16(str2double(sprintf('%5d',vd(i)*precision_mult)));

    % linear region check
    if vgi - vs_lin >= vtn_lin && vdi <= vgi - vtn_lin && vs_lin >= 0
        vsi = vs_lin;
        linear(i) = 1;
    end

    % saturation region check
    if vgi - vs_sat >= vtn_sat && vdi >= vgi - vtn_sat && vs_sat >= 0
        vsi = vs_sat;
        saturation(i) = 1;
    end
```

```
    % also in cut-off region if the equality satisfies
    if vgi - vs_sat == vtn_sat || vgi - vs_lin == vtn_lin
        cutoff(i) = 1;
    end

    % if linear and saturation checks both fail, the transistor is indeed
    % in cutoff
    if saturation(i) == 0 && linear(i) == 0 && cutoff(i) == 0
        vsi = vdi;
        cutoff(i) = 1;
    end

    vs(i) = double(vsi)/precision_mult;
    vt(i) = vtn0 + gamma*(sqrt(tphif+vs(i))-sqrt(tphif));
    vt(i) = str2double(sprintf('%5.3f',vt(i)));

end

for i = 1:N
    disp(sprintf('NMOS %d: Region of operation: [(sat,lin,off):
(%1d,%1d,%1d)] vg: %6.3f vd: %6.3f vs: %6.3f vgs: %6.3f vds: %6.3f vt:
%6.3f', i, saturation(i), linear(i), cutoff(i), vg(i), vd(i), vs(i), vg(i)-
vs(i), vd(i)- vs(i), vt(i)))
end
```

Results (With Body Effect, gamma = 0.4)

```
NMOS 1: Region of operation: [(sat,lin,off): (1,0,1)] vg:  1.000
vd:  1.000 vs:  0.576 vgs:  0.424 vds:  0.424 vt:  0.424
NMOS 2: Region of operation: [(sat,lin,off): (1,1,1)] vg:  1.000
vd:  0.576 vs:  0.576 vgs:  0.424 vds:  0.000 vt:  0.424
NMOS 3: Region of operation: [(sat,lin,off): (1,1,1)] vg:  1.000
vd:  0.576 vs:  0.576 vgs:  0.424 vds:  0.000 vt:  0.424
NMOS 4: Region of operation: [(sat,lin,off): (1,0,1)] vg:  0.576
vd:  0.576 vs:  0.223 vgs:  0.353 vds:  0.353 vt:  0.353
```

Results (Without Body Effect, gamma = 0)

```
NMOS 1: Region of operation: [(sat,lin,off): (1,0,1)] vg:  1.000
vd:  1.000 vs:  0.700 vgs:  0.300 vds:  0.300 vt:  0.300
NMOS 2: Region of operation: [(sat,lin,off): (1,1,1)] vg:  1.000
vd:  0.700 vs:  0.700 vgs:  0.300 vds:  0.000 vt:  0.300
NMOS 3: Region of operation: [(sat,lin,off): (1,1,1)] vg:  1.000
vd:  0.700 vs:  0.700 vgs:  0.300 vds:  0.000 vt:  0.300
NMOS 4: Region of operation: [(sat,lin,off): (1,0,1)] vg:  0.700
vd:  0.700 vs:  0.400 vgs:  0.300 vds:  0.300 vt:  0.300
```