

Homework 2

ECE 559: MOS VLSI Design (Fall 2009)

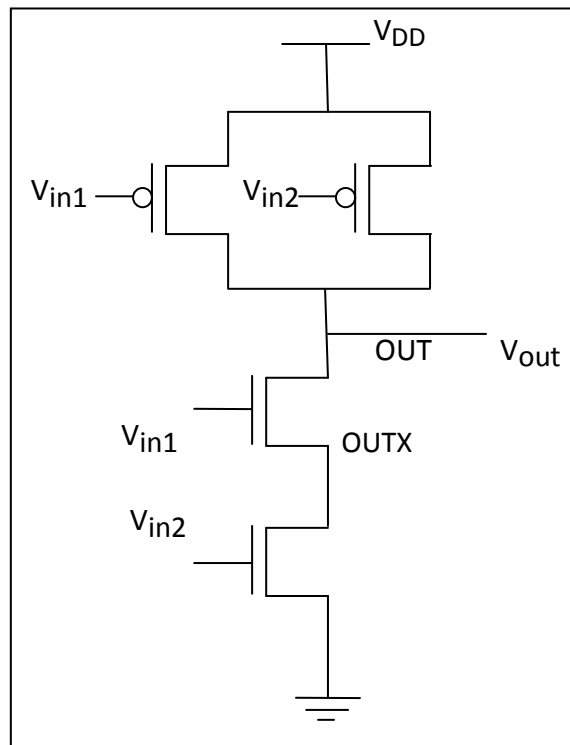
ECE Department, Purdue University

Assigned: 24-Sep-2009

Due: 06-Oct-2009

Important: Please turn-in all of your codes along with the waveforms (when necessary) during submission of your solution. You may be asked to provide the soft copy of your codes by email if such need arises.

Problem 1: Consider a 2-input NAND gate as below.



a) Assume the following two different cases of input transitions

- 1) V_{in1} is fixed at logic '1' and V_{in2} is making transition from 0→1.
- 2) V_{in2} is fixed at logic '1' and V_{in1} is making transition from 0→1.

Which case will incur a higher falling delay at the output? Explain clearly the reason.

- b) Do a SPICE simulation with the libraries that you have used in Tutorial 2, i.e., *tsmc25N* and *tsmc25P* to confirm the result. Assume the following parameters

$$L=240\text{nm}, W_p=1250\text{nm}, W_n=450\text{nm}, V_{DD}=2.5\text{ V}.$$

Also, connect a 20f F capacitance at both the nodes *OUT* and *OUTX*.

Problem 2: Consider the same 2-input NAND gate as in the problem 1. Assume that the substrates for all the PMOSs and NMOSs are connected to V_{DD} and ground, respectively.

- a) You do not need to consider the capacitances at the nodes *OUT* and *OUTX* for this part. Assume the following.

$$V_{DD} = 1\text{ V}$$

$$V_{in1} = V_{in2} = 0.5\text{ V}$$

$$K_p' = \mu_p C_{OX} = 30e-6\text{ A/V}^2$$

$$K_n' = \mu_n C_{OX} = 60e-6\text{ A/V}^2$$

$$V_{tp} = -0.3\text{ V}$$

$$V_{tn} = 0.3\text{ V} \quad (\text{without body effect})$$

$$|2\phi_f| = 0.6\text{ V}$$

$$\gamma = 0.4\text{ V}^{0.5}$$

$$W_p/L_p = 2$$

$$W_n/L_n = 2.$$

Determine the output voltage, V_{out}

- i. Without body effect
- ii. With body effect

You may think of using *matlab* to solve your equations.

- b) Do a SPICE simulation with the libraries that you have used in Tutorial 2, i.e., *tsmc25N* and *tsmc25P*. Assume the following parameters

$$L=240\text{nm}, W_p=1250\text{nm}, W_n=450\text{nm}, V_{DD}=2.5\text{ V}, V_{in1}=V_{in2}=1.25\text{ V}.$$

Also, connect a 20f F capacitance at both the nodes *OUT* and *OUTX*.

The body-effect is modeled in SPICE as follows.

$$\Delta V_{T, \text{body_effect}} = k1 \cdot \left(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f} \right) - k2 \cdot V_{BS}$$

where k_1 and k_2 are fitting coefficients. So if we don't want to consider the body effect, we need to make these two coefficients zero in the corresponding libraries *tsmc25N* and *tsmc25P*. The location of the library files is

`\package\eda\cells\ncsu-cdk-1.5.1\local\models\hspice\public\publicModel\.`

Problem 3: Consider a pass-transistor network as shown in the below figure. Assume the following. Assume that the substrates of all the NMOSs are connected ground.

$$V_{DD} = 1 \text{ V}$$

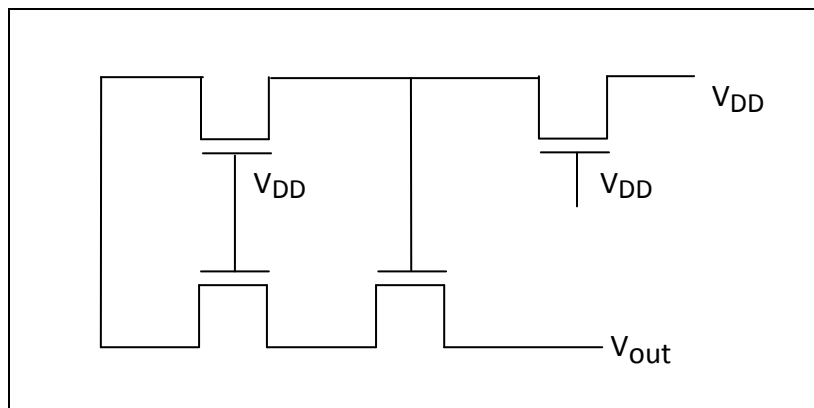
$$K_n' = \mu_n C_{ox} = 60e-6 \text{ A/V}^2$$

$$V_{tn} = 0.3 \text{ V (without body effect)}$$

$$|2\phi_f| = 0.6 \text{ V}$$

$$\gamma = 0.4 \text{ V}^{0.5}$$

$$W_n/L_n = 1.$$



Determine the output voltage, V_{out}

- i. Without body effect
- ii. With body effect

You may think of using *matlab* to solve your equations.