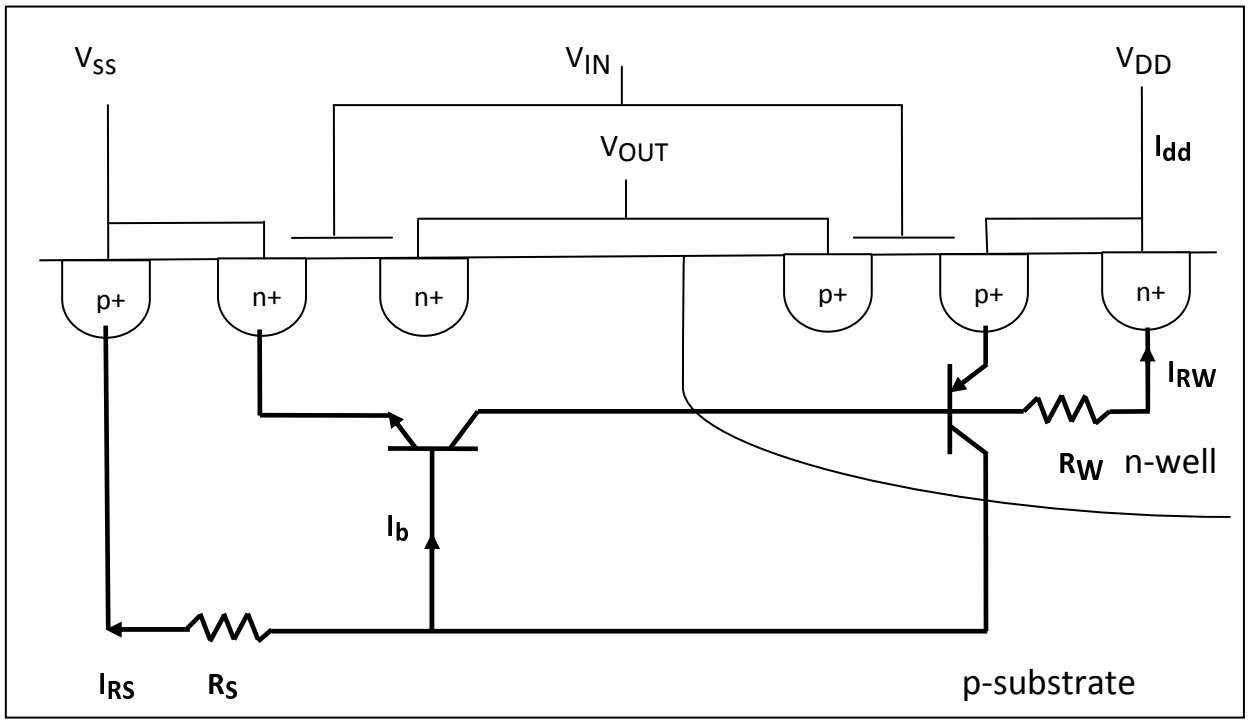
Homework 1 Solution

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

Assigned: 17-Sep-2009 Due: 24-Sep-2009

Problem 1 (Latchup): The schematic and equivalent circuit of parasitic resistors and bipolar transistors in a CMOS is shown below. Here, the latchup is triggered at the point when the *npn*-transistor is turned on, i.e., the voltage drop across the resistor R_s is larger than the turn-on voltage of *npn*-transistor.

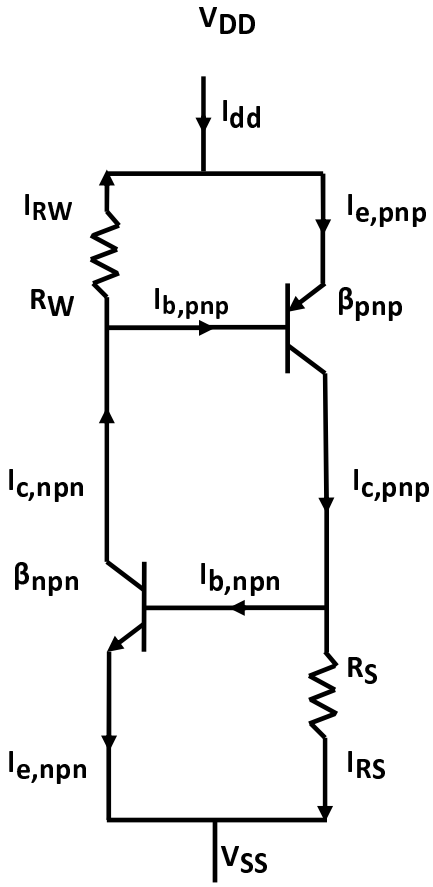


From this condition, derive the following inequality for the triggering of the latchup

$$\beta_{npn}\beta_{pnp} > 1 + \frac{\left(\beta_{npn}+1\right)\left(I_{RS}+I_{RW}\beta_{pnp}\right)}{\left(I_{dd}-I_{RS}\right)}.$$

Where β_{pnp} and β_{npn} are the common-emitter current gains for the *pnp* and *npn* transistors, respectively.

Solution:



The triggering of latchup occurs when $I_{latchup} > I_{RS}$.

where $I_{latchup}$ is the current flowing through the resistor R_s .

So the condition is

$$I_{latchup} = I_{c,pnp} - I_{b,npn} > I_{RS}$$
$$\Rightarrow \beta_{pnp} I_{b,pnp} - I_{b,npn} > I_{RS}$$
$$\Rightarrow \beta_{pnp} \left(I_{c,npn} - I_{RW} \right) - I_{b,npn} > I_{RS}$$
$$\Rightarrow \beta_{pnp} \left(\beta_{npn} I_{b,npn} - I_{RW} \right) - I_{b,npn} > I_{RS}$$
$$\Rightarrow \left(\beta_{pnp} \beta_{npn} - 1 \right) I_{b,npn} - \beta_{pnp} I_{RW} > I_{RS}$$

$I_{b,npn}$ can be expressed in terms of total supply current I_{dd} .

$$I_{dd} = I_{RS} + I_{e,npn}$$

$$\Rightarrow I_{dd} = I_{RS} + \left(\beta_{npn} + 1\right) I_{b,npn}$$

$$\Rightarrow I_{b,npn} = \frac{\left(I_{dd} - I_{RS}\right)}{\left(\beta_{npn} + 1\right)}$$

Substituting $I_{b,npn}$, we get

$$\left(\beta_{pnp}\beta_{npn} - 1\right)\frac{\left(I_{dd} - I_{RS}\right)}{\left(\beta_{npn} + 1\right)} - \beta_{pnp} I_{RW} > I_{RS}$$

$$\Rightarrow \beta_{pnp}\beta_{npn} > 1 + \frac{\left(\beta_{npn} + 1\right)\left(I_{RS} + \beta_{pnp} I_{RW}\right)}{\left(I_{dd} - I_{RS}\right)} \qquad \textbf{(Proved)}$$

Note: Ideally the directions of the current paths $\mathbf{I_{c,npn}}$, $\mathbf{I_{b,pnp}}$, and $\mathbf{I_{RW}}$ should have the opposite directions as of shown. But, to show the positive feedback path for the two transistors, the directions are shown in this way.

Problem 2 (CMOS Limits): Prove that the minimum V_{DD} for CMOS circuit operation is

$$V_{DD}\,|_{\min} = 2\ln(2)\frac{KT}{q}.$$

Solution:

Let us consider a simple inverter and assume subthreshold mode of operation. Equating the subthreshold currents for the NMOS and PMOS, we get

$$e^{\frac{qV_{GS,n}}{KT}}\left(1-e^{-\frac{qV_{DS,n}}{KT}}\right) = e^{\frac{qV_{SG,p}}{KT}}\left(1-e^{-\frac{qV_{SD,p}}{KT}}\right)$$

$$\Rightarrow e^{\frac{qV_{in}}{KT}}\left(1-e^{-\frac{qV_{out}}{KT}}\right) = e^{\frac{q(V_{DD}-V_{in})}{KT}}\left(1-e^{-\frac{q(V_{DD}-V_{out})}{KT}}\right)$$

$$\Rightarrow V_{in} = \frac{V_{DD}}{2} + \frac{KT}{2q}\ln\left(\frac{1-e^{-\frac{q(V_{DD}-V_{out})}{KT}}}{1-e^{-\frac{qV_{out}}{KT}}}\right).$$

Note that for simplicity we have assumed symmetric NMOS and PMOS. However, it is not limited to the case. See pp. 149-150 from the following paper.

> Swanson, R. M. and Meindel, J. D., "Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits", IEEE Journal of Solid-State Circuits, Vol. SC-7, No. 2, April 1972, pp. 146-153.

Also, we have assumed, m = 1. Actually,

$$m = 1 + \frac{C_D}{C_{ox}}$$

where C_D and C_{ox} are depletion capacitance and oxide capacitance, respectively. Assuming $C_D << C_{ox}$, m = 1. The minimum value of *m* is assumed that would give rise to minimum V_{DD}. Also we have ignored *channel length modulation* for large V_{DS}.

Let us assume

$$A = \left(1 - e^{-\frac{q(V_{DD} - V_{out})}{KT}}\right) \qquad B = \left(1 - e^{-\frac{qV_{out}}{KT}}\right)$$

$$\Rightarrow \frac{dA}{dV_{out}} = \frac{q}{KT}(A-1). \qquad \Rightarrow \frac{dB}{dV_{out}} = \frac{q}{KT}(1-B).$$

We know that for regenerative action of an inverter

$$\frac{dV_{in}}{dV_{out}} = -1$$

$$\Rightarrow \frac{1}{2}\left(\frac{(A-1)}{A} - \frac{(1-B)}{B}\right) = -1$$

$$\Rightarrow A + B = 4AB$$

$$\Rightarrow \left(1 - e^{-\frac{q(V_{DD} - V_{out})}{KT}}\right) + \left(1 - e^{-\frac{qV_{out}}{KT}}\right) = 4\left(1 - e^{-\frac{qV_{out}}{KT}} - e^{-\frac{q(V_{DD} - V_{out})}{KT}} + e^{-\frac{qV_{DD}}{KT}}\right)$$

$$\Rightarrow 3\left(e^{-\frac{q(V_{DD} - V_{out})}{KT}} - e^{-\frac{qV_{out}}{KT}}\right) = 4e^{-\frac{qV_{DD}}{KT}} + 2$$

We have to choose V_{out} for which minimum V_{DD} is achieved. Differentiating the previous expression with respect to V_{out} and making

$$\frac{dV_{DD}}{dV_{out}} = 0$$

we get

$$e^{-\frac{qV_{out}}{KT}} - e^{-\frac{qV_{DD}}{KT}} e^{\frac{qV_{out}}{KT}} = 0$$

$$\Rightarrow V_{out} = \frac{V_{DD}}{2}.$$

Putting $V_{out} = \frac{V_{DD}}{2}$,

$$\left(1-e^{-\frac{q\left(V_{DD}-\frac{V_{DD}}{2}\right)}{KT}}\right)+\left(1-e^{-\frac{qV_{DD}}{2KT}}\right)=4\left(1-e^{-\frac{qV_{DD}}{2KT}}-e^{-\frac{q\left(V_{DD}-\frac{V_{DD}}{2}\right)}{KT}}+e^{-\frac{qV_{DD}}{KT}}\right)$$

$$\Rightarrow 2\left(1-e^{-\frac{qV_{DD}}{2KT}}\right)=4\left(1-e^{-\frac{qV_{DD}}{2KT}}\right)^2$$

$$\Rightarrow \left(1-e^{-\frac{qV_{DD}}{2KT}}\right)=\frac{1}{2}$$

$$\Rightarrow e^{-\frac{qV_{DD}}{2KT}}=\frac{1}{2}$$

$$\Rightarrow V_{DD}\,|_{\min}=2\ln(2)\frac{KT}{q}.$$

Problem 3 (Pseduo-NMOS): Consider a pseudo-NMOS 2-input NAND gate as in the figure below. Use the following

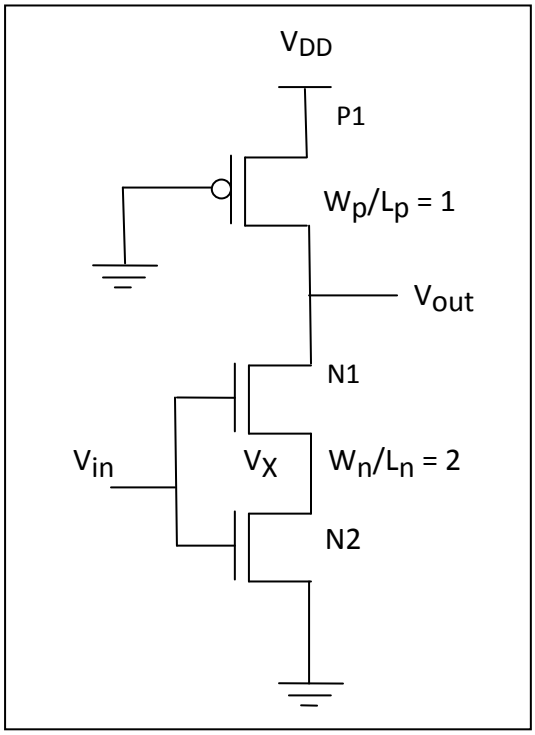
$V_{DD} = 1$ V

$K_p' = \mu_p C_{ox} = 30\text{e-}6\ A/V^2$ $K_n' = \mu_n C_{ox} = 60\text{e-}6\ A/V^2$

$V_{tp} = -0.3$ V $V_{tn} = 0.3$ V.

Assume there is no sub threshold current, no body effect, and every transistor has ideal long-channel characteristics.

Determine the output voltage (V_{out}) when the input voltage is i) 0 V ii) 0.2 V iii) 0.3 V iv) 0.4 V v) 0.7 V vi) 1 V.



Solution:

i) When $V_{in} = 0$, NMOS N2 is at cut-off region of operation ($V_{gs,N1} = 0$ V < $V_{tn} = 0.3$ V). So $I_{N2} = 0$. Since the transistors are serially connected, $I_{P1} = 0$. Hence the voltage drop across the PMOS P1 is 0. So

$$V_{out} = V_{DD} = 1 \text{ V}.$$

ii) When V_{in} = 0.2 V, NMOS N2 is at cut-off region of operation ($V_{gs,N1}$ = 0.2 V < V_{tn} = 0.3 V). So I_{N2} = 0. Since the transistors are serially connected, I_{P1}=0. Hence the voltage drop across the PMOS P1 is 0. So

$$V_{out} = V_{DD} = 1 \text{ V}.$$

iii) When V_{in} = 0.3 V, NMOS N2 is at cut-off region of operation ($V_{gs,N1} = V_{tn}$ = 0.3 V). So I_{N2} = 0. Since the transistors are serially connected, I_{P1} = 0. Hence the voltage drop across the PMOS P1 is 0. So

$$V_{out} = V_{DD} = 1 \text{ V}.$$

iv) When V_{in} = 0.4 V, NMOS N2 is no longer at cut-off region of operation ($V_{gs,N1}$ = 0.4 V > V_{tn} = 0.3 V). It can be either in linear or saturation region. We may have to do trial and error procedure to determine the correct regions of operation for the MOSs.

MOS	**Saturation**	**Linear**
P1	$V_{ds,P1} < V_{gs,P1} - V_{tp}$ $V_{out} - V_{DD} < (0 - V_{DD}) - V_{tp}$ **$V_{out} < 0.3$**	**$V_{out} > 0.3$**
N1	$V_{ds,N1} > V_{gs,N1} - V_{tn}$ $(V_{out} - V_X) > (0.4 – V_X) - 0.3$ **$V_{out} > 0.1$**	**$V_{out} < 0.1$**
N2	$V_{ds,N2} > V_{gs,N2} - V_{tn}$ $V_X > 0.4 – 0.3$ **$V_X > 0.1$**	**$V_X < 0.1$**

Since with V_{in} = 0.4 V and V_{DD} = 1 V, it is *expected* that V_{out} would be quite high (greater than 0.3 V), we will first assume that *P1 is in linear region* and *N1 is in saturation region*. Since N1 is assumed to be in saturation region, on current flowing through the NMOS N1 will be high and it will incur a high voltage drop across the NMOS N1 itself. But we are not very sure how much the voltage drop would be. So we have to quite assume here for the region of operation for NMOS N2. Let us assume that V_X < 0.1,

i.e., the *linear region of operation for the NMOS N2*. So the equations for the currents for the three MOSs would be as follows.

$$I_{D,P1} = 30*10^{-6}*1*\left((-1+0.3)*(vout-1) - \frac{(vout-1)^2}{2} \right).$$

$$I_{D,N1} = 60*10^{-6}*2*\left(\frac{(0.4-0.3-vx)^2}{2} \right).$$

$$I_{D,N2} = 60*10^{-6}*2*\left((0.4-0.3)*vx - \frac{vx^2}{2} \right).$$

Solving for $I_{D,N1} = I_{D,N2}$ we get vx = 0.0293. Then using $I_{D,P1} = I_{D,N2}$ we get vout = 0.9856. Since our assumptions $V_X < 0.1$ and $V_{out} > 0.3$ have come correct, we are right about our assumptions. So the results are

P1: linear
N1: saturation
N2: linear
V_X = 0.0293 V
V_{out} = 0.9856 V.

v) When V_{in} = 0.7 V, NMOS N2 is definitely no longer at cut-off region of operation ($V_{gs,N1}$ = 0.7 V > V_{tn} = 0.3 V). It can be either in linear or saturation region. We may have to do trial and error procedure to determine the correct regions of operation for the MOSs.

MOS	**Saturation**	**Linear**
P1	$V_{ds,P1} < V_{gs,P1} - V_{tp}$ $V_{out} - V_{DD} < (0 - V_{DD}) - V_{tp}$ **$V_{out} < 0.3$**	**$V_{out} > 0.3$**
N1	$V_{ds,N1} > V_{gs,N1} - V_{tn}$ $(V_{out} - V_X) > (0.7 - V_X) - 0.3$ **$V_{out} > 0.4$**	**$V_{out} < 0.4$**

N2	$V_{ds,N2} > V_{gs,N2} - V_{tn}$ $V_X > 0.7 - 0.3$ **$V_X > 0.4$**	**$V_X < 0.4$**

With V_{in} = 0.7 V and V_{DD} = 1 V, the output V_{out} may have value greater than 0.4 V, in between 0.3 V and 0.4 V, or even less than 0.3 V. However, this time you can quite assume that the NMOS N2 is in *linear* region as quite a lot of voltage drop will be happening across the ON NMOS N1 even if the output is at higher side. That we have already seen from the previous part (Vin = 0.4 V). So this time our assumption is strong on NMOS N2 that *N2 is in linear region*. We can try the following conditions for P1 and N1.

Step	Assumed Vout	P1	N1
1	$V_{out} > 0.4$	linear	saturation
2	$0.3 < V_{out} < 0.4$	linear	linear
3	$V_{out} < 0.3$	saturation	linear

Now, from the above table, we can easily observe that as the input voltage Vin is increased (i.e., Vout is decreased), we are going towards the combinations corresponding to the steps 1 to 3 gradually and subsequently. We can start from the first step. So we are assuming at first P1: linear, N1: saturation, and N2: linear. Recall what we have got from the previous part (Vin = 0.4 V) - P1: linear, N1: saturation, and N2: linear. So this time we *may* have to go for the other two combinations for the P1 and N1 as well.

Accordingly, the equations for the currents for the three MOSs would be as follows.

$$I_{D,P1} = 30*10^{-6}*1*\left((-1+0.3)*(vout-1) - \frac{(vout-1)^2}{2} \right).$$

$$I_{D,N1} = 60*10^{-6}*2*\left(\frac{(0.7-0.3-vx)^2}{2} \right).$$

$$I_{D,N2} = 60*10^{-6}*2*\left((0.7-0.3)*vx - \frac{vx^2}{2} \right).$$

Solving for $I_{D,N1} = I_{D,N2}$ we get vx = 0.1172. Then using $I_{D,P1} = I_{D,N2}$ we get vout = 0.7123. Since our assumptions $V_X < 0.4$ and $V_{out} > 0.4$ have come correct, we are right about our assumptions. So the results are

P1: linear
N1: saturation
N2: linear
$V_X = 0.1172$ V
$V_{out} = 0.7123$ V.

vi) When $V_{in} = 1.0$ V, NMOS N2 definitely is no longer at cut-off region of operation ($V_{gs,N1} = 0.7$ V > $V_{tn} = 0.3$ V). It can be either in linear or saturation region. We may have to do trial and error procedure to determine the correct regions of operation for the MOSs.

MOS	Saturation	Linear
P1	$V_{ds,P1} < V_{gs,P1} - V_{tp}$ $V_{out} - V_{DD} < (0 - V_{DD}) - V_{tp}$ **$V_{out} < 0.3$**	**$V_{out} > 0.3$**
N1	$V_{ds,N1} > V_{gs,N1} - V_{tn}$ $(V_{out} - V_X) > (1.0 - V_X) - 0.3$ **$V_{out} > 0.7$**	**$V_{out} < 0.7$**
N2	$V_{ds,N2} > V_{gs,N2} - V_{tn}$ $V_X > 1.0 - 0.3$ **$V_X > 0.7$**	**$V_X < 0.7$**

With $V_{in} = 1$ V and $V_{DD} = 1$ V, it is quite expected that the output V_{out} will have value less than 0.7 V. Also, this time we can quite assume that the NMOS N2 is in *linear* region as quite a lot of voltage drop will be happening across the ON NMOS N1 even if the output is at higher side. That we have already seen from the from the previous two parts (Vin = 0.4 V and Vin = 0.7 V). So this time our assumption is strong for the NMOSs *N1 and N2 that both are in linear region*.

We have to do assumption for PMOS P1. Since we are applying the highest voltage (Vin = V_{DD}) at the input, we should assume first that the output has reached a quite low value to put the PMOS P1 in saturation (Vout < 0.3 V).

Accordingly, the equations of the currents for the three MOSs would be as follows.

$$I_{D,P1} = 30*10^{-6}*1*\left(\frac{(-1+0.3)^2}{2}\right).$$

$$I_{D,N1} = 60*10^{-6}*2*\left((1.0-0.3-vx)*(vout-vx)-\frac{(vout-vx)^2}{2}\right).$$

$$I_{D,N2} = 60*10^{-6}*2*\left((1.0-0.3)*vx-\frac{vx^2}{2}\right).$$

Solving for $I_{D,P1} = I_{D,N2}$ we get vx = 0.0938. Then using $I_{D,P1} = I_{D,N1}$ we get vout = 0.2050. Since our assumptions $V_X < 0.7$ and $V_{out} < 0.3$ have come correct, we are right about our assumptions. So the results are

P1: saturation
N1: linear
N2: linear
V_X = 0.0938 V
V_{out} = 0.2050 V.

Since it is cumbersome to first figure out the regions of operation for the MOSs, to subsequently solve the equations, and then to cross-check the validity of our assumption, it makes sense to write an automated program for the steps. Such an automated program is given next. However, we should have an at least rough understanding of the circuit at hand first.

```
%
% The program finds the regions of operation (linear/saturation) for the
% transistors in a 2-input NAND gate (pseduo-NMOS style) with ints two
% inputs connected together
%
% by Kuntal Roy
% ECE Dept., Purdue University
% royk@purdue.edu
% Date: 24-Sep-2009
%

clear all
close all

% These values are hardcoded in the equations
% However, you can use num2str for all the variables like vin as below

vdd = 1;        % in V
kpd = 30;       % in uA/V2
knd = 60;       % in uA/V2
vtp = -0.3;     % in V
vtn = 0.3;      % in V
wplp = 1;
wnln = 2;

% use vin values more that vtn
vin = [0.31 0.4:0.1:1.0];

cond = ['l' 's'];   % 'l' for linear and 's' for saturation

% current equations for PMOS
p_lin = '30*1*((-1+0.3)*(vout-1)-(vout-1)^2/2)';  %
p_sat = '30*1*((-1+0.3)^2/2)';

% To be able to simulate for multiple VINs, use num2str inside for loop
% as below

% vin = 0.7;
% n1_lin = '60*2*((0.7-0.3-vx)*(vout-vx) - (vout-vx)^2/2)';
% n1_sat = '60*2*((0.7-0.3-vx)^2/2)';
%
% n2_lin = '60*2*((0.7-0.3)*vx - vx^2/2)';
% n2_sat = '60*2*((0.7-0.3)^2/2)';

for ivin = vin

    matched  = 0;

    % current equations for NMOS 1 (upper one)
    n1_lin = strcat( ...
    '60*2*((', num2str(ivin, '%4.2f'),'-0.3-vx)*(vout-vx)-(vout-vx)^2/2)');
    n1_sat = strcat('60*2*((', num2str(ivin, '%4.2f'),'-0.3-vx)^2/2)');

    % current equations for NMOS 2 (below one)
```

```
n2_lin = strcat('60*2*((', num2str(ivin, '%4.2f'),'-0.3)*vx-vx^2/2)');
n2_sat = strcat('60*2*((', num2str(ivin, '%4.2f'),'-0.3)^2/2)');

for icondp = cond            % pmos
    for icondn1 = cond       % nmos1
        for icondn2 = cond   % nmos2

            % selecting the equations for the corresponding region of
            % operation
            switch icondp
                case  'l'
                    pmoseq = p_lin;
                case  's'
                    pmoseq = p_sat;
                otherwise
                    disp('Unknown region of opearion!')
                    return
            end

            switch icondn1
                case  'l'
                    nmos1eq = n1_lin;
                case  's'
                    nmos1eq = n1_sat;
                otherwise
                    disp('Unknown region of opearion!')
                    return
            end

            switch icondn2
                case  'l'
                    nmos2eq = n2_lin;
                case  's'
                    nmos2eq = n2_sat;
                otherwise
                    disp('Unknown region of opearion!')
                    return
            end

            % preparing two equations from three currents
            eq1 = strcat(pmoseq, '=', nmos1eq);
            eq2 = strcat(pmoseq, '=', nmos2eq);

            % solving the equations
            [vout_op, vx_op] = solve(eq1, eq2);

            % there may be multiple roots
            for ilop = 1:length(vout_op)

                % converting sym to double
                svout_op = double(vout_op(ilop));
                svx_op = double(vx_op(ilop));

                % ignore if imaginary solution
                if ~isreal(svout_op) || ~isreal(svx_op)
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```
                    continue;
                end

                % ignore if negative or values greated than vdd
                if svout_op < 0 || svout_op > vdd || ...
                        svx_op < 0 || svx_op > vdd
                    continue;
                end

                % determine vgs and vds for all the transistors
                vgsp = (0-vdd);         vdsp = (svout_op-vdd);
                vgsn1 = (ivin-svx_op);  vdsn1 = (svout_op-svx_op);
                vgsn2 = ivin;           vdsn2 = svx_op;

                % detrmining the region of operation for the
                % transistors
                if vgsp >= vtp    % cutoff
                    continue;
                else
                    if vdsp > vgsp-vtp
                        pmos_cond = 'l';
                    else
                        pmos_cond = 's';
                    end
                end

                if vgsn1 <= vtn   % cutoff
                    continue;
                else
                    if vdsn1 < vgsn1-vtn
                        nmos1_cond = 'l';
                    else
                        nmos1_cond = 's';
                    end
                end

                if vgsn2 <= vtn   % cutoff
                    continue;
                else
                    if vdsn2 < vgsn2-vtn
                        nmos2_cond = 'l';
                    else
                        nmos2_cond = 's';
                    end
                end

                % checking the condition that if the assumed conditions
                % are correct or not
                if pmos_cond == icondp && nmos1_cond == icondn1 ...
                        && nmos2_cond == icondn2
                    disp(sprintf('Matched: vin: %6.4f\tvout:
%6.4f\tvx:%6.4f\tpmos: %c\tnmos1: %c\tnmos2: %c', ...
                        ivin, svout_op, svx_op, pmos_cond, nmos1_cond,
nmos2_cond))
                    matched = 1;
```

```
                    break;
                end
            end

            if matched == 1
                break;
            end
        end

        if matched == 1
            break;
        end
    end

    if matched == 1
        break;
    end
end
end
```

Results

Vin (V)	Vout (V)	Vx (V)	PMOS P1	NMOS N1	NMOS N2
0.31	0.9999	0.0029	linear	saturation	linear
0.40	0.9856	0.0293	linear	saturation	linear
0.50	0.9403	0.0586	linear	saturation	linear
0.60	0.8568	0.0879	linear	saturation	linear
0.70	0.7123	0.1172	linear	saturation	linear
0.80	0.4000	0.1394	linear	linear	linear
0.90	0.2609	0.1127	saturation	linear	linear
1.00	0.2050	0.0938	saturation	linear	linear

Note that for Vin = 0.8 V, all the MOSs are in *linear* region which would have been very difficult to solve by hand.