

Exam 3

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

December 3, 2009

Name: _____

PUID: _____

Instructions: It is important that you clearly show your work and mark the final answer clearly, closed book, closed notes, no calculator.

Time: **1 hour 15 minutes**

Scoring

Problem 1 (Total 30 points)

Part a) 20 points _____

Part b) 10 points _____

Problem 2 (Total 30 points)

Part a) 15 points _____

Part b) 15 points _____

Problem 3 (Total 40 points)

Part a) 20 points _____

Part b) 20 points _____

Total: 100 points _____

Problem 1: Consider an inverter of minimum size (input capacitance of C_i) driving a load C_L , which is x times large as C_i ($C_L = x.C_i$). The width of the PMOS transistor is a times larger than the NMOS transistor. You decide to introduce another inverter (transistor widths are u times larger than the first for both PMOS and NMOS) between the minimum sized inverter and the load C_L .

Answer the following questions. Clearly state your assumptions, if any.

[30 points]

a) What should u be to minimize the delay? Show your calculations.

[20 points]

b) If $x = 5$, does it make sense to introduce the second inverter? Explain your answer. (Without explanation, you will not get any points.)

[10 points]

Problem 2: Consider a standard 6-T SRAM cell as shown in the below diagram. Due to *Random Dopant Fluctuation (RDF)*, transistors in a single cell may have different *threshold voltages* than that of what was designed for. Assume that the cell is designed for

$$V_{DD} = 1 \text{ V}, V_{tn} = 0.3 \text{ V}, V_{tp} = -0.3 \text{ V}.$$

Consider that due to *RDF*, a variation of $\pm 30 \text{ mV}$ in threshold voltage can happen.

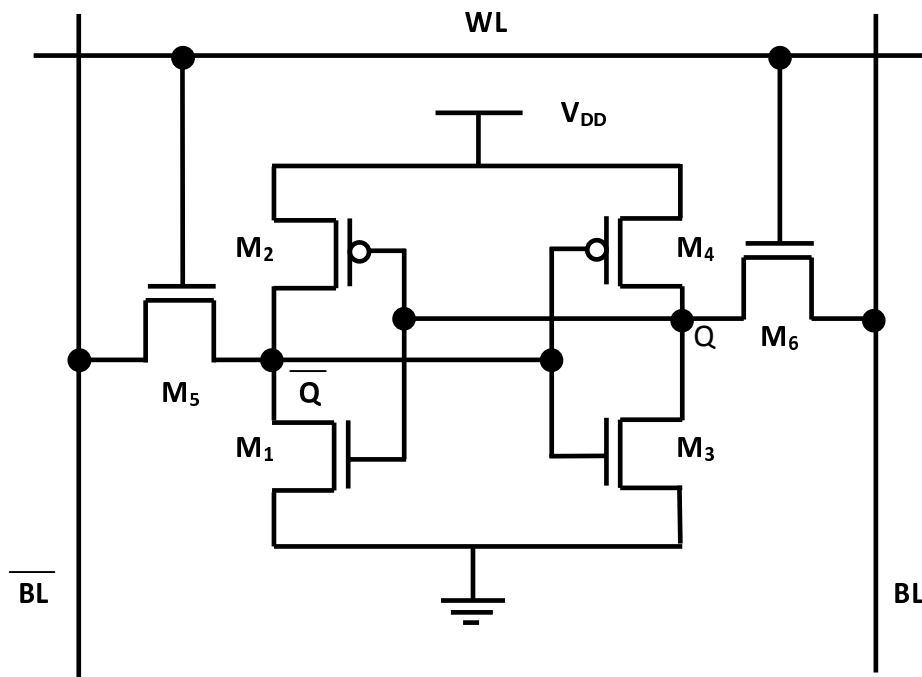
Clearly and concisely answer the following questions with explanation. Write your assumptions, if any. [30 points]

a) Determine the threshold voltages of *all the transistors* for *worst case read operation*.

[15 points]

b) Determine the threshold voltages of *all the transistors* for *worst case write operation*.

[15 points]



Problem 3: Consider a *10-bit* NAND row address decoder with *2-bit pre-decoder* for a memory array. Answer the following questions. Write your assumptions, if any.

[40 points]

- a) Design the decoder and draw the corresponding schematic diagram. (You don't need to draw the complete diagram, but draw *enough* so that it's clear.) **[20 points]**
- b) Using the *Elmore delay model*, determine the approximate delay improvement compared to the case when the pre-decoder is not used. **[20 points]**

Scratch Paper 1

Scratch Paper 2