Exam 2

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

November 5, 2009

Name: SOLUTION

PUID: _____

Instructions: It is important that you clearly show your work and mark the final answer clearly, closed book, closed notes, no calculator.

Time: 1 hour 15 minutes

Scoring

Problem 1 (Total 30 points)

Part a) 10 points _____

Part b) 10 points _____

Part c) 10 points _____

Problem 2 (Total 40 points)

Part a) 10 points _____

Part b) 10 points _____

Part c) 10 points _____

Part d) 10 points _____

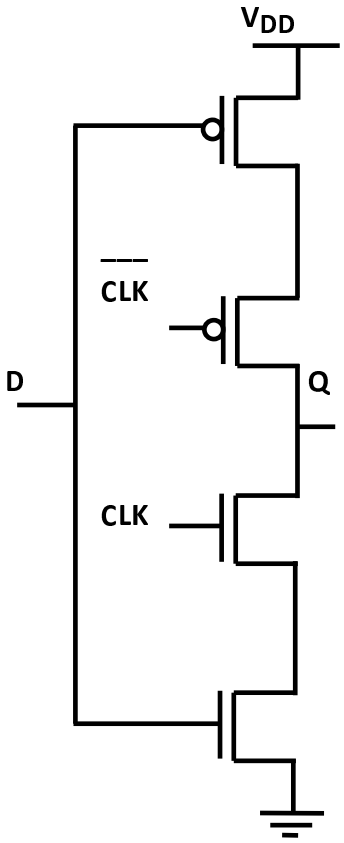
Problem 3 (30 points) _____

Total: 100 points _____

Problem 1: **[30 points]**

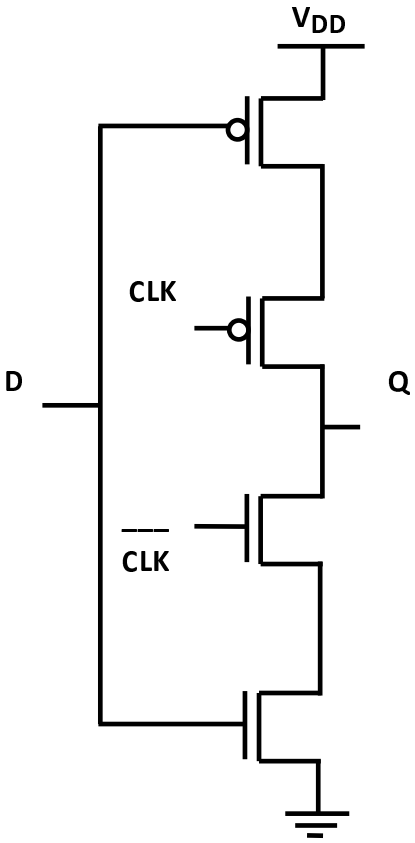
Part a) Draw *positive* and *negative* C^2MOS latches. Clearly show the applied clock signals. **[10 points]**

Solution:



Positive Latch

(as it is transparent when CLK = 1)

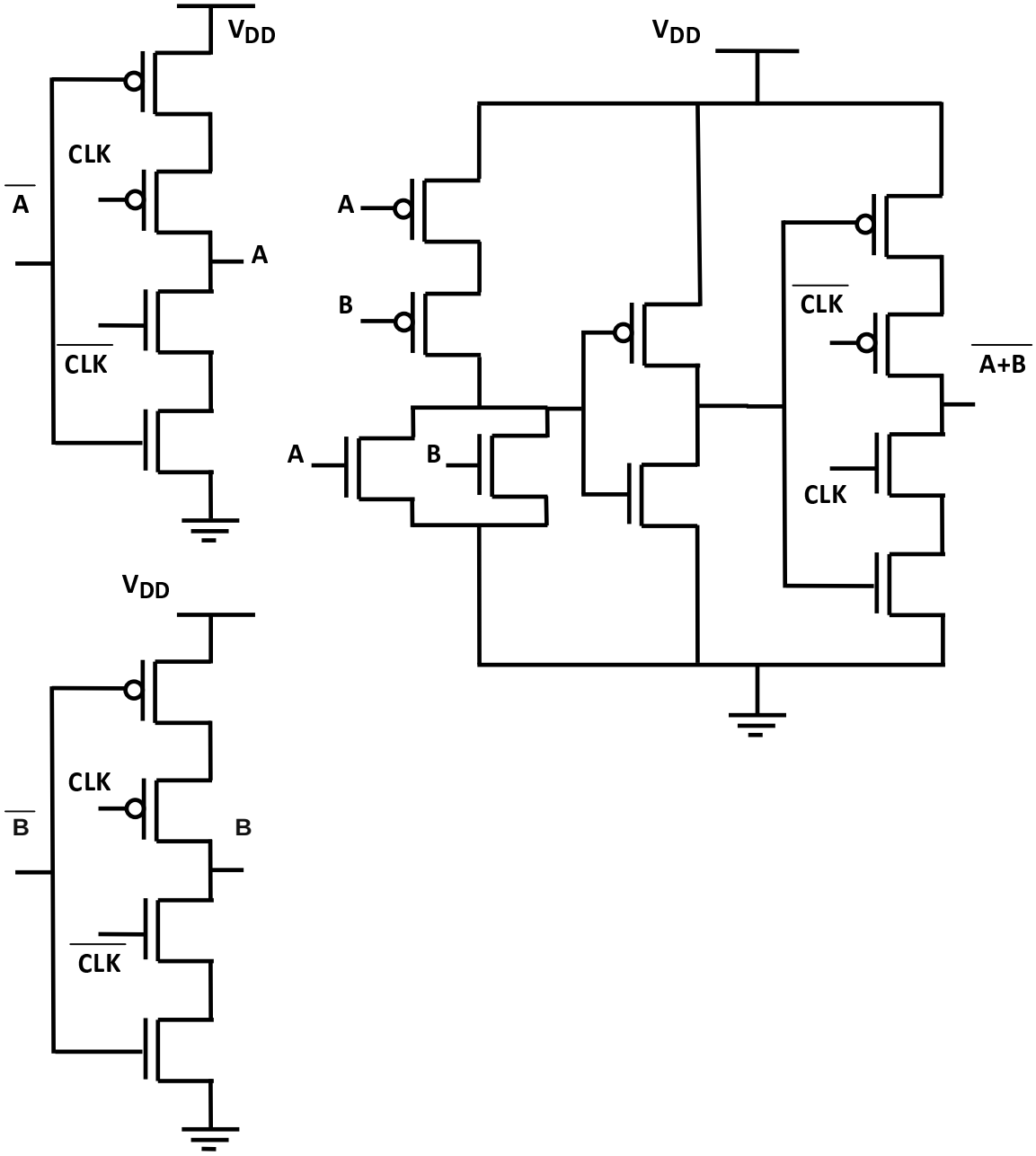


Negative Latch

(as it is transparent when CLK = 0)

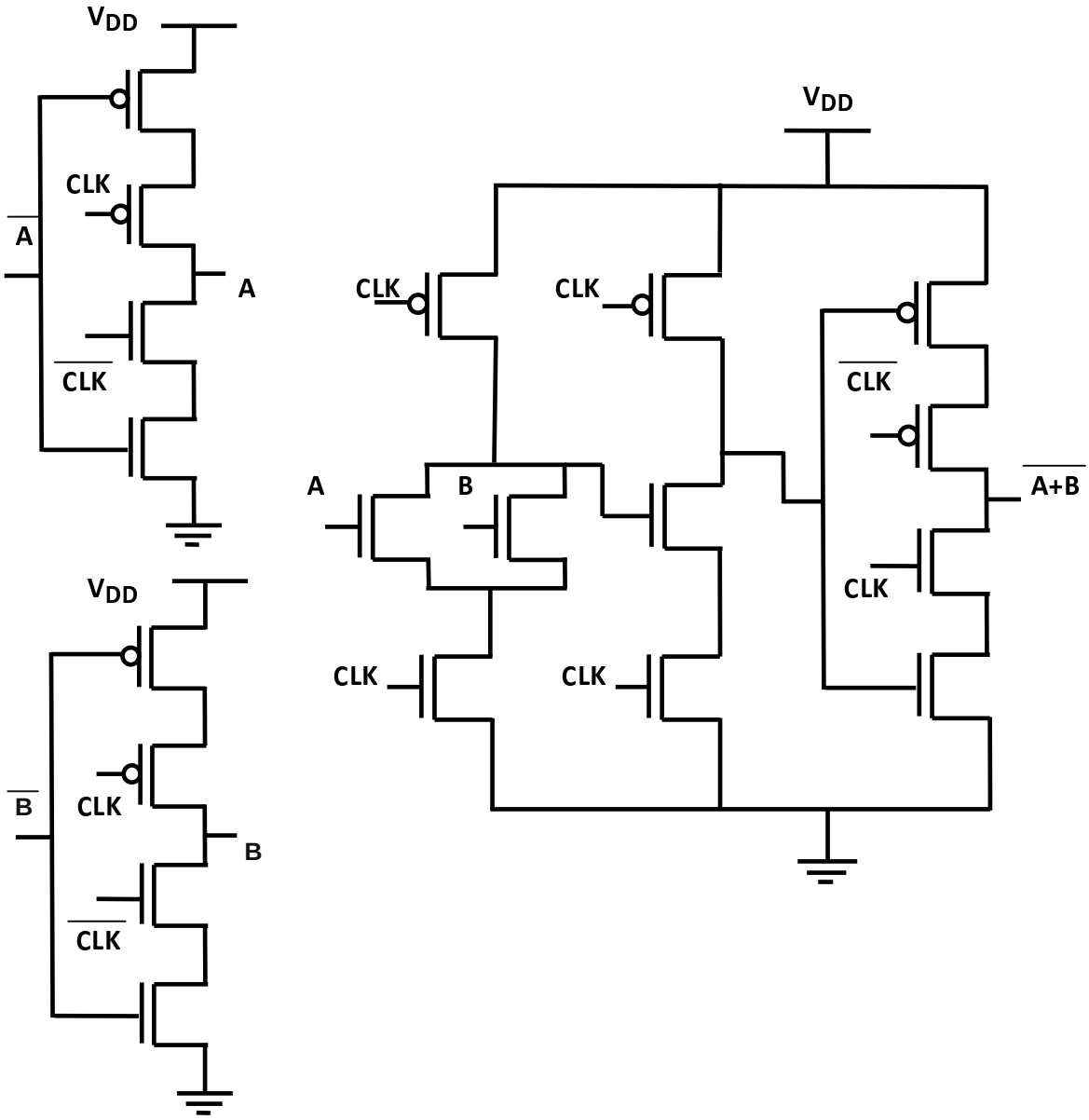
Part b) Implement NOR operation **using static logic** as a pipelined datapath using C^2MOS latches that *avoids any race-condition due to clock overlaps*. Clearly draw all the transistors and the applied clock signals in your diagram. Write your assumptions, if any. **[10 points]**

Solution: C^2MOS latches are inverting. In a pipelined datapath we can *assume* that we are getting inverted signals at the inputs of the latches that will be again inverted to get the non-inverted inputs. To avoid race condition due to clock overlaps, we need to have *non-inverting* logic functions between the latches. So we have to add one inverter stage in between the latches. We can design the subsequent stages depending on what logic function we have at the next stage or if it's the primary output, we are done.



Part c) Implement NOR operation **using dynamic logic** as a pipelined datapath using C^2MOS latches that *avoids any race-condition due to clock overlaps*. Clearly draw all the transistors and the applied clock signals in your diagram. Write your assumptions, if any. **[10 points]**

Solution: C^2MOS latches are inverting. In a pipelined datapath we can *assume* that we are getting inverted signals at the inputs of the latches that will be again inverted to get the non-inverted inputs. To avoid race condition due to clock overlaps, we need to have *non-inverting* logic functions between the latches. So we have to add one inverter stage in between the latches. We can design the subsequent stages depending on what logic function we have at the next stage or if it's the primary output, we are done. For dynamic logic, we should make sure that when the dynamic logic is evaluating, the latch that is followed-by is in transparent mode. Charge loss due to cascading of the dynamic gates is assumed to be non-substantial.



Problem 2: Consider the edge-triggered register shown below. Clearly and concisely answer the following questions with explanation. Write your assumptions, if any.

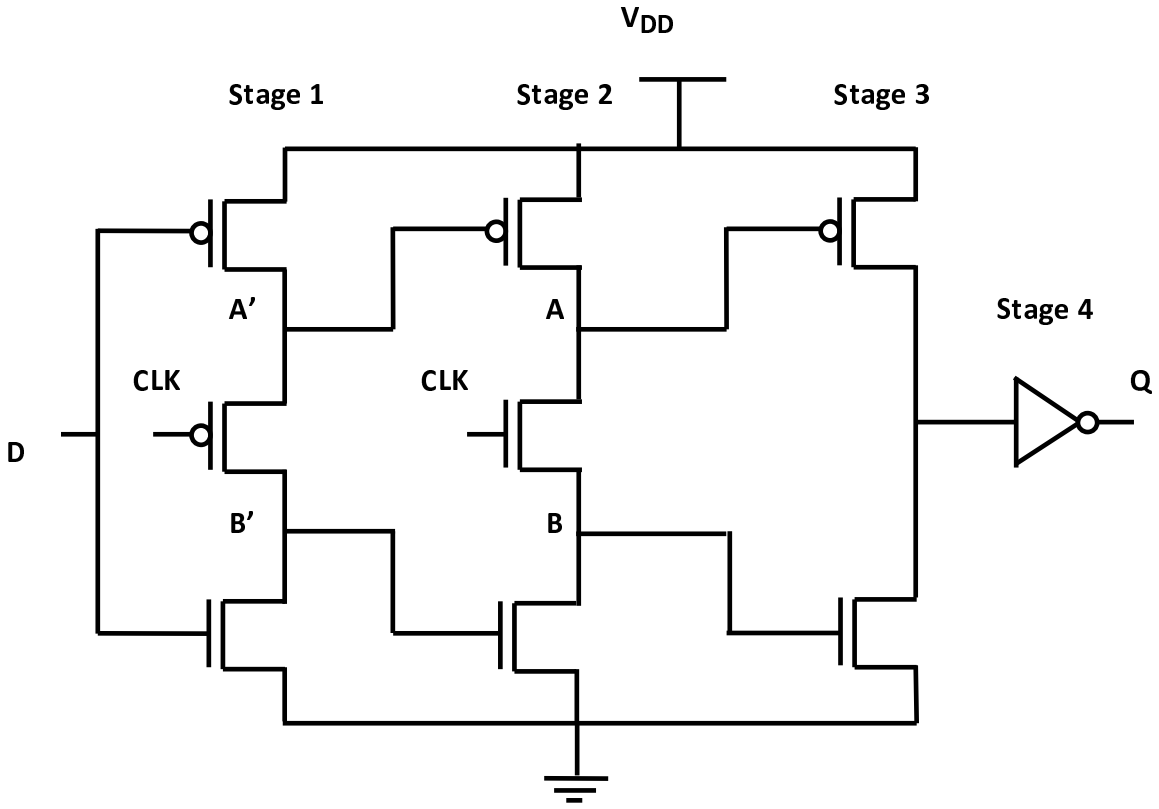
[40 points]

a) What are the minimum and maximum voltages possible at the nodes A and B? **[10 points]**

b) Determine the set-up time. **[10 points]**

c) Determine the propagation delay. **[10 points]**

d) Determine the hold time. **[10 points]**



Solution:

a) $V_{A',\,min} = |V_{tp}|$, $V_{A',\,max} = V_{DD}$, $V_{B',\,min} = 0$, $V_{B',\,max} = V_{DD}$.

It needs explanation for $V_{A',\,min} = |V_{tp}|$. When D = V_{DD} and CLK = 0, at $V_{A'} = |V_{tp}|$, current stops flowing through the series-connected MOSs at stage 1, so $V_{A'}$ remains at $|V_{tp}|$.

Accordingly, $\mathbf{V_{A,\,min} = 0}$, $\mathbf{V_{A,\,max} = V_{DD}}$, $\mathbf{V_{B,\,min} = 0}$, $\mathbf{V_{B,\,max} = V_{DD} - V_{tn}}$.

We have assumed that $V_{A',\,min} = |V_{tp}|$ is low enough to have $V_{A,\,max} = V_{DD}$ which normally is quite a good assumption.

It needs explanation for $V_{B,\,max} = V_{DD} - V_{tn}$. When $V_{A'} = |V_{tp}|$, $V_{B'} = 0$, and CLK = V_{DD}, at $V_B = V_{DD} - V_{tn}$, current stops flowing through the series-connected MOSs at stage 2, so V_B remains at $V_{DD} - V_{tn}$.

b) Setup time is the time for the nodes A'/B' to be valid that is **one inverter delay corresponding to stage 1**.

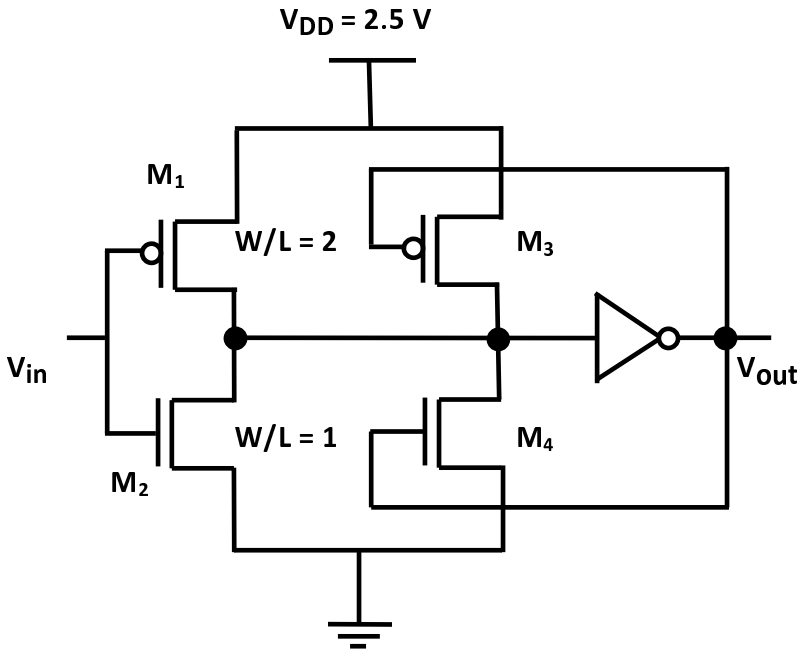
c) Propagation delay is the time for the value at node A'/B' to propagate at the output Q that is **three inverter delays corresponding to stage 2, stage 3, and stage 4**.

d) After the rising edge of clock occurs, input D must be kept stable until the values at the nodes A and B get stable corresponding to the values we have at nodes A' and B'. If D changes, the values at the nodes A'/B' would change and that will in turn affect the node values at A and B. So the hold time is **one inverter delay corresponding to stage 2**.

To be specific, the hold time should be **less than one inverter delay corresponding to stage 2** because it takes one inverter delay corresponding to stage 1 for D to change voltage levels at nodes A' and B'.

Problem 3: Consider the Schmitt trigger circuit shown below. Find the widths of the transistors M_3 and M_4 to have V_{M-} = 1 V and V_{M+} = 2 V. Clearly write the *regions of operation* of the transistors during your calculation and write your assumptions, if any.

[30 points]



$K_p' = \mu_p C_{ox}$ = 50e-6 A/V^2

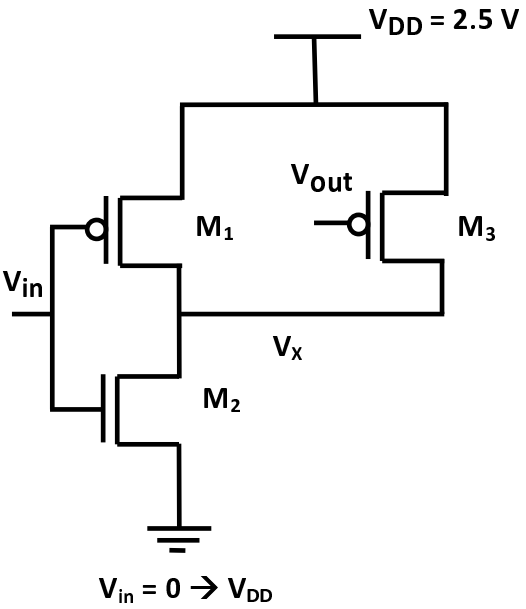
$K_n' = \mu_n C_{ox}$ = 100e-6 A/V^2

V_{tp} = -0.5 V, V_{tn} = 0.5 V

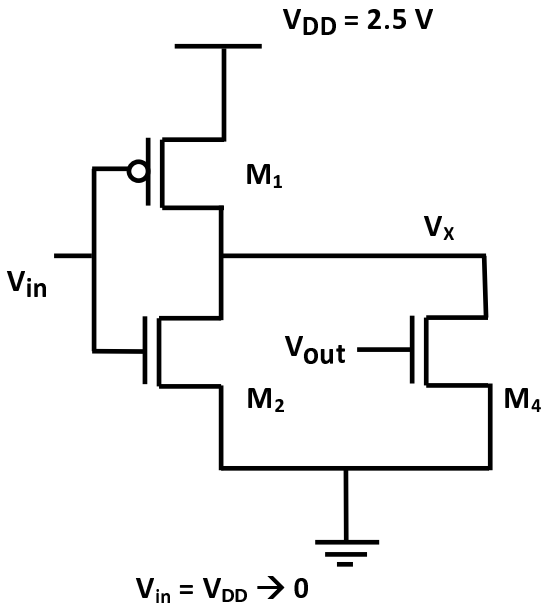
L = 300 nm

Solution:

When we start from V_{in} = 0, we have V_{out} = 0 and consequently M_3 comes into action. When we start from $V_{in} = V_{DD}$, we have $V_{out} = V_{DD}$ and consequently M_4 comes into action.



$V_{in} = 0 \rightarrow V_{DD}$



$V_{in} = V_{DD} \rightarrow 0$

Case $V_{in} = 0 \rightarrow V_{DD}$

When $V_{in} = V_{M+} = 2$ V, $V_X = V_{M+} = 2$ V.

$V_{GS,M1} = (2 – 2.5)$ V = -0.5 V = V_{tp}.

Accordingly, we can assume that the transistor M1 is in cutoff (note that we can tell that the transistor M1 is in saturation as well as $V_{DS,\ M1} = (V_X – 2.5) = -0.5\ V < V_{GS,M1} - V_{tp} = 0$). So the transistor **M1 is at the boundary of cut-off and saturation region**. $I_{D,\ M1} = 0$.

$V_{GS,M2} = (2 – 0)$ V = 2 V > V_{tn} = 0.5 V. So M2 is ON. **M2 is in saturation region** since

$V_{DS,\ M2} = (V_X – 0) = 2\ V > V_{GS,M2} - V_{tn} = (2 – 0.5) = 1.5$ V.

We will assume sharp transition of the output, V_{out}. Since we have started from $V_{out} = 0$, we will assume that V_{out} is still at 0.

$V_{GS,M3} = (0 – 2.5)$ V = -2.5 V < V_{tp} = -0.5 V. So M3 is ON.

$V_{DS,\ M3} = (V_X – 2.5) = -0.5\ V > V_{GS,M3} - V_{tp} = (-2.5 + 0.5)$ V = -2 V. So **M3 is in linear region**.

$$I_{D,M1} + I_{D,M3} = I_{D,M2}$$

$$\Rightarrow 0 + 50 * \left(\frac{W}{L}\right)_3 * \left((-2.5+0.5)(-0.5) - \frac{(-0.5)^2}{2} \right) = 100 * 1 * \frac{(2-0.5)^2}{2}$$

$$\Rightarrow \left(\frac{W}{L}\right)_3 = \frac{1.5*1.5}{1-0.125} \simeq \frac{1.5*1.5}{0.9}$$

$$\Rightarrow W_3 = \frac{2.25*300}{0.9} nm = 750\, nm$$

$W_3 = 750$ nm

Case $V_{in} = V_{DD} \rightarrow 0$

When $V_{in} = V_{M-} = 1$ V, $V_X = V_{M-} = 1$ V.

$V_{GS,M1} = (1 - 2.5)$ V = -1.5 V < V_{tp} = -0.5 V. So M1 is ON.

$V_{DS,\,M1} = (V_X - 2.5)$ = -1.5 V < $V_{GS,M1} - V_{tp}$ = -1 V. So the transistor **M1 is in saturation region**.

$V_{GS,M2} = (1 - 0)$ V = 1 V > V_{tn} = 0.5 V. So M2 is ON. **M2 is in saturation region** since

$V_{DS,\,M2} = (V_X - 0)$ = 1 V > $V_{GS,M2} - V_{tn} = (1 - 0.5)$ V = 0.5 V.

We will assume sharp transition of the output, V_{out}. Since we have started from V_{out} = 2.5 V, we will assume that V_{out} is still at 2.5 V.

$V_{GS,M4} = (2.5 - 0)$ V = 2.5 V > V_{tn} = 0.5 V. So M4 is ON. **M4 is in linear region** since

$V_{DS,\,M4} = (V_X - 0)$ = 1 V < $V_{GS,M4} - V_{tn} = (2.5 - 0.5)$ = 2 V.

$$I_{D,M1} = I_{D,M2} + I_{D,M4}$$

$$\Rightarrow 50*2*\frac{(-1.5+0.5)^2}{2} = 100*1*\frac{(1-0.5)^2}{2} + 100*\left(\frac{W}{L}\right)_4 *\left((2.5-0.5)(1) - \frac{(1)^2}{2}\right)$$

$$\Rightarrow 0.5 = 0.125 + \left(\frac{W}{L}\right)_4 *1.5$$

$$\Rightarrow \left(\frac{W}{L}\right)_4 = \frac{0.375}{1.5} = \frac{0.75}{3}$$

$$\Rightarrow W_4 = \frac{0.75*300}{3} nm = 75\,nm$$

W_4 = 75 nm

W_4 has come out to be less than L = 300 nm. It would not be quite allowable by a technology library. So for proper operation of the Schmitt trigger circuit, we need to make the width of the transistor M1 higher so that the W_4 conforms at least to the *minimum* specification of transistor widths provided by a technology library.