EE595S Notes - ACSL
Fall 2005

Largely Taken w/o Permission
From ESAC ACSL Course
Section 3: More ACSL Features
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7/7/98 - 7/10/98

More ACSL Features

- SCHEDULE Operator and DISCRETE Blocks
- IF THEN Constructs
- PROCEDURAL Blocks
- MACRO Facilities

SCHEDULE Operator and DISCRETE BLOCKS

- Forms:
  - SCHEDULE block/flag .AT. time-expression
  - SCHEDULE block/flag .XZ. real-expression
  - SCHEDULE block/flag .XP. real-expression
  - SCHEDULE block/flag .XN. real-expression
- Where:
  - block = optional name of DISCRETE block
  - flag = optional flag set true when event occurs
  - .AT. = time to schedule event (cannot be in DERIVATIVE block)
  - .XP. = positive zero crossing (must be used in DERIVATIVE block)
  - .XN. = negative zero crossing (must be used in DERIVATIVE block)
  - .XZ. = zero crossing (must be used in DERIVATIVE block)

Example 1: A Basketball

- Dynamics:

$$pv = -g$$

$$px = v$$

- Collision:

$$v\,|_{after} = -kv\,|_{before}$$

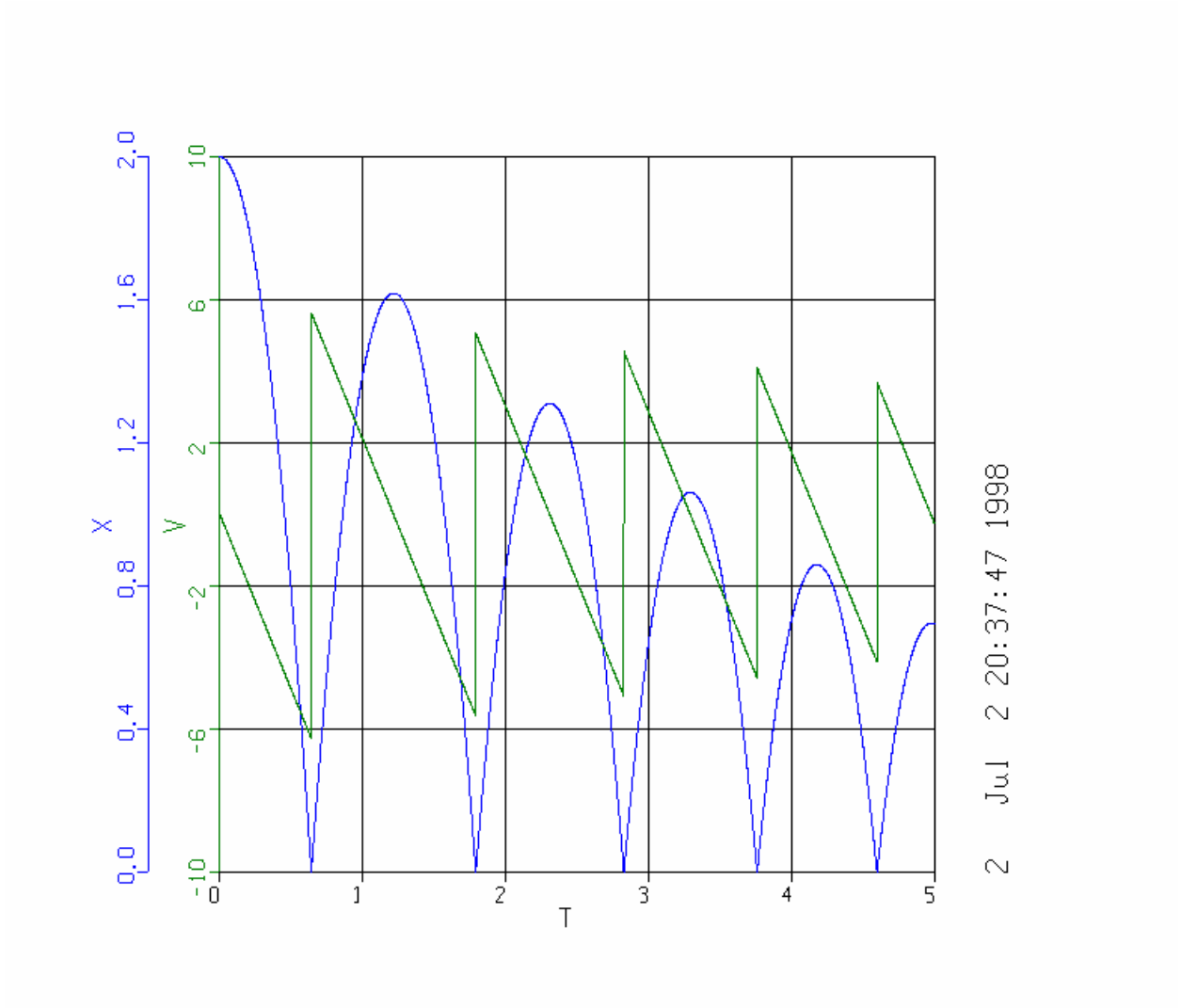
Basket.csl

```
PROGRAM BASKET

   DERIVATIVE

      ALGORITHM IALG=4
      MAXTERVAL MAXT=1.0e-3
      MINTERVAL MINT=1.0e-6
      CINTERVAL CINT=1.0e-3
      CONSTANT tstop=5.0
      TERMT(t .GT. tstop,'Exit on Tstop')

      CONSTANT g=9.8        !  acceleration due to gravity m/s
      CONSTANT v0=0.0       !  initial velocity, m/s
      CONSTANT x0=2.0       !  initial height m
      CONSTANT k=0.9        !  rebound coefficient

      ! dynamic model of basketball
      pv=-g
      v=INTEG(pv,v0)
      px=v
      x=INTEG(v,x0)

         ! the floor is at height 0
         SCHEDULE HITFLOOR .XN. x
    END

    DISCRETE HITFLOOR
       v=-k*v
    END

END
```

Basket.cmd

```
s weditg=.f.
s hvdprn=.f.
prepare /all
```

Results



Example 2: Squarewave Voltage Source Feeding RL Load

- Circuit:

- Dynamics:

$$pi = (v - ri) / L$$

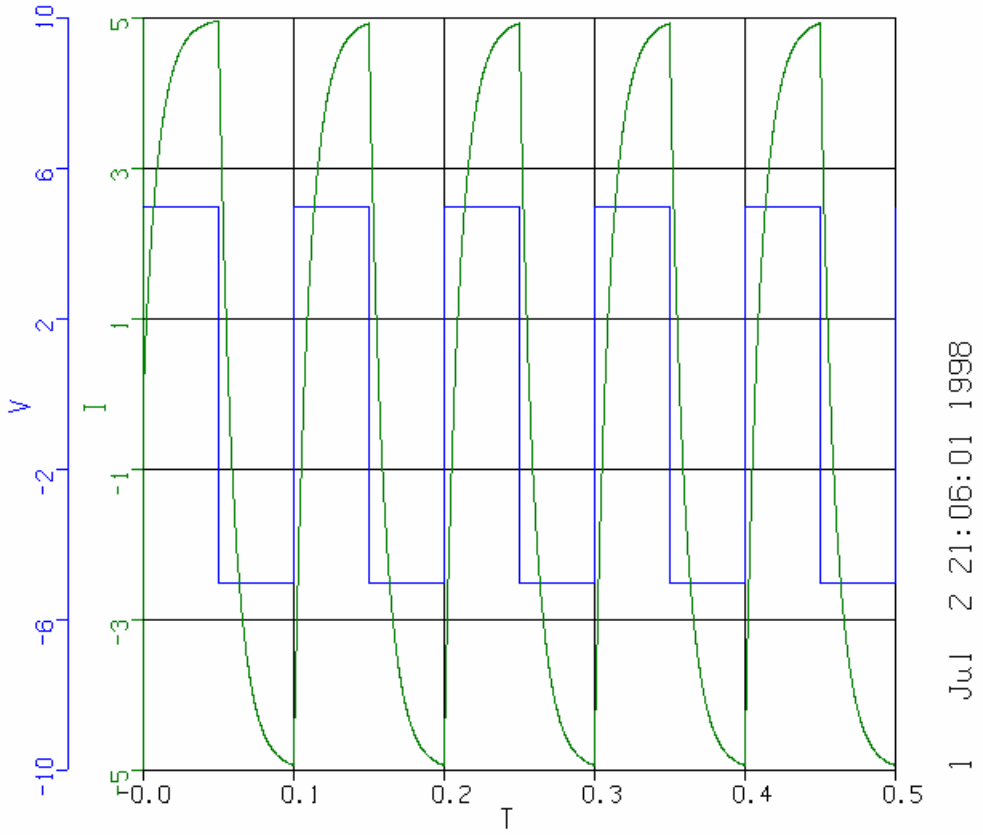
Square.csl

```
PROGRAM SQUARE

   DERIVATIVE

      ALGORITHM IALG=4
      MAXTERVAL MAXT=1.0e-4
      MINTERVAL MINT=1.0e-6
      CINTERVAL CINT=1.0e-4
      CONSTANT tstop=0.5
      TERMT(t .GT. tstop,'Exit on Tstop')

      ! dynamic model of rl load
      CONSTANT l=10.0e-3          ! Inductance in H
      CONSTANT r=1.0              ! Resistance in Ohms
      CONSTANT i0=0.0             ! Initial current in A
      pi=(v-r*i)/l                ! Time derivative of current A/s
      i=INTEG(pi,i0)              ! Current, A
```

Square.csl (cont.)

```
      ! voltage source
      CONSTANT vmag=5.0                    ! Voltage magnitude
      CONSTANT freq=10.0                   ! Frequency
      INITIAL
         halfperiod=1.0/(2.0*freq);        ! Half-Period
         v=vmag                            ! Inital Voltage
         SCHEDULE CHNGSGN .AT. t+halfperiod! Schedule First Sign Change
      END

   END

   DISCRETE CHNGSGN
      v=-v                                 ! Change sign of voltage
      SCHEDULE CHNGSGN .AT. t+halfperiod   ! Schedule next change
   END  ! Discrete Block

END  ! Program
```

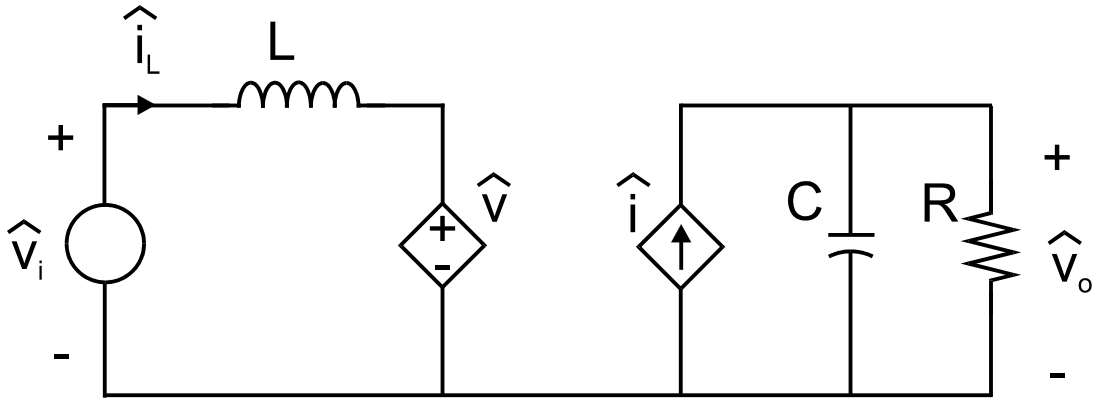
Results:



ACSL MACRO LANGUAGE

- Primary means of constructing well organized code
- Primary means of constructing component model libraries

Example: NLAM Model of DC/DC Converter



$$\hat{v} = d\hat{v}_o \qquad \hat{i} = d\hat{i}_L$$

Switch Average Value Model

Switch Average Value Model (Cont)

ADCDC1.CSL

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                      "
"            1285 Electrical Engineering Building                  "
"            Purdue University                                     "
"            West Lafayette, IN 47905-1285                         "
"            (765) 494-3246                                        "
" For:       ACSL Short Course                                     "
" Date:      7/6/98                                                "
" Version:   1.0                                                   "
"                                                                   "
"-------------------------------------------------------------------"

INCLUDE '../macros/adcdc.mac'

PROGRAM ADCDC1

   DERIVATIVE

      ALGORITHM IALG=4
      MAXTERVAL MAXT=1.0e-4
      CINTERVAL CINT=1.0e-4
      TERMT(t .GE. tstop,'Terminated on Tstop')
      CONSTANT tstop=0.2
```

ADCDC1.CSL (Cont.)

```
      "ideal power source"
      CONSTANT vin=300.0

      "no control"
      CONSTANT d=1.0

      "dc/dc converter"
      ADCDC(con1,d,vin,iout,vout,iin, &
            "lcon1=5.0e-3","rlcon1=0.1","ccon1=100.0e-6")

      "resistive load on converter"
      CONSTANT rload=20.0
      iout=vout/rload

   END ! Derivative

END ! Program
```

ADCDC.MAC

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                      "
"            1285 Electrical Engineering Building                  "
"            Purdue University                                     "
"            West Lafayette, IN 47905-1285                         "
"            (765) 494-3246                                        "
" For:       ACSL Short Course                                     "
" Date:      7/6/98                                                "
" Version:   1.0                                                   "
"                                                                   "
"-------------------------------------------------------------------"
"-------------------------------------------------------------------"
"                                                                   "
"       MACRO: ADCDC                                                "
" DESCRIPTION: NLAM model of two quadrant dc/dc converter           "
"                                                                   "
"                             CONCATENATION                         "
"                                                                   "
"    z          -     identifier                                   "
"                                                                   "
"                                                                   "
```

ADCDC.MAC (Cont)

```
"                                INPUTS                                  "
"                                                                        "
"    d           -     duty cycle (upper switch on over total period)   "
"    vin         -     input voltage (V)                                "
"    iout        -     current out of output terminal (A)               "
"                                                                        "
"                               OUTPUTS                                  "
"                                                                        "
"    vout        -     output voltage (V)                               "
"    iin         -     current into input terminal (A)                  "
"                                                                        "
"                              PARAMETERS                                "
"                                                                        "
"    l&z         -     inductance of leg inductor (H)                   "
"    rl&z        -     resistance of leg inductor (Ohms)                "
"    c&z         -     output capacitance (F)                           "
"                                                                        "
"                               INTERNAL                                 "
"                                                                        "
"    vs          -     average voltage across lower switch (V)          "
"    is          -     average current out of upper switch (A)          "
"    p&iin       -     time derivative of iin (A/s)                     "
"    icap&z      -     current into the output capacitor (A)            "
"    p&vout      -     time derivative of vout (V/s)                    "
"                                                                        "
"------------------------------------------------------------------------"
```

ADCDC.MAC (Cont.)

```
MACRO ADCDC(z,d,vin,iout,vout,iin,par_l,par_rl,par_c)

   INITIAL

      CONSTANT par_l
      CONSTANT par_rl
      CONSTANT par_c

   END

   MACRO REDEFINE vs,is

   "compute the average voltage across the lower switch"
   vs=d*vout

   "compute the current out of the upper switch"
   is=d*iin

   "compute the input current"
   p&iin=(vin-vs-rl&z*iin)/l&z
   iin=INTEG(p&iin,0.0)

   "compute the output capacitor current"
   icap&z=is-iout
   p&vout=icap&z/c&z
   vout=INTEG(p&vout,0.0)

MACRO END
```

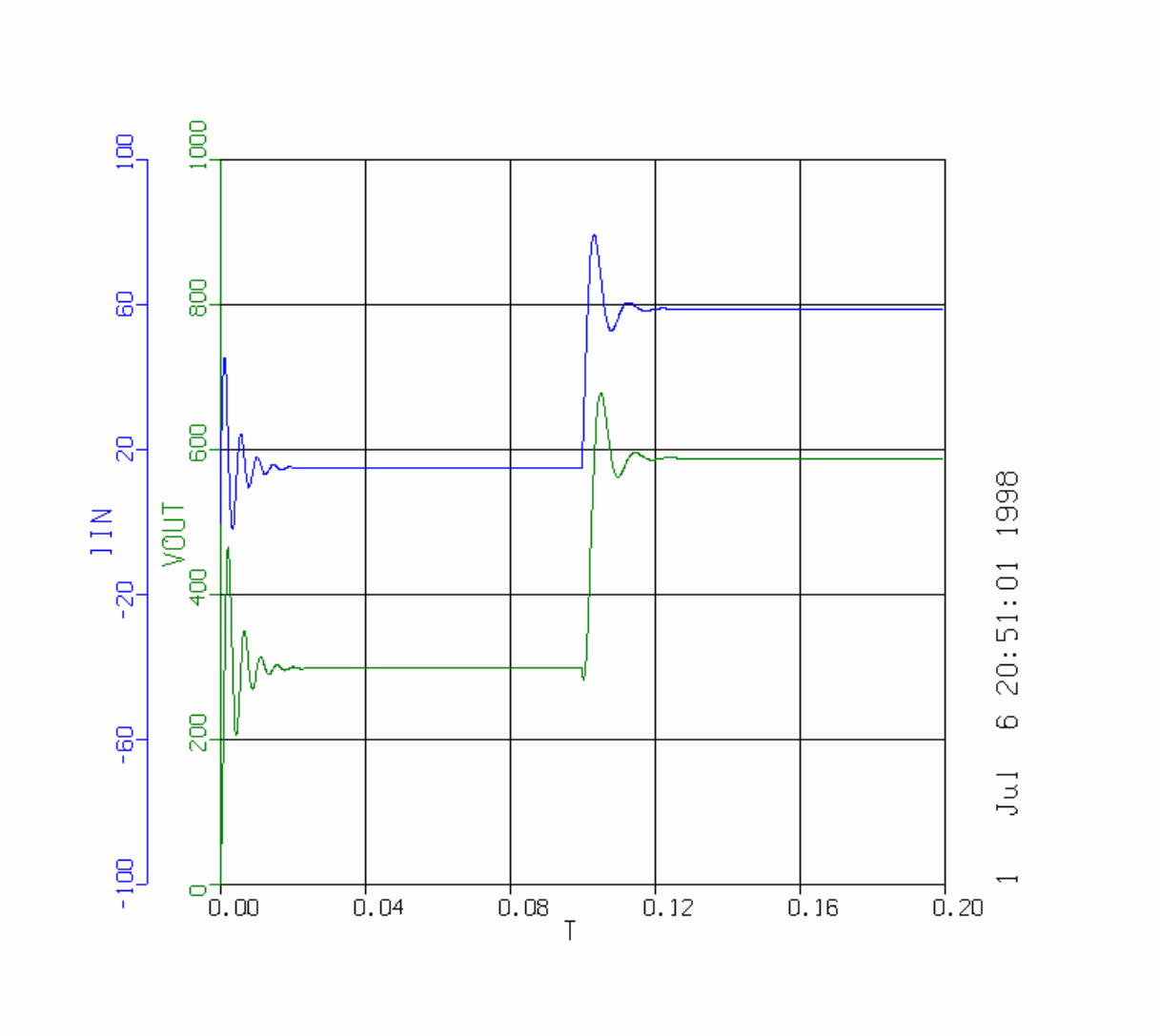
Important Points

- MACRO REDEFINE
- Concatenation (&)
- Concatenation variable (&z)
- INITIAL Section
- Parameter passing
- MACROS can call MACROS
- Extensive MACRO Language Available

ADCDC1.CMD

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                       "
"            1285 Electrical Engineering Building                   "
"            Purdue University                                      "
"            West Lafayette, IN 47905-1285                          "
"            (765) 494-3246                                         "
" For:       ACSL Short Course                                      "
" Date:      7/6/98                                                 "
" Version:   1.0                                                    "
"                                                                   "
"-------------------------------------------------------------------"

s hvdprn=.f.
prepare /all

proced study1

   action/var=0.1/val=0.5/loc=d
   start
   action /clear
   plot iin,vout

end
```

RESULTS (study1)



IF, IF THEN ELSE

- Forms:

```
IF (lexpr) STATEMENT

IF (lexpr) THEN
   block1
ELSE
   block2
END IF
```

IF, IF THEN ELSE

- SORTING RULES
  - Variables on left must be defined for all possible cases, or disaster can result
  - Material in IF THEN construct moved as a block when sorting with variables on the right as inputs and variables on the left as outputs

IF THEN Example

```
IF (x .GT. 0) THEN
    z=sqrt(x)
    y=z**2
ELSE
    y=x**2
    z=2*y
END IF
```

ACSL PROCEDURALS

- Allows user to specify order of operations
- Internal sequence not seen or affected by sorter
- Handy for assigning elements of arrays, for iterative solutions, or situations where you may want to recompute a variable if it goes out of range

PROCEDURAL Constructs

- Syntax

```
PROCEDURAL(x1,x2,..xn = y1,y2)
        unsorted statemens
END
```

- Example

```
PROCEDURAL(v=i1,i3)
   v(1)=3*i1+i3
   v(2)=i1*i3
END
```

PROCEDURAL Constructs

- 2nd Example

```
PROCEDURAL(y=x,z)
   y=x*3-z^2
   IF (y .LT. 0.0) THEN
       y=-y
   END IF
END
```

PROCEDURAL Constructs

- 3rd Example

```
PROCEDURAL(y=x,v,N)
   y=0.0
   DO L10 i=1,N
     y=y+x(i)*v(i)
   L10.. CONTINUE
END
```

Assignment: DCDC Control

ADCDC2.CSL

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                      "
"            1285 Electrical Engineering Building                  "
"            Purdue University                                     "
"            West Lafayette, IN 47905-1285                         "
"            (765) 494-3246                                        "
" For:       ACSL Short Course                                     "
" Date:      7/6/98                                                "
" Version:   1.0                                                   "
"                                                                   "
"-------------------------------------------------------------------"

INCLUDE '../macros/adcdc.mac'
INCLUDE '../macros/dcdcscon.mac'

PROGRAM ADCDC1

   DERIVATIVE

      ALGORITHM IALG=4
      MAXTERVAL MAXT=1.0e-4
      CINTERVAL CINT=1.0e-4
      TERMT(t .GE. tstop,'Terminated on Tstop')
      CONSTANT tstop=0.2
```

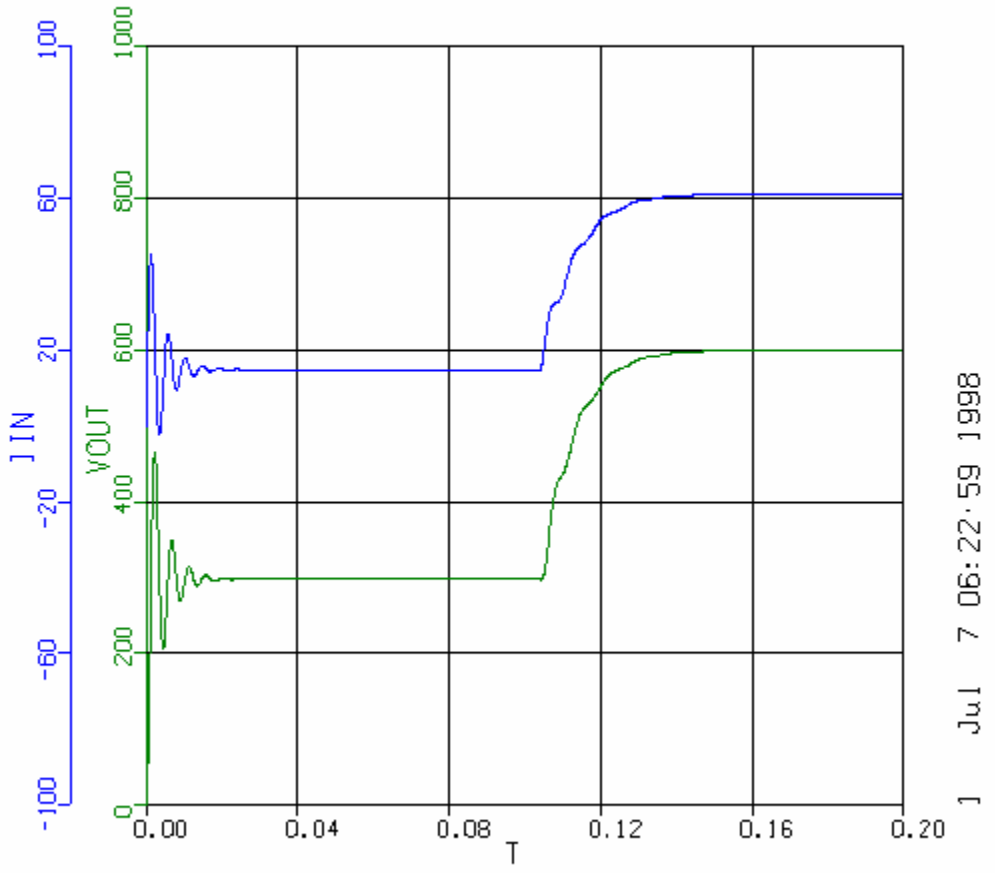
ADCDC2.CSL

```
      "ideal power source"
      CONSTANT vin=300.0

      "simple control"
      CONSTANT vref=300.0
      DCDCSCON(1,vref,vout,d,"k1=1.0e-3","tau1=2.0e-3")

      "dc/dc converter"
      ADCDC(con1,d,vin,iout,vout,iin, &
            "lcon1=5.0e-3","rlcon1=0.1","ccon1=100.0e-6")

      "resistive load on converter"
      CONSTANT rload=20.0
      iout=vout/rload

   END ! Derivative

END ! Program
```

ADCDC2.CMD

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                       "
"            1285 Electrical Engineering Building                   "
"            Purdue University                                      "
"            West Lafayette, IN 47905-1285                          "
"            (765) 494-3246                                         "
" For:       ACSL Short Course                                      "
" Date:      7/6/98                                                 "
" Version:   1.0                                                    "
"                                                                   "
"-------------------------------------------------------------------"

s hvdprn=.f.
prepare /all

proced study1

   action/var=0.1/val=600/loc=vref
   start
   action /clear
   plot iin,vout
   s vref=300.0

end
```

Results:


100
60
20
-20
-60
-100
IIN
1000
800
600
400
200
0
VOUT
0.00
0.04
0.08
0.12
0.16
0.20
T
1 Jul 7 06:22:59 1998

Assignment: Detailed DC/DC Converter Simulation

Coding The Modulator

DCDC1.CSL

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                      "
"            1285 Electrical Engineering Building                  "
"            Purdue University                                     "
"            West Lafayette, IN 47905-1285                         "
"            (765) 494-3246                                        "
" For:       ACSL Short Course                                     "
" Date:      7/6/98                                                "
" Version:   1.0                                                   "
"                                                                   "
"-------------------------------------------------------------------"

INCLUDE '../macros/ddcdc.mac'
INCLUDE '../macros/dcdcscon.mac'

PROGRAM DDCDC1

   DERIVATIVE

      ALGORITHM IALG=4
      MAXTERVAL MAXT=1.0e-4
      MINTERVAL MINT=1.0e-7
      CINTERVAL CINT=1.0e-4
      TERMT(t .GE. tstop,'Terminated on Tstop')
      CONSTANT tstop=0.2
```

DDCDC1.CSL (Cont)

```
      "ideal power source"
      CONSTANT vin=300.0

      "simple control"
      CONSTANT vref=300.0
      DCDCSCON(1,vref,vout,d,"k1=1.0e-3","tau1=2.0e-3")

      "dc/dc converter"
      DDCDC(con1,d,vin,iout,vout,iin, &
            "lcon1=5.0e-3","rlcon1=0.1", &
            "ccon1=100.0e-6","fcon1=5000.0")

      "resistive load on converter"
      CONSTANT rload=20.0
      iout=vout/rload

   END ! Derivative

   "Discrete Blocks associated with DDCDC"
   DDCDCD(con1)

END ! Program
```

DDCDC.MAC (Partially)

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                      "
"            1285 Electrical Engineering Building                  "
"            Purdue University                                     "
"            West Lafayette, IN 47905-1285                         "
"            (765) 494-3246                                        "
" For:       ACSL Short Course                                     "
" Date:      7/6/98                                                "
" Version:   1.0                                                   "
"                                                                   "
"-------------------------------------------------------------------"
"-------------------------------------------------------------------"
"                                                                   "
"       MACRO: DDCDC                                                "
" DESCRIPTION: Detailed model of two quadrant dc/dc converter       "
"                                                                   "
"                             CONCATENATION                         "
"                                                                   "
"    z          -     identifier                                   "
"                                                                   "
"                                                                   "
```

DDCDC1.MAC (Cont)

```
"                                INPUTS                                  "
"                                                                        "
"    d          -     duty cycle (upper switch on over total period)    "
"    vin        -     input voltage (V)                                 "
"    iout       -     current out of output terminal (A)                "
"                                                                        "
"                               OUTPUTS                                  "
"                                                                        "
"    vout       -     output voltage (V)                                "
"    iin        -     current into input terminal (A)                   "
"                                                                        "
"                              PARAMETERS                                "
"                                                                        "
"    l&z        -     inductance of leg inductor (H)                    "
"    rl&z       -     resistance of leg inductor (Ohms)                 "
"    c&z        -     output capacitance (F)                            "
"    f&z        -     switching frequency (Hz)                          "
"                                                                        "
"                               INTERNAL                                 "
"                                                                        "
"    iin0&z     -     initial value of iin (A)                          "
"    vout0&z    -     initial value of vin (V)                          "
"    vs         -     average voltage across lower switch (V)           "
"    is         -     average current out of upper switch (A)           "
"    p&iin      -     time derivative of iin (A/s)                      "
"    icap&z     -     current into the output capacitor (A)             "
```

DCDC.MAC (Cont)

```
"    p&vout     -     time derivative of vout (V/s)                    "
"    tri&z      -     modulator triangle wave                          "
"    ptri&z     -     time derivative of triangle wave (/s)            "
"    slope&z    -     absolute value of rate of change of triange      "
"                     wave (/s)                                        "
"                                                                      "
"----------------------------------------------------------------------"

MACRO DDCDC(z,d,vin,iout,vout,iin,par_l,par_rl,par_c,par_f)

   INITIAL

      CONSTANT par_l
      CONSTANT par_rl
      CONSTANT par_c
      CONSTANT par_f

      "compute the intitial conditions"
      iin0&z=0.0
      vout0&z=0.0

      "intitialize the triangle wave"
      tri&z=0.0
      slope&z=2*f&z
      ptri&z=slope&z

   END
```

DCDC.MAC (Cont)

```
   MACRO REDEFINE vs,is

   "FILL IN HERE"
   "compute the triangle wave and schedule changes of sign"

   "FILL IN HERE"
   "compute the switch voltage and switch current"
   "vs and is are function of d, tri&z, vout, and iin"

   "FILL IN HERE"
   "schedule crossings of the triangle wave and the duty"
   "cycle for more accurate representation of the switching"

   "compute the input current"
   p&iin=(vin-vs-rl&z*iin)/l&z
   iin=INTEG(p&iin,iin0&z)

   "compute the output capacitor current"
   icap&z=is-iout
   p&vout=icap&z/c&z
   vout=INTEG(pvout,vout0&z)

MACRO END
```

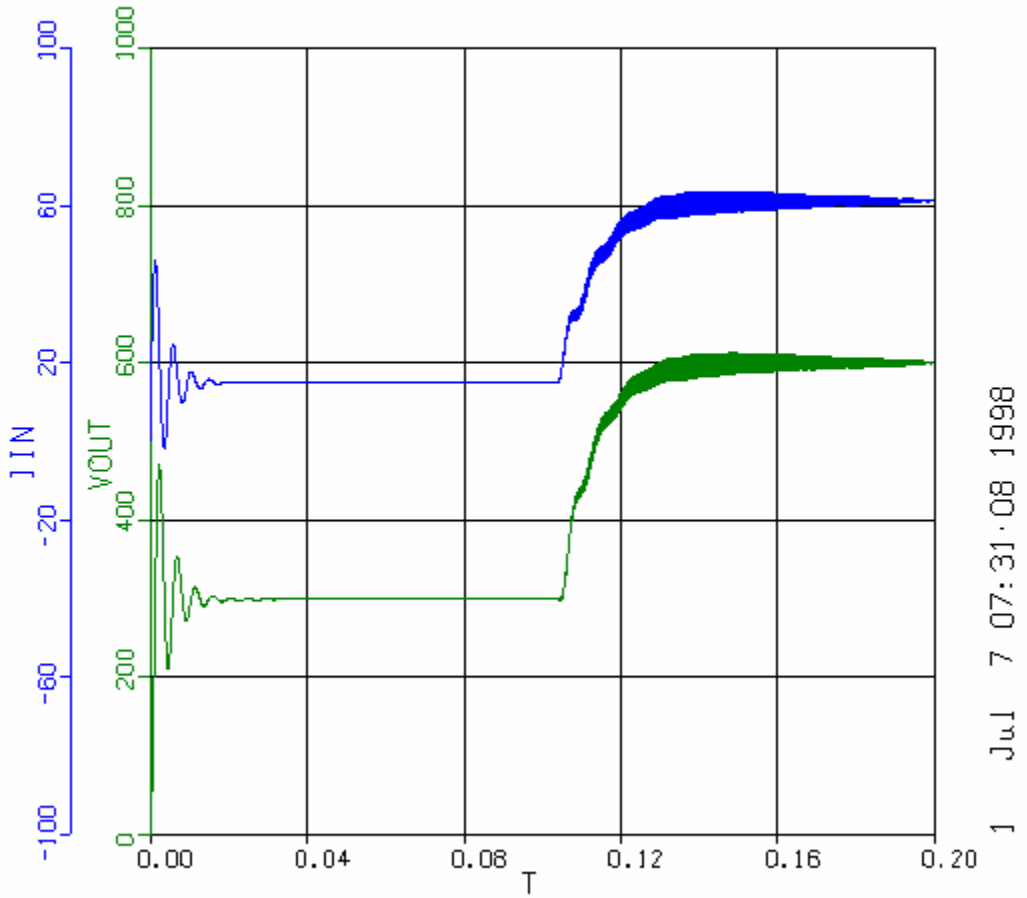
DCDC.MAC (Cont)

```
"-------------------------------------------------------------------"
"                                                                   "
"       MACRO: DDCDCD                                               "
" DESCRIPTION: Support macro for DDCDC. See DDCDC for documentation.  "
"                                                                   "
"-------------------------------------------------------------------"

MACRO DDCDCD(z)

   DISCRETE triangle&z

      "recompute the slope in case switching frequency has changed"
      slope&z=2*f&z

      "FILL IN"
      "This block is executed whenever triangle&z is called"
      "Use if statement to sort out up and down cases"


   END ! triangle&z

MACRO END
```

DCDC1.CMD

```
"-------------------------------------------------------------------"
"                                                                   "
" Author:    S.D. Sudhoff                                          "
"            School of Electrical Engineering                       "
"            1285 Electrical Engineering Building                   "
"            Purdue University                                      "
"            West Lafayette, IN 47905-1285                          "
"            (765) 494-3246                                         "
" For:       ACSL Short Course                                      "
" Date:      7/6/98                                                 "
" Version:   1.0                                                    "
"                                                                   "
"-------------------------------------------------------------------"

s hvdprn=.f.
prepare /all

proced study1

   action/var=0.1/val=600/loc=vref
   start
   action /clear
   plot iin,vout
   s vref=300.0

end
```

Results:


IIN
VOUT
T
100
60
20
-20
-60
-100
1000
800
600
400
200
0
0.00
0.04
0.08
0.12
0.16
0.20
1 Jul 7 07:31:08 1998