Fully Controlled 3-Phase Bridge Converter

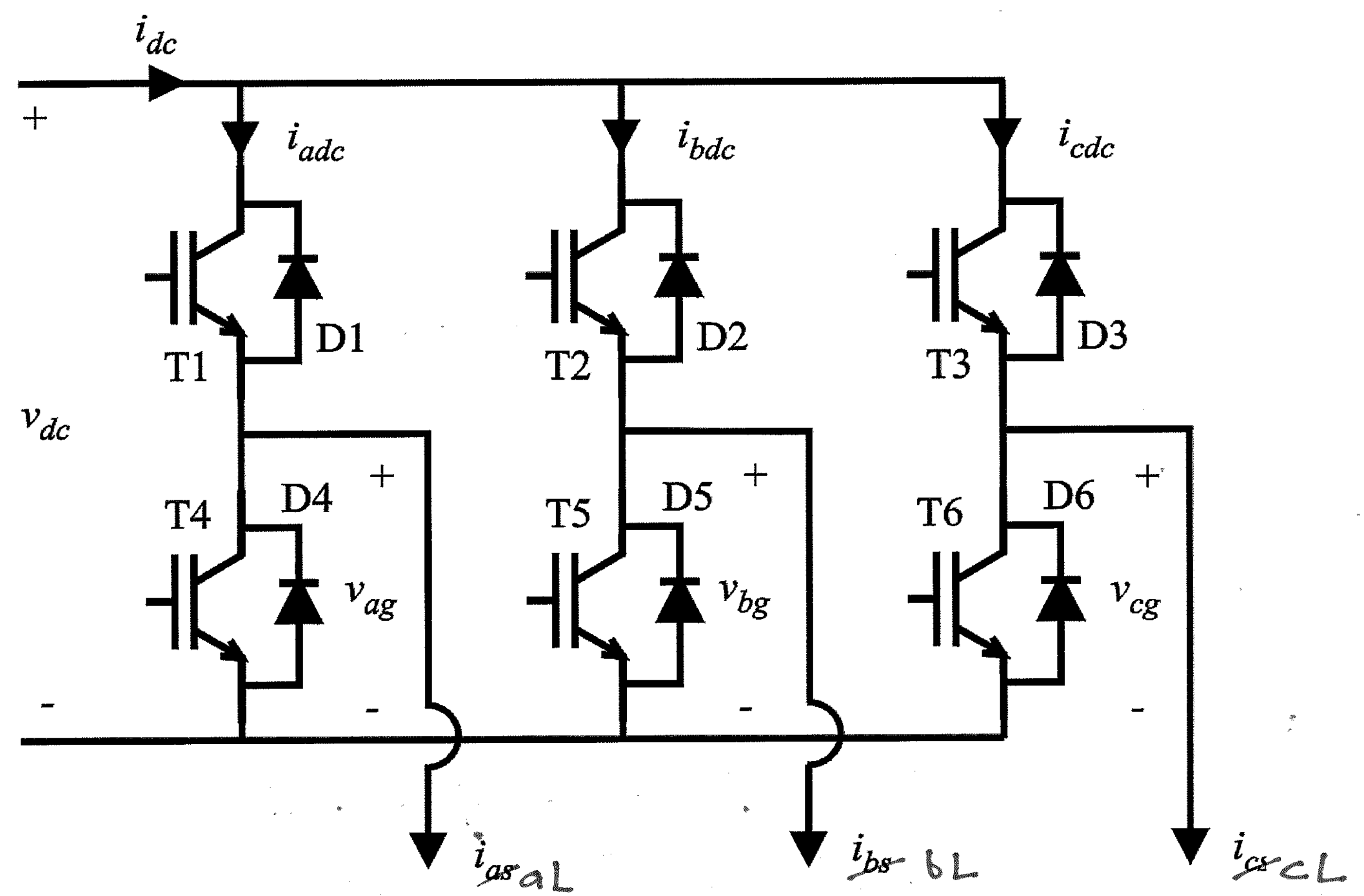


Figure 13.2-1 The three-phase bridge converter toplogy.

One Phase Leg

① if upper switch on, $i_{xs} > 0$

$V_{xg} = V_{dc} - V_{fsw}$

$I_{xdc} = I_{xs}$

② if upper switch on, $i_{xs} < 0$

$V_{xg} = V_{dc} + V_{fd}$

$I_{xdc} = I_{xs}$

③ if upper switch on, $i_{xs} = 0$

$V_{xs} = V_{dc}$

$I_{xdc} = I_{xs} = 0$

④ if lower on, $I_{xs} > 0$

$V_{xg} = -V_{fd}$

$I_{xdc} = 0$

⑤ if lower on, $I_{xs} < 0$

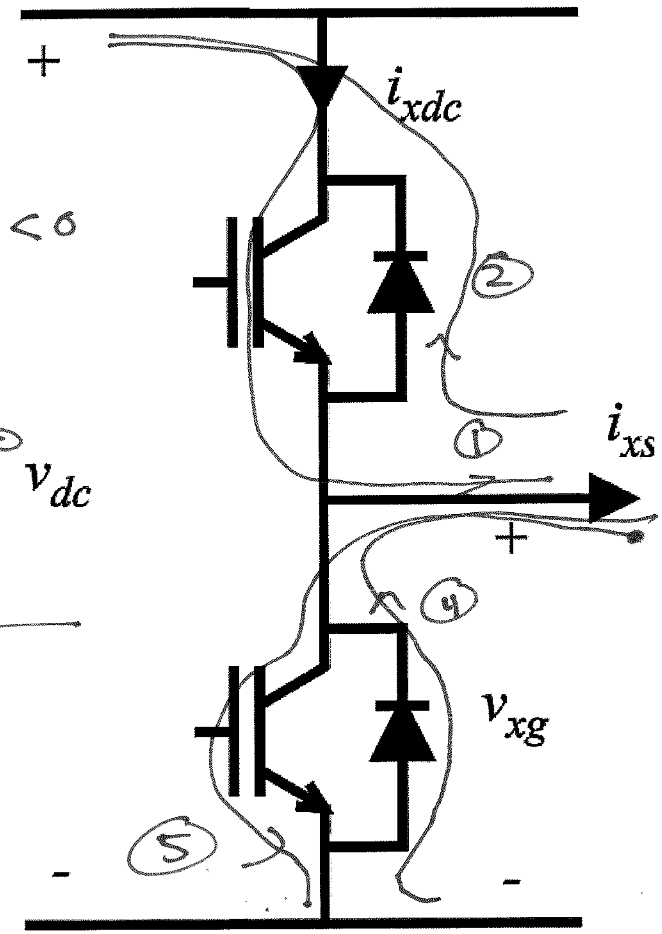
$V_{xg} = V_{fsw}$

$I_{xdc} = 0$

⑥ if lower on, $I_{xs} = 0$

$V_{xs} = 0$

$I_{xdc} = 0$



$X \in$ ['a', 'b', 'c']

⑦ if neither switch on,

$I_{xs} > 0$

$V_{xg} = -V_{fd}$

$I_{xdc} = 0$

⑧ if neither switch on

$I_{xs} < 0$

$V_{xs} = V_{dc} + V_{fd}$

$I_{xdc} = I_{xs}$

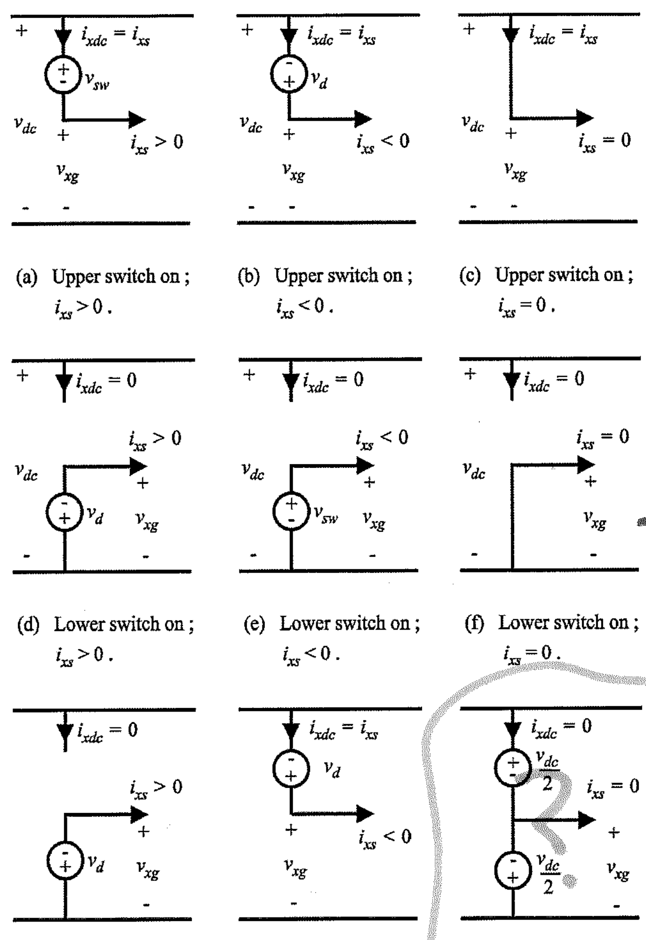
⑨ if neither switch is on and

$I_{xs} = 0$

$I_{xdc} = 0$

$V_{\cancel{dc}\,xs} = ?\ \frac{V_{dc}}{2}$

Phase Leg Equivalent Circuits



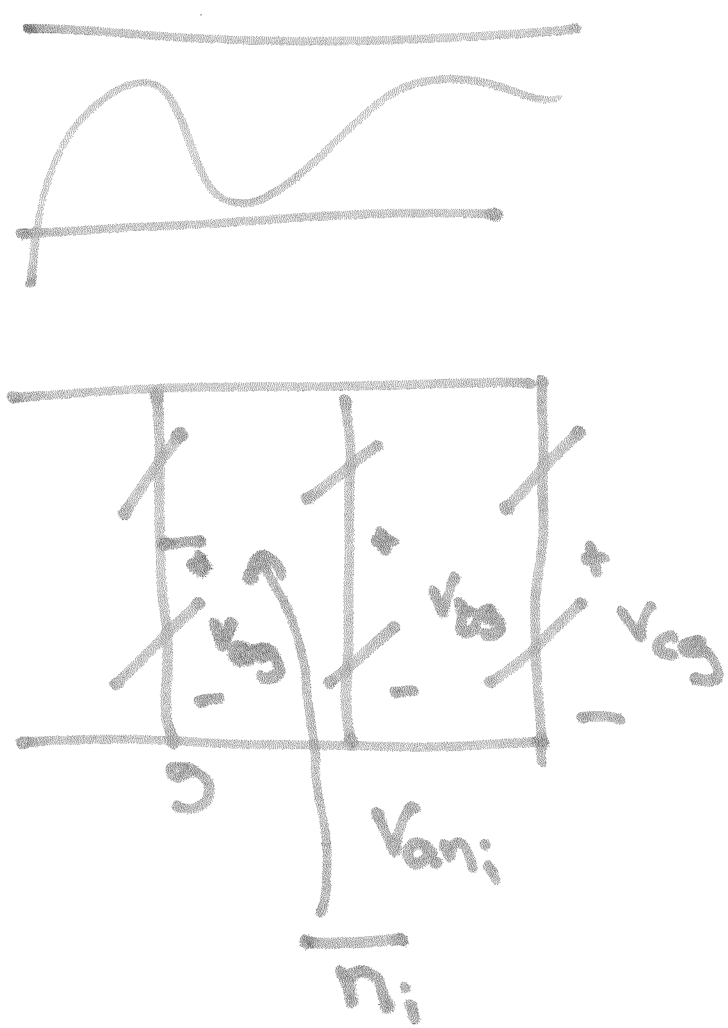
(a) Upper switch on ; $i_{xs} > 0$.
(b) Upper switch on ; $i_{xs} < 0$.
(c) Upper switch on ; $i_{xs} = 0$.
(d) Lower switch on ; $i_{xs} > 0$.
(e) Lower switch on ; $i_{xs} < 0$.
(f) Lower switch on ; $i_{xs} = 0$.
(g) Neither switch on ; $i_{xs} > 0$.
(h) Neither switch on ; $i_{xs} < 0$.
(i) Neither switch on ; $i_{xs} = 0$.

Phase Leg Voltages and Currents

Switch On	Current Direction	v_{xg}	i_{xdc}
Upper	Positive	$v_{dc} - v_{sw}$	i_{xs}
	Negative	$v_{dc} + v_d$	i_{xs}
	Zero	v_{dc}	i_{xs}
Lower	Positive	$-v_d$	0
	Negative	v_{sw}	0
	Zero	0	0
Neither	Positive	$-v_d$	0
	Negative	$v_{dc} + v_d$	i_{xs}
	Zero	$v_{dc}/2$	0

Calculation of QD Voltages

- We do not need line-to-neutral voltages to find QD voltages !



$$V_{qd0} = K_s \begin{bmatrix} V_{an_i} \\ V_{bn_i} \\ V_{cn_i} \end{bmatrix}$$

$$-V_{ag} + V_{an_i} + V_{n_ig} = 0$$

$$V_{an_i} = V_{ag} - V_{n_ig}$$

$$V_{abcn_i} = \begin{bmatrix} V_{ag} - V_{n_ig} \\ V_{bg} - V_{n_ig} \\ V_{cg} - V_{n_ig} \end{bmatrix}$$

$$V_{qd_i} = \frac{2}{3} \begin{bmatrix} c & c^- & c^+ \\ s & s^- & s^+ \end{bmatrix} V_{abcn_i}$$

$$V_{qd_i} = K_s \big|_{UTR} V_{abcg}$$

upper two rows

Limits on Current Tracking

suppose

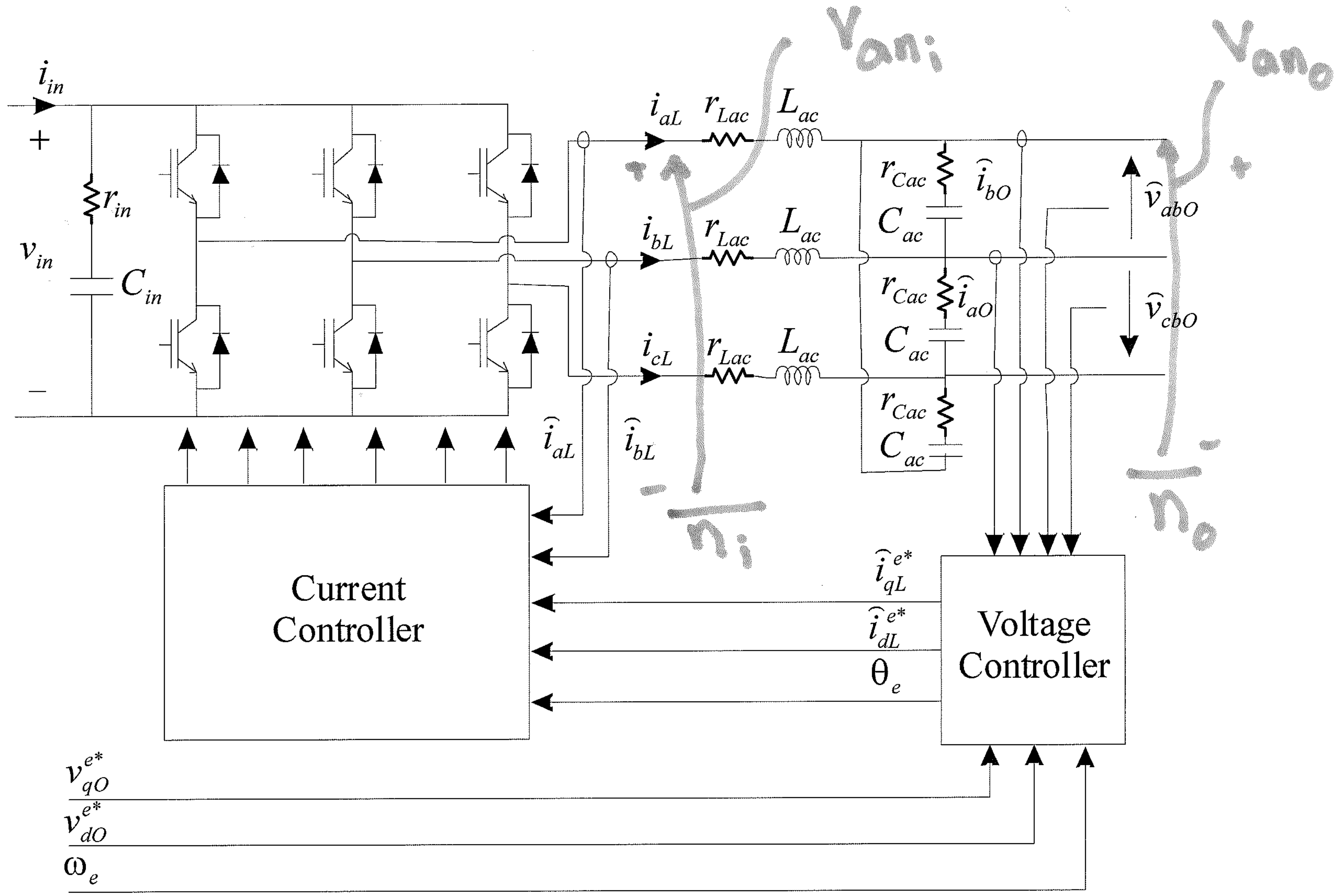
$$V_{ai} = \sqrt{2}\, V_s \cos(\omega_e t)$$

$$\Rightarrow V_{abi} = \sqrt{6}\, V_s \cos(\omega_e t + ?)$$

$$\therefore \sqrt{6}\, V_s < V_{dc}$$

$$\boxed{V_s < \frac{V_{dc}}{\sqrt{6}}}$$

QD Representation of LC Filter



QD Representation of LC Filter

$$-v_{an_i} + r_{Lac}\, i_{aL} + L_{ac}\, p\, i_{aL} + v_{an_o} + v_{n_on_i} = 0$$

$$-v_{abcn_i} + r_{Lac}\, i_{abcL} + L_{ac}\, p\, i_{abcL} + v_{abcn_o} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} v_{n_on_i}$$

$$-v_{qdi} + r_{Lac}\, i_{qdi} + L_{ac}\left[p\, i_{qdi} + \omega \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} i_{qdi} \right] = 0$$

$$+ v_{qdo} = 0$$

$$p\, i_{qdi} = \frac{1}{L_{ac}}\left[v_{qdi} - v_{qdo} - r_{Lac}\, i_{qdi} \right] - \omega \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} i_{qdi}$$

QD Representation of LC Filter

$$Z_1 = \frac{Z_a Z_b}{Z_a + Z_b + Z_c}$$

$$Z_2 = \frac{Z_a Z_c}{Z_a + Z_b + Z_c}$$

$$Z_3 = \frac{Z_b Z_c}{Z_a + Z_b + Z_c}$$

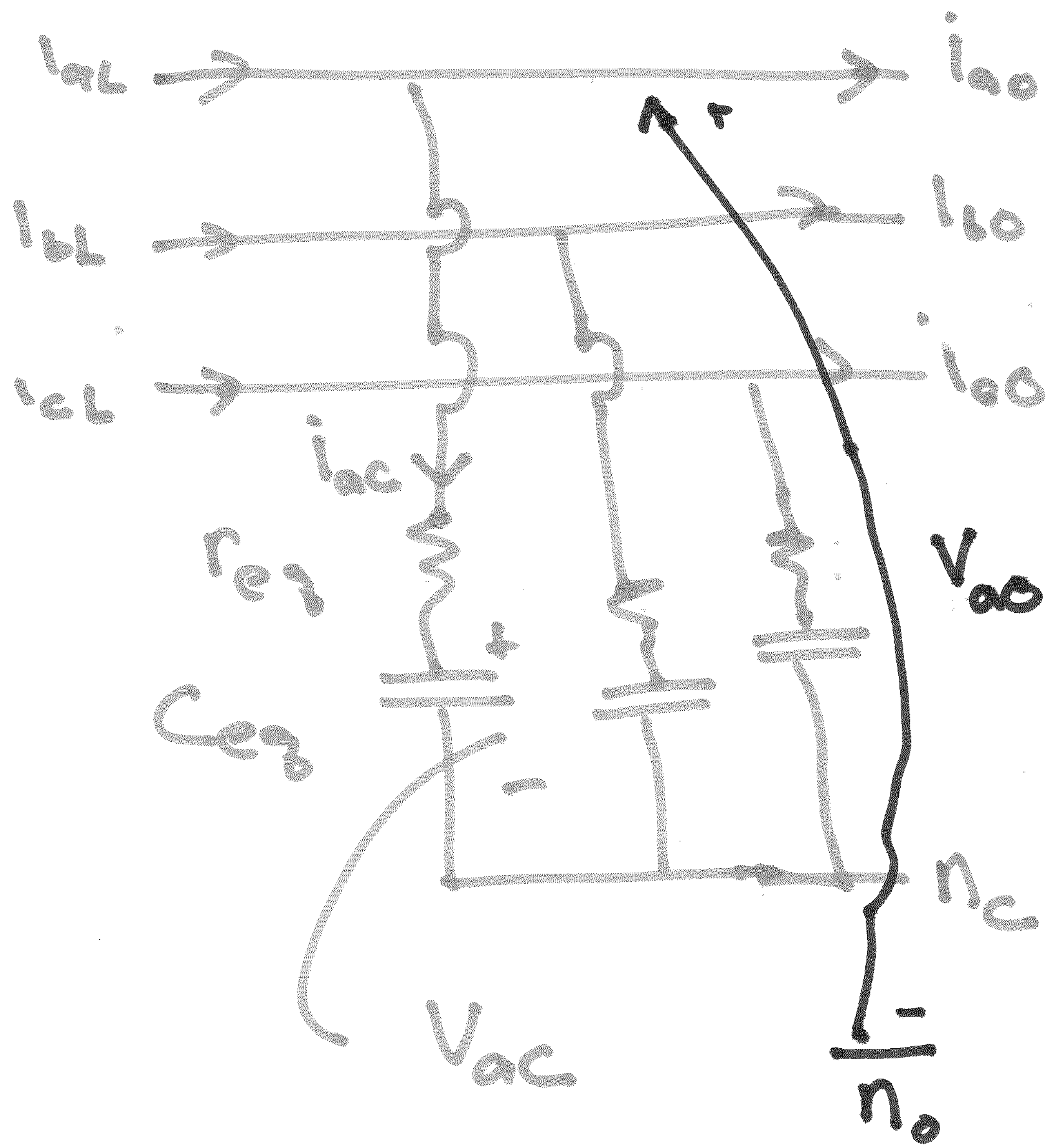
QD Representation of LC Filter

$$Z_a = Z_b = Z_c = r_{cac} + \frac{1}{C_{cac} s}$$

$$Z_1 = \frac{Z_a Z_a}{Z_a + Z_a + Z_a} = \frac{1}{3} Z_a$$

$$= \underbrace{\frac{1}{3} r_{cac}}_{r_{eq}} + \frac{1}{\underbrace{3 C_{cac}}_{C_{eq}} s} = r_{eq} + \frac{1}{C_{eq} s}$$

QD Representation of LC Filter



$$i_{abcL} = i_{abcC} + \dot{i}_{abco}$$

$$\Downarrow$$

$$\dot{i}_{qdL} = \dot{i}_{qdC} + \dot{i}_{qdo}$$

QD Representation of LC Filter

$$-V_{ao} + r_{eq} i_{ac} + V_{ac} + V_{n_c n_o} = 0$$

$$-V_{abco} + r_{eq} \dot{i}_{abcc} + V_{abcc} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} V_{n_c n_o} = 0$$

$$-V_{qdo} + r_{eq} \bar{i}_{qdc} + V_{qdc} = 0$$

QD Representation of LC Filter

$$p\,v_{abcc} = \frac{1}{C_{eq}}\, i_{abcc}$$

$$p\,v_{qdc} + \omega \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} v_{qdc} = \frac{1}{C_{eq}}\, i_{qdc}$$

$$\boxed{p\,v_{qdc} = \frac{1}{C_{eq}}\, i_{qdc} - \omega \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} v_{qdc}}$$

QD Representation of LC Filter

QD Representation of LC Filter

QD Representation of LC Filter

i_{qdi} = inverter current = inductor current = i_{qdL}

$$p\mathbf{i}_{qdi} = \frac{1}{L_{ac}}\left(\mathbf{v}_{qdi} - \mathbf{v}_{qd0} - r_{Lac}\mathbf{i}_{qdi}\right) - \omega\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\mathbf{i}_{qdi}$$

$$r_{eq} = \frac{1}{3}r_{Cac}$$

$$C_{eq} = 3C_{ac}$$

$$p\mathbf{v}_{qdC} = \frac{1}{C_{eq}}\mathbf{i}_{qdC} - \omega\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\mathbf{v}_{qdC}$$

$$\mathbf{i}_{qdC} = \frac{1}{r_{eq}}\left(\mathbf{v}_{qd0} - \mathbf{v}_{qdC}\right)$$

$$\mathbf{i}_{qdi} = \mathbf{i}_{qdC} + \mathbf{i}_{qdO}$$

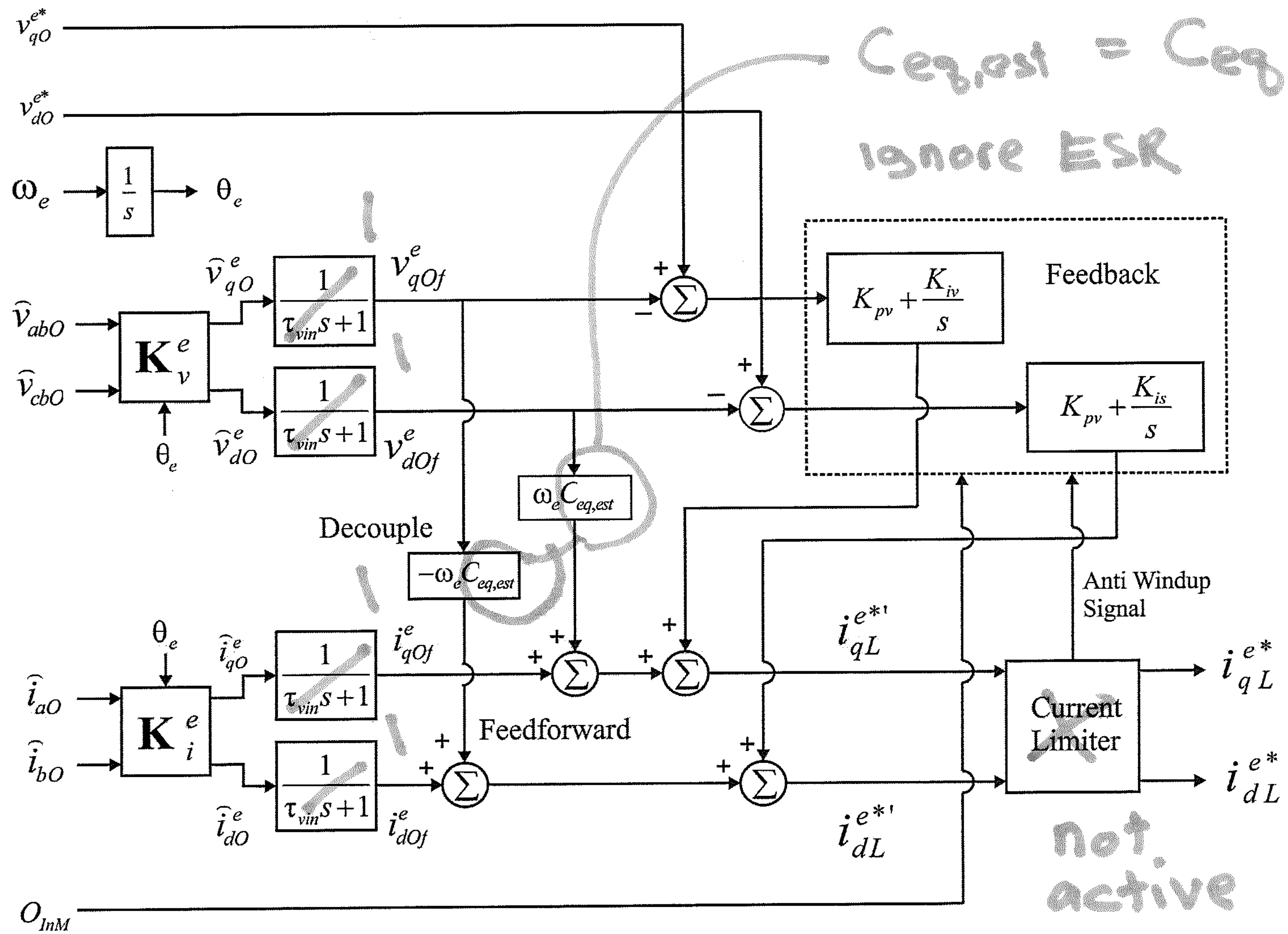
$$\mathbf{v}_{qd0} = r_{eq}\mathbf{i}_{qdC} + \mathbf{v}_{qdC}$$

Analysis of Voltage Control

assume we have current tracking

$C_{eq,est} = C_{eq}$

ignore ESR



Analysis of Voltage Control

$$i_{qL}^{e} = \left(K_{pv} + \frac{K_{iv}}{s}\right)\left(V_{qo}^{*e} - V_{qo}^{e}\right) + \omega_e C_{eq} V_{do}^{e} + I_{qo}^{e}$$

$$i_{dL}^{e} = \left(K_{pv} + \frac{K_{iv}}{s}\right)\left(V_{do}^{e*} - V_{do}^{e}\right) - \omega_e C_{eq} V_{qo}^{e} + I_{do}^{e}$$

$$s V_{qo}^{e} = \frac{1}{C_{eq}}\left(I_{qL}^{e} - I_{qo}^{e}\right) - \omega_e V_{do}^{e}$$

$$s V_{qo}^{e} C_{eq} = \left(K_{pv} + \frac{K_{iv}}{s}\right)\left(V_{qo}^{e*} - V_{qo}^{e}\right)$$

$$V_{qo}^{e} C_{eq} s^2 = \left(K_{pv} s + K_{iv}\right)\left(V_{qo}^{e*} - V_{qo}^{e}\right)$$

Analysis of Voltage Control

$$\left[C_{eq}s^2 + K_{pv}s + K_{iv}\right] v_{qo}^{e} = \left(K_{pv}s + K_{iv}\right) v_{qo}^{e*}$$

$$\frac{v_{qO}^{e}}{v_{qO}^{e*}} = \frac{K_p s + K_i}{Cs^2 + K_p s + K_i}$$

QD Current Limit

Start with $i_{qL}^{e'*}$ and $i_{dL}^{e'*}$

$$i_{pk} = \sqrt{\left(i_{qL}^{e'*}\right)^2 + \left(i_{dL}^{e'*}\right)^2}$$

if $i_{pk} < i_{pk,lim}$

$i_{qL}^{e*} = i_{qL}^{e'*}$

$i_{dL}^{e*} = i_{dL}^{e'*}$

$a = 0$ ← Flag to anti-windup control

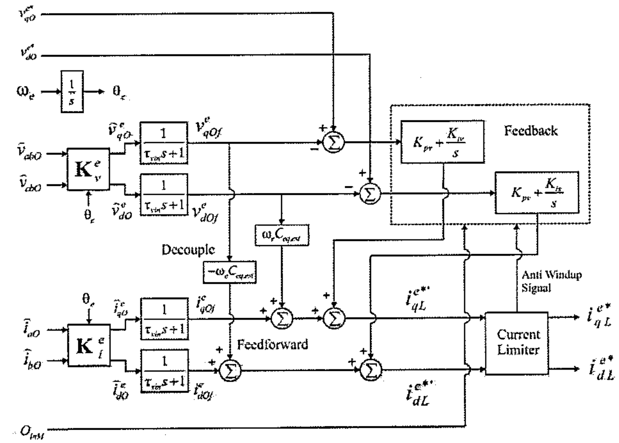
else

$i_{qL}^{e*} = i_{qL}^{e'*} \dfrac{i_{pk,lim}}{i_{pk}}$

$i_{dL}^{e*} = i_{dL}^{e'*} \dfrac{i_{pk,lim}}{i_{pk}}$

$a = 1$

end



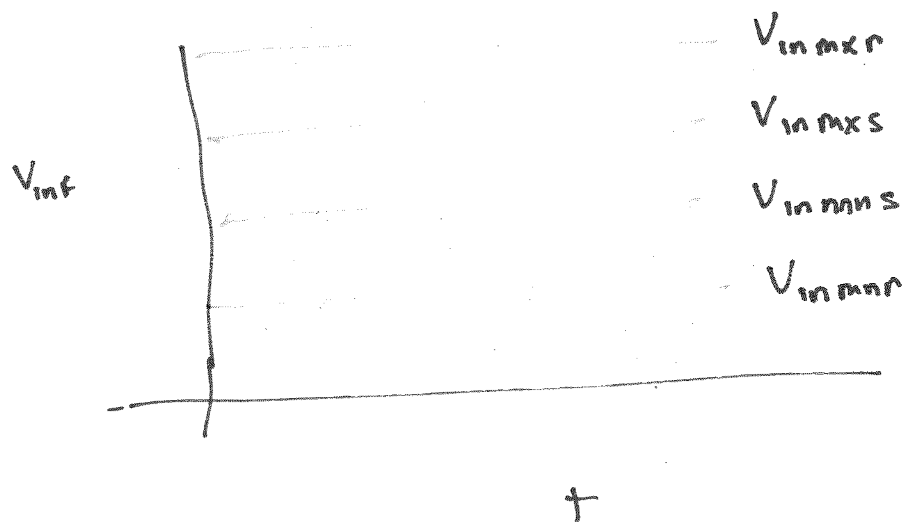
Operating Status

~~Voltage Control – Off State or Limits~~

O^* = desired operating status

O = actual operating status

$$V_{in} \longrightarrow \boxed{\frac{1}{\tau_{vin} s + 1}} \longrightarrow V_{inf}$$



Operating Status

if $\overline{O^*}$

$\quad O = O^*$

else

$\quad$ if O

$\qquad O = (V_{inf} \geq V_{inmnr}) \cdot (V_{inf} \leq V_{inmxr})$

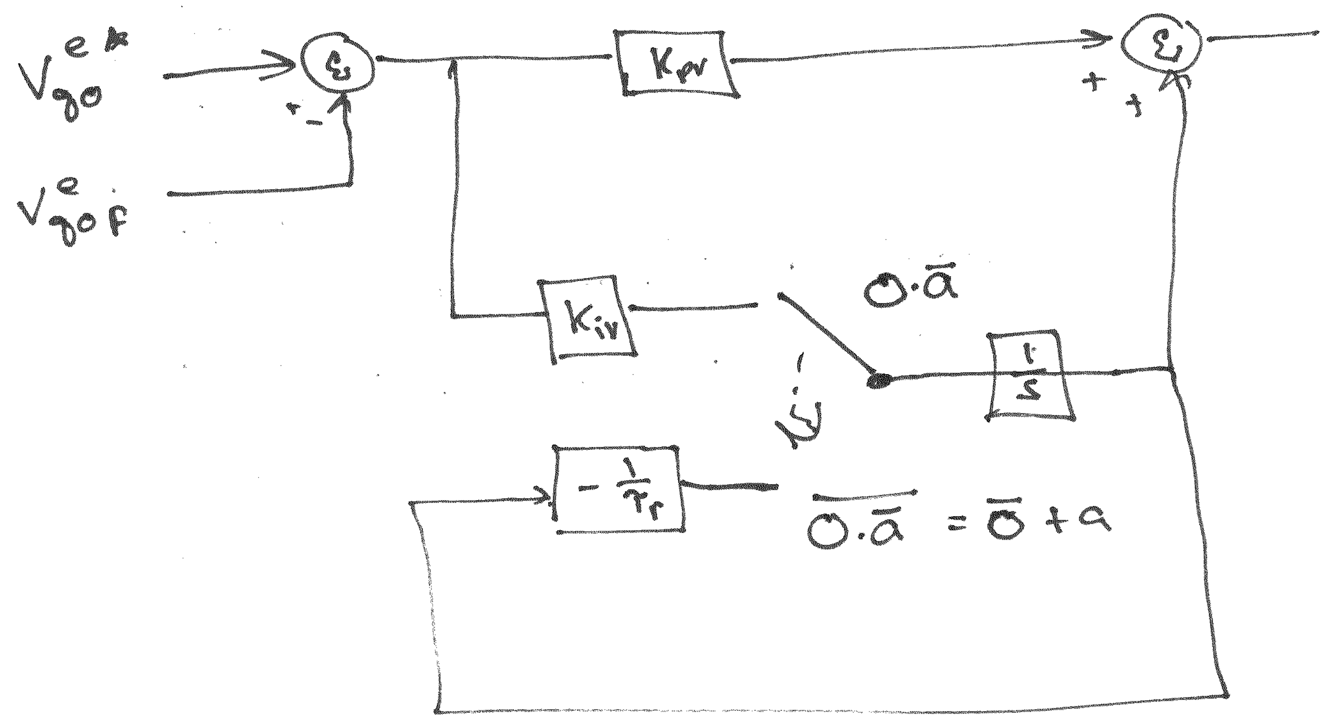
$\quad$ else

$\qquad O = (V_{inf} \geq V_{inmns}) \cdot (V_{inf} \leq V_{inmxs})$

$\quad$ end

end

~~Operating Status~~ Anti-Windup



$\overline{O \cdot \bar{a}} = \bar{O} + a$

Sample Study

- Commanded voltage: 230 V l-l rms
- Commanded frequency: 60 Hz
- Peak current limit: 30 A
- Minimum voltage to run: 350
- Maximum voltage to run: 450
- Minimum voltage to start: 400
- Maximum voltage to start: 430
- Estimated l-n capacitance: 160 uF
- Sampling frequency: 450 kHz
- Hysteresis level: 1 A

$$V_{qo}^{e*} = \frac{230\sqrt{2}}{\sqrt{3}}$$

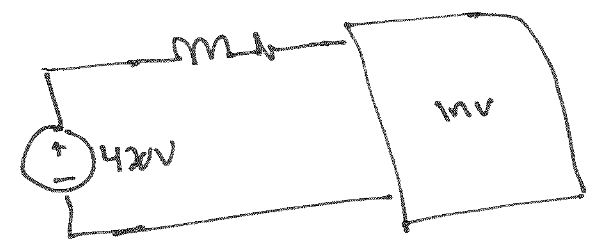
$$V_{do}^{e*} = 0$$

Sample Study

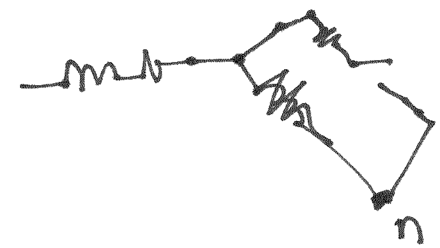
- Forward switch drop: 1 V
- Forward switch resistance: 100 mΩ
- Forward diode drop 2 V
- Forward diode resistance 50 mΩ
- Input capacitor capacitance 590 uF
- Input capacitor resistance 127 uΩ
- Equivalent l-n output capacitance: 150 uF
- Equivalent l-n output capacitor resistance: 2.67 mΩ
- AC inductor inductance: 550 uH
- AC inductor resistance: 38 m~~W~~Ω

Sample Study

- DC Source
  - 420 V with 50 uH and 50 mΩ



- Loads
  - Cable: 100 mΩ and 0.1 mH impedance
  - Load 1: 105.8 Ω line-to-neutral
  - Load 2: 10.58 Ω line-to-neutral

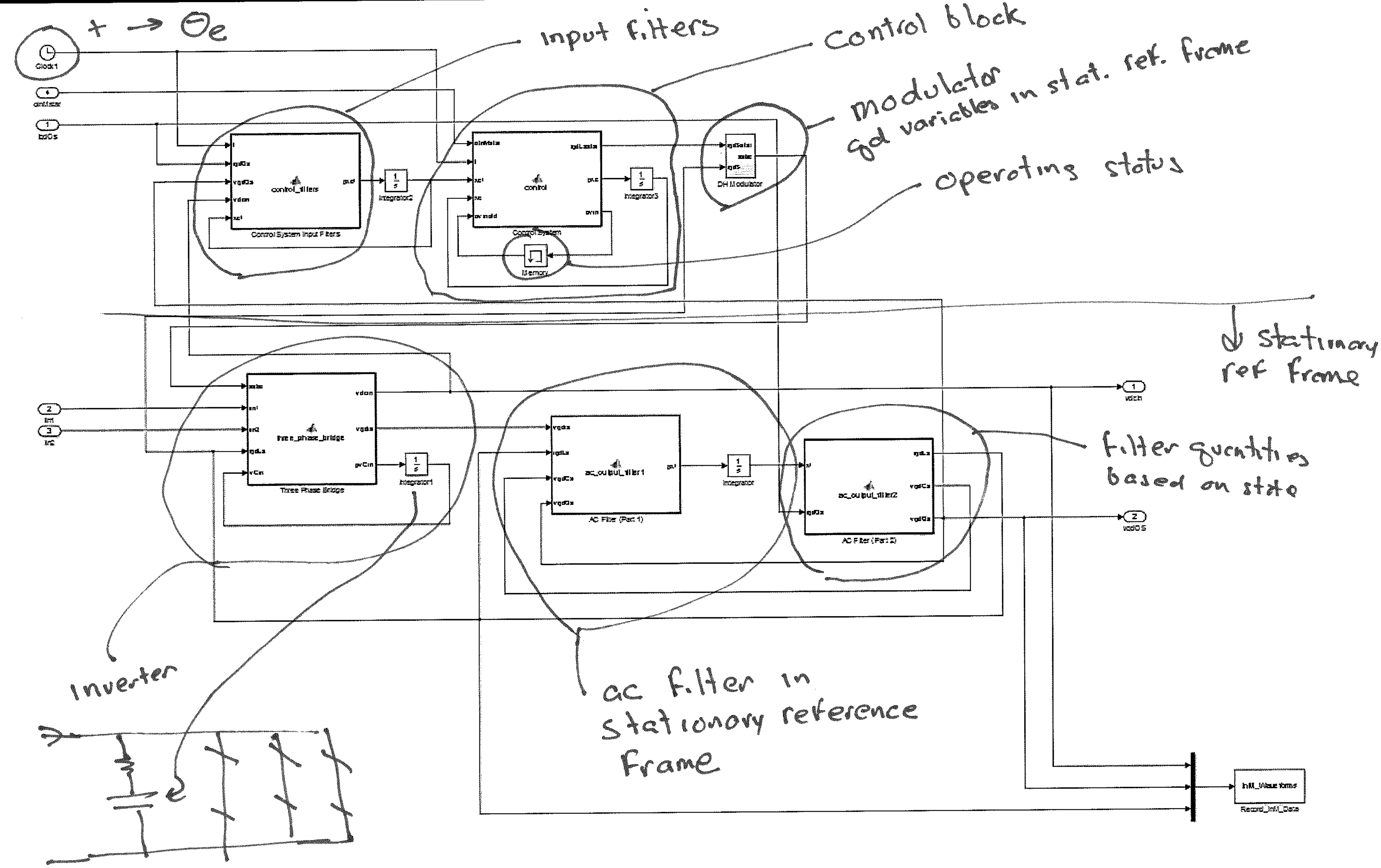


Scenario

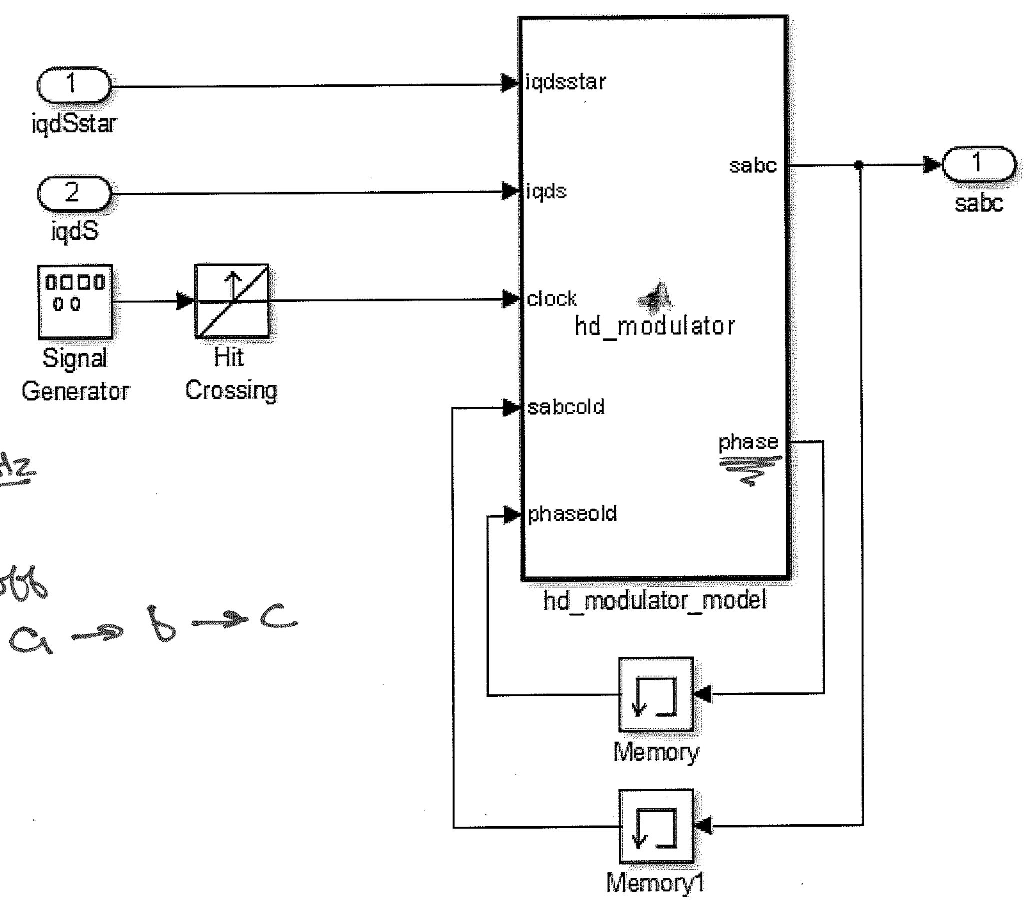
- Power connected at $t=0$
  - Load 1 is initial present
  - Initially device is commanded off
  - Turned on at $t=0.02$ s
- Load 2 replaces load 1 at $t=0.05$ s

Simulation Overview

$\theta_e = \omega_e t$



Simulation Overview



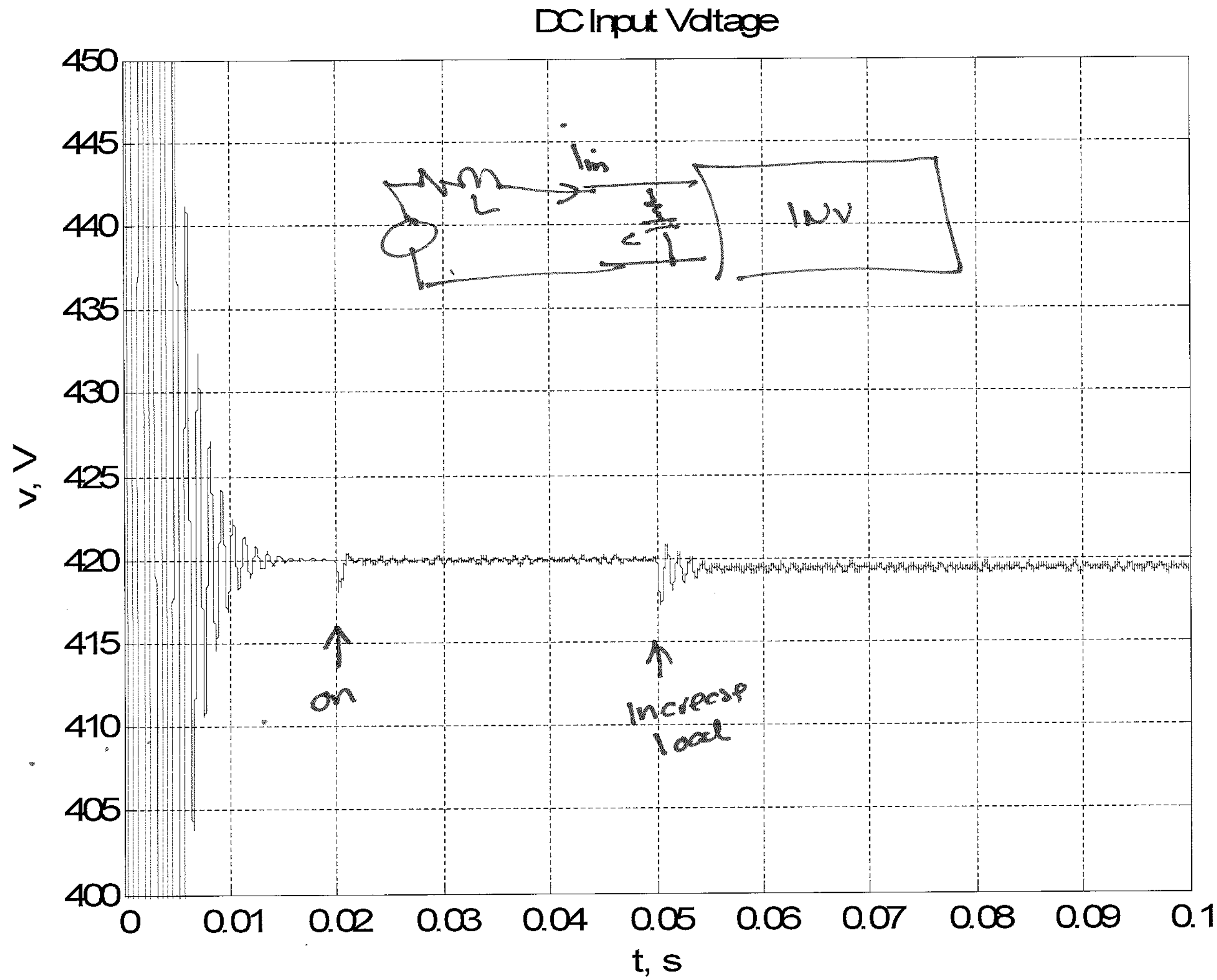
450 kHz

maximum switching Frequency is $\frac{450\text{ kHz}}{6}$

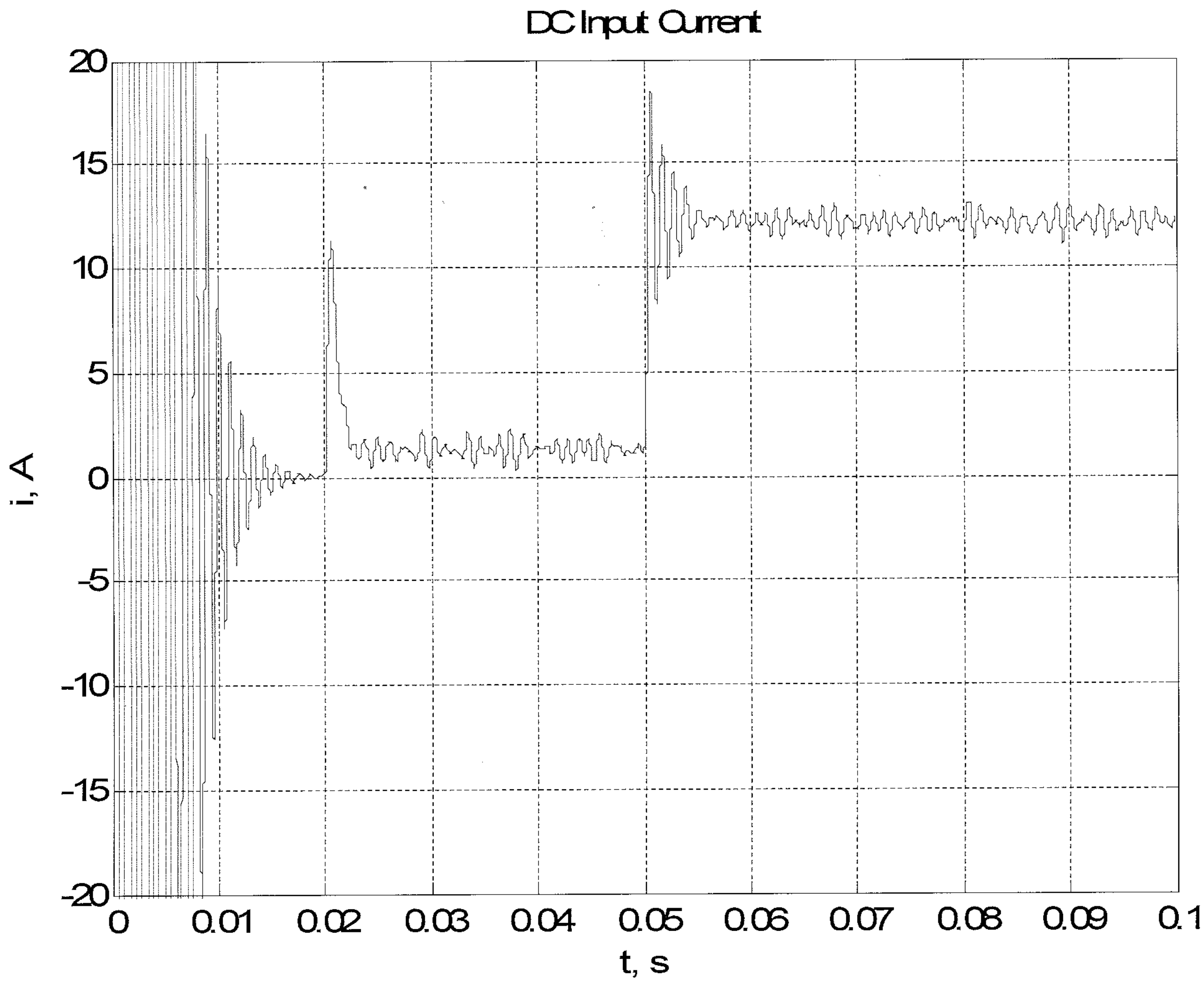
on   off

$a \rightarrow b \rightarrow c \rightarrow a \rightarrow b \rightarrow c$

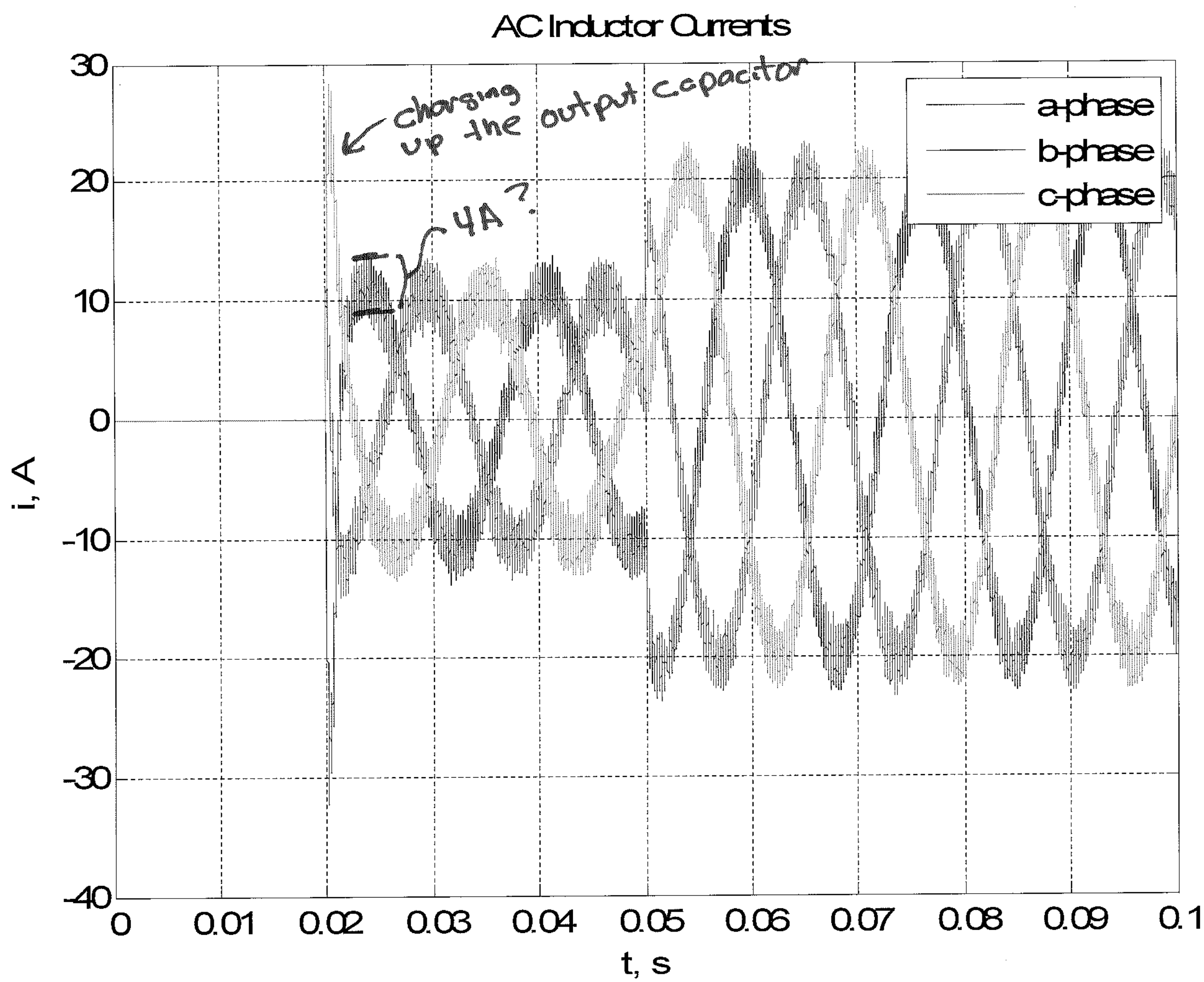
Input Voltage



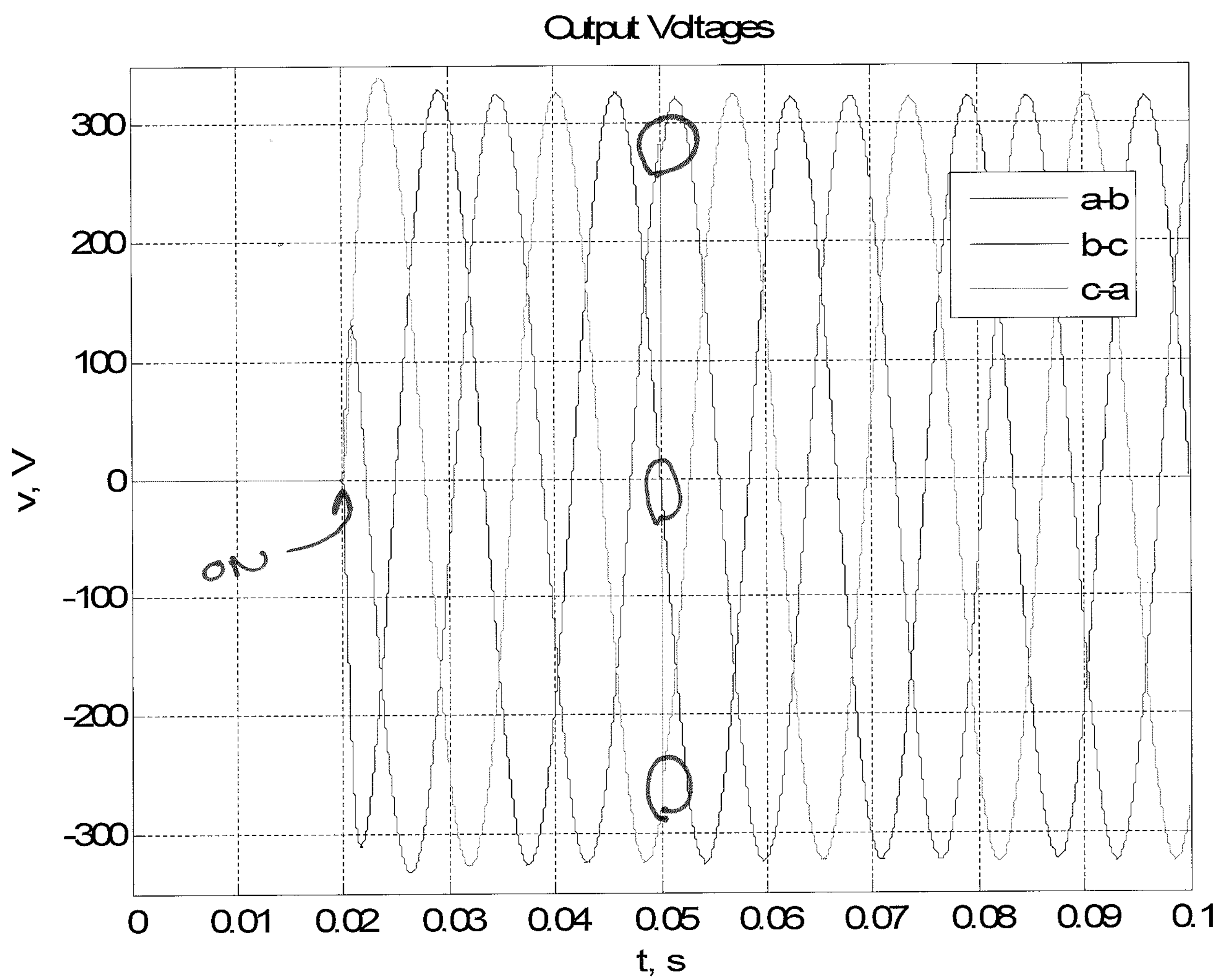
Input Current



Inductor Current



Output Voltage



Thoughts on Average Value Modeling

- Use synchronous reference frame
- Representation of Modulator
  - Approach 1: Assume that $\underline{\underline{i_{qdL}^{e} = i_{qdL}^{e*}}}$
  - Approach 2: Represent inverter as equivalent voltage source

AVM of Inverter Module

- Features
  - Include conduction losses
  - Ignore switching losses
  - Based on sine-triangle with 3rd harmonic modulation