METHOD TO DETECT AND PROTECT INDUSTRIAL POWER CONVERTER SYSTEMS FROM LINE-TO-GROUND FAULTS

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ABSTRACT


An Industrial-Power-Converter-System (IPCS) is a system made up of several power converters, such as Adjustable Speed Drive (ASDs), filters, and any kind of reactive power-compensation components. Today, an IPS requires the ability to accurately detect and isolate electric faults to avoid further compromise of the integrity of the whole system. One particular type of electric fault is the cable line-to-ground fault. Due to the complexity and asymmetry of IPS, reliably detecting cable line-to-ground faults is a formidable task. Therefore, it is necessary to identify current/voltage signature uniquely linked to the occurrence of the fault; set a threshold; and construct a method that allows for identifying the faulted ASD in the IPS. The method presented in this dissertation tracks low-frequency current sourced by the Common Mode Voltage (CMV) of the ASD. It is reliable, modular (as defined in Chapter 7); and it can be extended to complex IPS.
1. INTRODUCTION

1.1 Background

Consistent and reliable operation of Industrial Power Converter Systems (IPCS) is important to ensure personnel safety and to lower production and maintenance costs [1], [2]. Hence, detection of faults and protection of IPCS has received considerable impetus from industry, leading to a flurry of research activity in industry and in academia. The focus is on early detection of faults and abnormal operating conditions, in order to provide sufficient time for controlled shutdown of the process and scheduled tasks, thereby reducing outage time and damage of the IPCS [3].

High Resistance Ground (HRG) systems are the recommended practice for industrial power systems in general and for IPCS, in particular, to detect line-to-ground faults [4]. They are recommended over ungrounded systems and solidly grounded systems, shown in Fig. 1.1.

An advantage of the ungrounded system (shown in Fig. 1.1) is that it does not require immediate interruption of power flow when a line-to-ground fault occurs. A disadvantage is that primary line-to-ground voltage transients are passed to the secondary without attenuation. According to [5], impulse testing of a transformer with ungrounded neutral shows a 2000 Vpeak 1.2 μs/50 μs impulse test applied line-to-ground on the transformer primary is virtually unattenuated, line-to-ground, on the secondary side. Another disadvantage is that X₀ neutral point is capacitively coupled to the ground, allowing X₀ voltage to float toward the line voltage during transients, and overstress the line-to-neutral insulation system. The principal problem with an ungrounded neutral system is that an arcing ground fault can cause escalation of the system line-to-ground voltages to several times normal line-to-ground voltage. This occurs as the arcing fault alternatively extinguishes and reestablishes itself, successively trapping a higher charge on the system shunt capacitance each time. This causes displacement of the system neutral, which is only connected to ground through the shunt capacitance, to a voltage that is several times the normal line-to-ground voltage. Voltages-to-ground which are sufficient to cause insulation failures, especially in motors, are likely [5].

An advantage of a solidly grounded Y-system, like the one presented in Fig. 1.1, is that it can provide a 5:1 – 10:1 attenuation of transformer primary line-to-ground voltage transients. According to [5], impulse testing of a transformer with a grounded neutral showed a 2000 Vpeak 1.2 μs/50 μs impulse test applied line-to-ground voltage on the transformer primary,
had only a 200 Vpeak line-to-ground voltage on the secondary side. Also, an X₀ neutral, solidly connected to earth ground potential, reduces the possibility of overstressing line to neutral insulation [6]. A disadvantage of solidly grounded Y-systems is that a line-to-ground fault will interrupt power to the process line immediately. Moreover, with a solidly grounded neutral system, the problem with line-to-ground voltage escalation, due to an arcing ground fault, is eliminated since the neutral is held to ground potential. The higher ground fault current also has the possibility to inflict more damage due to the higher energy to be dissipated. Other circuits may also be disrupted due to the severe voltage drop caused by the higher fault current [5].

![Diagram of neutral grounding systems](image)

**Fig. 1.1. Typical neutral grounding systems**

The HRG system of Fig. 1.1 is designed to add sufficient neutral-to-ground resistance to limit the line-to-ground fault current to a value greater than or equal to the system capacitive charging current [7], which is normally kept in the range of 1-5 A for low-voltage networks (≤ 600 Vac) [8]. For low-voltage networks, HRG systems provide all the benefits of an ungrounded system and almost none of their disadvantages [5], [9]. HRG allows the process to continue on the occurrence of the first line-to-ground fault, permitting an orderly shutdown, if necessary. Moreover, it prevents overvoltage due to arcing grounds, eliminating the risk of flash hazards [10], [11], [12], [13].

The theory behind HRG systems presented briefly in this section has been applied in industry for the last few decades without too much change. The incorporation of power converters, however, poses new challenges that require to be accounted for and surprisingly have been neglected. This is attempted in Chapter 5.

### 1.2 Line-to-ground faults on the inverter side of a 1-ASD IPCS

Line-to-ground faults on the inverter-side of 1 ASD (referred from now on as simply line-to-ground faults) are among the most common type of faults in IPCS, yet among the most difficult to accurately detect [14]. There are a handful of techniques to detect such faults that are based on the measurement of certain current signature [15], [16], [17]. Similarly, techniques that involve the measurement of line-to-ground voltages are also utilized.
Thorough literature search, however, has failed to identify advantages and disadvantages of current-based methods and voltage-based methods. This is addressed in Chapter 8.

Some of the difficulties associated with the implementation of line-to-ground fault detection techniques are:
- Setting a threshold, addressed in Chapter 6
- Magnetic coupling-related issues, addressed in Chapter 7

Setting a threshold to which compare a voltage/current level to determine the occurrence of a line-to-ground fault is challenging. PWM Voltage Source Inverters and Converters (VSI, VSC) require switching semiconductors with fast rise and fast fall edges that effectively excite parasitic capacitances that become paths for the circulation of current. Moreover, reconfiguration of IPCSs (i.e., addition or random turn-on, turn-off of converters), is very common. Such issues, combined with insufficient filtering capability of line-to-ground fault sensing mechanisms, make it difficult to set a threshold for the voltage/current signature utilized to detect the occurrence of a line-to-ground fault. A solution that requires complex filtering capability is proposed in [5].

Asymmetric cabling arrangements in conjunction with ground grids contaminated by converter spectra may yield installations where traditional protection techniques can be inadequate. Discriminating between wanted and unwanted signals requires either detuning protection functions thus resulting in under-protected systems or highly sensitive systems susceptible to nuisance tripping. In the literature, it has not been found that the consequences of asymmetric magnetic coupling between line conductors and ground loops have been explored. The additional current coupled to ground conductors can lead to increased amperage loading of the conductors in addition to ground voltage gradients. Furthermore, a mechanism exists by which asymmetric magnetic coupling can mask line-to-ground fault detection.

1.3 Problem statement

In this dissertation, a method to detect line-to-ground faults is developed. The goals for this method are:
- To be reliable in HRG systems
- To be reliable in multi-drive HRG system applications (complex IPCS)
- To utilize an appropriate threshold
- To specify voltage/current signature to comply with reliability
- To adequately track voltage/current signature (tracking filter implementation)
- To detect a fault on the inverter side of 1 ASD
- To identify the faulted ASD in an IPCS
• To be impervious to asymmetric magnetic coupling (cable asymmetries and multiple ground loops)
• To be impervious to system reconfiguration
• To be impervious to voltage unbalance

1.4 Organization of the Proposal
The rest of this dissertation is organized as follows:

In Chapter 2, two topologies (diode-rectifier front-end and active front-end) and 3 systems comprised of 1 ASD each are presented. These test-beds are implemented in hardware and simulated to prove the validity of analytical results. Then, a more complex IPCS to extend the developed method to detect line-to-ground faults on the inverter side of one ASD is introduced. Finally, a top-down strategy to clarify the methodology followed to develop the line-to-ground fault detection method is unveiled.

In Chapter 3, a review of reported line-to-ground fault detection techniques is introduced.

In Chapter 4, simplified models of the IPCS presented in Chapter 2 that allow for including components of interest are introduced. These models are later on utilized through Chapters 5-8 to aid in the understanding of the problem and the development of the line-to-ground fault detection method.

In Chapter 5, the difficult task of setting a voltage/current threshold is explored.

In Chapter 6, the problem of asymmetric magnetic coupling is studied and voltage/current signature uniquely linked to the occurrence of a line-to-ground fault is identified and discussed.

In Chapter 7, advantages and disadvantages of voltage measurement-based methods and current measurement-based methods, are explored. The benefits of using current measurement-based methods over voltage measurement-based methods are presented.

In Chapter 8, a method to detect a line-to-ground fault and a realization of a filter to obtain instantaneous magnitude and phase of specific harmonic content are introduced. The method is comprised of an off-line line-to-ground fault detection stage and an on-line line-to-ground fault detection stage. It is based on current measurement as per the recommendation made in Chapter 7. Furthermore, the threshold and HRG value established in Chapter 5 are utilized along with the signature of the current established in Chapter 6 to be the more reliable indication of the occurrence of a line-to-ground fault.

In Chapter 9, results of hardware implementation are presented.

In Chapter 10, the steps to complete this dissertation are discussed.
1.5 Contributions

The contributions of the preliminary version of this dissertation are as follows:

1) Study and proposal of a model for a 1-ASD IPCS that provides powerful insight in the development of a reliable method to detect line-to-ground faults (Chapter 4)

2) Extension of the state-of-the-art for HRG systems design with sine-wave sources to HRG systems with PWM excitation (Chapter 5)

3) Determination of preferred signature to find a threshold for

4) A method to calculate a threshold for the sum of the 3-line currents at the output of the inverter that is extensible to calculate a threshold for each line current at the output of the inverter (Chapter 5)

5) The demonstration that differentially sourced voltage/current is not a reliable indication of the occurrence of a line-to-ground fault due to asymmetric magnetic coupling (Chapter 6).

6) The demonstration that the current sourced by the CMV of the ASD is a more reliable indication of the presence of a line-to-ground fault (Chapter 6).

7) The introduction of criteria to adequately select current signature instead of voltage signature to detect the occurrence of a line-to-ground fault on the inverter side of an ASD (Chapter 7)

8) The introduction of an algorithm that encompasses steps for reliable line-to-ground fault detection in IPCS

9) The introduction of a non-linear tracking filter to track specific current signature of the current that flows through the line-to-ground fault path (Chapter 8)
2. POWER CONVERTER SYSTEM SETUP AND TOP-DOWN STRATEGY FOR LINE-TO-GND FAULT DETECTION METHOD

This chapter has been included herein for the sake of clarity of the rest of this dissertation. In the first part (section 2.1), the experimental setup that has been used to validate analytical results is presented. In the second part (section 2.2), multi-drive system topologies are introduced. In the third part (section 2.3), a top-down strategy that comprises the steps taken to develop the line-to-ground fault detection method is presented.

2.1. Experimental setup
The experimental setup built to validate analytical results is a 10 HP diode-rectifier-inverter system. The experimental setup has been adequately designed thermally and electromagnetically. The rise time of the power semiconductor switches were adjusted to 400 ns. This can be demonstrated to be a good trade-off between switching losses, reflected waveform overvoltage [18], Electro Magnetic Compatibility (EMC) requirements and compliance with NEMA MG 131 standard for motor insulation. Furthermore, parts were tested for Corona Inception Voltage (CIV) to discard partial discharge. The heat sink and air-cooling system were designed to accommodate switching and conduction losses of the power semiconductor switches. No further details other than electrical are provided for any of these setups since those are out of the scope of this dissertation.

2.1.1. Setup: Diode-rectifier-inverter system
In Fig. 2.1, the experimental setup for the diode-rectifier-inverter system is depicted. Its elements are numerated from 1 to 10, as depicted in Fig. 2.1. Each following section refers to one of these elements. For instance, section 2.1.1.1 describes the 1st element, called incoming power. Section 2.1.1.2 describes the 2nd element, called 2.5 MVA isolation transformer, an so on and so forth.

2.1.1.1. Incoming power
The incoming power is the Southeastern Wisconsin grid. The location of the site that is served is Mequon, Ozaukee county. Through power quality readings, power factor correction instants supplied by the utility were detected. Large disturbance was observed during these scheduled turning-on and turning-off of capacitor banks. Tests to validate results of this dissertation were performed at instants of time at which no scheduled turning-on and turning-off of capacitor banks were performed to avoid distortion.

2.1.1.2. 2.5 MVA isolation transformer
The power rating of the isolation transformer is 2.5 MVA. The primary of the transformer is Δ-connected; and the input voltage is 13.2 KV. The secondary of the transformer is solidly Y-connected; its rating is 480 V. Table 2.1 shows the input inductance and resistance of this transformer, according to the report of the experimental calculation done. The test was performed phase-by-phase. The short-circuit current was as high as 32 KA.

Table 2.1. 2.5 MVA Isolation transformer nominal parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{2.5MVA}$ (inductance at 60 Hz)</td>
<td>12 μH</td>
</tr>
<tr>
<td>$R_{2.5MVA}$ (resistance at 60 Hz)</td>
<td>7.7 mΩ</td>
</tr>
<tr>
<td>$C_{2.5MVA}$ (parasitic capacitance)</td>
<td>2.4 μF</td>
</tr>
</tbody>
</table>

2.1.1.3. Input fuses

The input fuses to the setup are 3 fast-acting, high limiting current Ferraz Shawmut A6T30. This means that the current should not be greater than 30 Arms.

2.1.1.4. 51 KVA isolation transformer

The 51 KVA isolation transformer is a Δ-Y isolation transformer with parameters presented in Table 2.2. Both, primary and secondary, are nominally 480 Vrms line-to-line. Table 2.2 depicts the nominal parameters of such a transformer.

Table 2.2. 51 KVA isolation transformer nominal parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L$ (inductance at 60 Hz)</td>
<td>11.5 mH</td>
</tr>
<tr>
<td>$R$ (resistance at 60 Hz)</td>
<td>0.302 Ω</td>
</tr>
</tbody>
</table>

Connecting this isolation transformer in series with the 2.5 MVA isolation transformer is done to have access to the neutral point of the feeder and for local isolation. An HRG is connected to this neutral.

2.1.1.5. Converter-side electric cable

By default, the converter-side electric cable is unshielded and comprised of 3 phase conductors and 3 ground conductors symmetrically distributed in a bundle. The size is 12 AWG, rated at 600 V. The length of this cable is very short, about 5 m. This cable might be changed from test to test. The actual cable characteristics if changed, are indicated in each simulation or experimental test.

2.1.1.6. Drive

The element drive is comprised of 1) diode-rectifier, as front-end, 2) DC-link capacitor bank and 3) inverter. The next 3 subsections will describe each of these elements.
Fig. 2.1. Diode-rectifier-inverter system
2.1.1.6.1. Diode-rectifier

The front-end of the setup is a 3-phase diode-rectifier. This front-end is not stressed beyond rated power supplied to the load.

2.1.1.6.2. DC-link capacitor bank

The DC-link capacitor bank is comprised of 2 sets of capacitors in series that provide access to the middle point of this connection. The total DC-link capacitance is calculated so as to have DC-link capacitance and converter-side cable inductance determining a filter cut-off frequency of 115 Hz. For the case of this implementation, the DC-link capacitance is 450 µF, or equivalently normalized to 45 µF/Arms.

2.1.1.6.3. Inverter

The speed control technique used is the Volt/Hertz (V/Hz) control, as described in [19], chapter 14, Sect 14.2. The modulator used is the SVPWM with CMV as described in [20]. The DC-link bus voltage, $V_{cap}$, is ridden (i.e., measured) to calculate the duty cycle for the pulses of each phase as shown in (2.1).

$$x_{duty} = \frac{1}{2} \left(1 + \frac{2}{V_{cap}}V_x\right), \quad x=u,v,w$$ (2.1)

The dead-time of the IGBTs used is 3 µs. To limit torque oscillations, the IGBT’s dead-time compensation technique used is the one presented in [21]. If reflected wave effects are neglected [18], [22], [23], electric cables utilized are short compared to the distance a voltage wave travels in the time it takes for an IGBT to open or to close (rise, fall times) [24].

The modulation index is defined as $M = V_{im}/V_{6step}$ where $V_{im}$ is the amplitude of the fundamental of any particular modulation scheme, SVPWM in this dissertation, and $V_{6step}$ is the amplitude of the fundamental of the 6-step modulation. The maximum amplitude of $V_{im}$ within the linear region of the SVPWM is $1/\sqrt{3} V_{cap}$ while the amplitude of the six step modulation is $2/\pi V_{cap}$, which means that for the linear region, the maximum modulation index is $M = 0.9069$.

The control algorithm is updated every 256 µs or every 250 µs. The current, on the other hand, is sampled using asymmetrical S/H to minimize distortion [25].

2.1.1.6.7. Inverter-side electric cable

The inverter-side electric cable is a dominant element of an IPCS with ASDs and deserves special attention. This section is three-fold. First, the cable structures to be used are presented. Second, the cable model to be used is discussed. Third, calculation of cable parameters is made for different cable gauges.

Two cable structures are utilized for simulation/experimentation. The first one of these structures is depicted in Fig. 2.2. It is comprised of 3-phase conductors arranged in a
triangular bundle and 3 bare ground conductors placed in the interstices. The cable is shielded with a 35 mil thick aluminum armor for all gauges. The outer wrap used for calculation of parameters is cross-linked polyethylene (XLPE). Geometric dimensions for different gauges have been obtained from [26] for Cu type cables; and they are presented in Table 2.3. $R_c$ is the radius of the conductor. $D_i$ is the insulation thickness. $D$ is the distance between centers of conductors: $2(R_c+D_i)$.

![Diagram of cable structure]

**Fig. 2.2 Cross-section of symmetric 3-phase cable with 3 symmetrical ground wires**

<table>
<thead>
<tr>
<th>Cable</th>
<th>$R_c$ (mm)</th>
<th>$D_i$ (mm)</th>
<th>$D$ (mm)</th>
<th>$R_g$ (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 MCM</td>
<td>10.3505</td>
<td>1.651</td>
<td>24.003</td>
<td>3.759</td>
</tr>
<tr>
<td>2_0</td>
<td>5.334</td>
<td>1.397</td>
<td>13.462</td>
<td>2.362</td>
</tr>
<tr>
<td>6</td>
<td>2.362</td>
<td>1.143</td>
<td>7.01</td>
<td>1.486</td>
</tr>
<tr>
<td>14</td>
<td>0.9398</td>
<td>0.762</td>
<td>3.4036</td>
<td>0.7365</td>
</tr>
</tbody>
</table>

The cross section of the second cable structure to be used is depicted in Fig. 2.3. It is a 4-conductor asymmetric shielded cable. Phase conductors are named A, B and C. The ground conductor is named G. Geometric dimensions are the same that were presented in Table 2.3: 1) the radius of the conductor is named $R_c$, 2) the XLPE insulation thickness is named $D_i$, 3) the distance between centers of conductors is named $D=2(R_c+D_i)$. The cable is shielded; and it is located in a rack with no ground plane.

The cable model to be used depends on the characteristics of the cable that need to be captured. In this dissertation, the characteristic of the cable that needs to be captured is the current flowing to ground up to frequencies comparable with the carrier frequency of the inverter. Fast rise/fall time of PWM pulses combined with long electric cables create reflected wave effects that the cable model considered accounts for. In case reflected wave effects are attenuated, a terminator [23] can be added at the terminals of a motor which impedance matches the characteristic impedance of the cable. The model should be applicable to asymmetric cable configurations.
Fig. 2.3. Cross-section of 4-conductor asymmetric shielded cable

While transmission line models give more accurate results compared to a lumped parameter or multi-segment RLC model [22], the main drawback is the lack of interaction with various 3-phase modulation schemes that might affect cable/motor waveforms under a multi-pulse train. This lack of interaction is especially detrimental to model accuracy if the electric cable is asymmetric. Furthermore, asymmetry is enhanced in the presence of an asymmetric line-to-ground fault.

From [27], it is clear that a 3-phase segment-based lumped parameter model can be used for the frequency range of interest to obtain results of reasonable accuracy (5% - 10%). Such a model has the advantage of accounting for the interaction between the differential and common modes in a cable. The electrical parameters for this segment-based can be calculated utilizing Finite Element Analysis (FEA). Its advantage is the flexibility of being extended to any cable structure and length. Unlike the methodology to calculate cable electric parameters presented in [28] which is restricted to cases in which the distance between conductors is large with respect to the radius of the conductors, such as in transmission lines, FEA is flexible and can be extended to any cable structure and length. Cable electric parameters for several gauges and cable structures for the per-unit length segment model utilizing FEA for different cable sizes is provided in Appendix A.

The number of segments of the segment-based model is determined taking into account the Band-Width (BW) of interest and the computational time [29]. The natural frequency given by only 1 section of the lumped model for 100 m of the symmetric 3-conductor 3-ground wire 500 MCM cable depicted in Fig. 2.2, for instance, is $f_n = 678.92$ KHz, which is not enough to estimate the current flowing to ground at the carrier frequency (4 KHz). This is due to the multiple resonances present in an electric cable that could be excited by the rich spectrum contained in the rise/fall edges of PMW pulses ($t_rise$). With a 400 ns fall/rise time for good trade-off between EMI and thermal losses, $f_{rise} = 1/(\pi t_{rise}) = 0.8$ MHz. Then, the maximum frequency of interest is 1.6 MHz [30]. From the cable parameters calculated using FEA in Appendix A, it is clear that such a frequency corresponds to the first few resonance/anti-resonance peaks of the input impedance of the cable [29]. This means that
roughly a few segments would be necessary to consider for the cable model. In this dissertation, roughly 5 segments are considered for every 100 m of electric cable. As per recommendation made in [27], the resistance of the cable is lumped at one end of the cable model. The segment model per unit length for the cable structure depicted in Figs. 2.3 is depicted in Fig. 2.4.

For the symmetrical configuration depicted in Fig. 2.2, the \( R \) and \( L \) parameter matrices of a cable can be represented by \( 5 \times 5 \) symmetrical matrices and the \( C \) parameters can be represented by a \( 3 \times 3 \) symmetric matrix as presented in (2.2-3). The off-diagonal elements in \( R \) are due to proximity effect; and they are neglected. In the \( L \) matrix, the diagonal elements represent the self-inductances and the off-diagonal elements represent the mutual inductances. It has been shown in [27] that the \( R \) and \( L \) matrices vary with frequency while the \( C \) matrix does not show significant change with frequency. The values used for (2.2-3) for the simulations done in chapters 4-5 are calculated at 1 KHz.

\[
R = \begin{bmatrix}
R_{Ar} & R_{Arg} & R_{Arw} & R_{Arv} & R_{Arw} \\
R_{Arg} & R_{g} & R_{gw} & R_{gv} & R_{gw} \\
R_{Arw} & R_{gw} & R_{Ar} & R_{Arw} & R_{Arv} \\
R_{Arv} & R_{gv} & R_{Arw} & R_{Ar} & R_{Arv} \\
R_{Arw} & R_{gv} & R_{Arv} & R_{Arw} & R_{Ar} \\
\end{bmatrix}
\]

\[
L = \begin{bmatrix}
L_{Ar} & M_{Arg} & M_{Arw} & M_{Arv} & M_{Arw} \\
M_{Arg} & L_{g} & M_{gw} & M_{gv} & M_{gw} \\
M_{Arw} & M_{gw} & L_{Ar} & M_{Arw} & M_{Arv} \\
M_{Arv} & M_{gv} & M_{gw} & L_{Ar} & M_{Arv} \\
M_{Arw} & M_{gw} & M_{Arw} & M_{Arv} & L_{Ar} \\
\end{bmatrix}
\]

\[
C = \begin{bmatrix}
C_{ug} & C_{uv} & C_{uw} \\
C_{uvg} & C_{uv} & C_{uw} \\
C_{uvw} & C_{v} & C_{uw} \\
\end{bmatrix}
\]

\[
(2.2)
\]

\[
(2.3)
\]

![Fig. 2.4. Multiple-segment lumped-parameter electric cable model](image)

2.1.1.8. Load: motor

The motor used by default is the 10 HP Reliance Electric L0194A. A model of this motor that can be connected to the cable model presented in a previous section and provides an
estimate of the current flowing to ground before and after a line-to-ground fault has occurred is utilized. For such, a 3-phase equivalent circuit with capacitances coupling to ground is depicted in Fig. 2.5. This model was introduced in [31] and it is easy to characterize, although its low-order only allows for limited accuracy. This model will only be used to aid with the analysis. The electric parameters for the 10 HP motor are presented in Table 2.5. Differential Mode (DM) and Common Mode (CM) magnitude and phase frequency response plots are depicted in Fig. 2.7 and compared with those of measured data. Corresponding parameters for other motor power ratings are given in Appendix B.

![3-phase motor model with capacitive coupling to ground.](image)

**Fig. 2.5. 3-phase motor model with capacitive coupling to ground.**

<table>
<thead>
<tr>
<th>C₁</th>
<th>C₂</th>
<th>R₁</th>
<th>R₂</th>
<th>R₃</th>
<th>R₄</th>
<th>L₁</th>
<th>L₂</th>
<th>L₃</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 nF</td>
<td>1.15 nF</td>
<td>100 Ω</td>
<td>190 Ω</td>
<td>2000 Ω</td>
<td>0.5 Ω</td>
<td>10.8 mH</td>
<td>6.85 mH</td>
<td>100 nH</td>
</tr>
</tbody>
</table>

**2.1.1.9. Contactor and line-to-ground fault resistor**

A contactor between one of the lines and a variable resistor, set by default at 10 Ω, is used in this test-bed. It will be opened or closed to emulate the occurrence of a non-arc line-to-ground fault. The resistor value, if changed, is indicated.

**2.1.1.10. Grounding resistor at the neutral of the 51 KVA isolation transformer**

By default, a 106 Ω HRG is connected between the neutral of the 51 KVA isolation transformer and ground. The HRG value is not unique. The actual value, if changed, is indicated in each test throughout this dissertation.
Fig. 2.7. Magnitude and phase frequency response plots of Differential Mode (DM) and Common Mode (CM) for a 10 HP motor

2.2. Multi-drive system topology

The line-to-ground fault detection method developed in this dissertation can be extended to multi-drive systems. A multi-drive system topology is presented in this section.

In Fig. 2.13, a compact view of the systems explored in the previous section is depicted. Two subsystems: 1) ASD-load and 2) inverter-load are formed as indicated. They are used to build complex multi-drive systems for which the line-to-ground fault detection method developed should be reliable.

Multi-drive systems are a common application among IPCS. Among the different topologies of multi-drive systems, that will be utilized later in this dissertation are mentioned: 1) Single AC Source / Multi-drive system, 2) Common DC-bus / Multi-drive system. These are depicted in Fig. 2.14 and Fig. 2.15.

Multi-drive system topologies might influence the setting of the voltage/current threshold for the developed line-to-ground fault detection method. Furthermore, they might be
determinant to define the line-to-ground fault method and specifics about voltage/current signature selected.

Fig. 2.13. Electric network, 1 ASD & 1 ground loop

Fig. 2.14. Single AC-source / Multi-drive system
2.3. Top-down strategy

In this section, a top-down strategy for the rest of this dissertation (chapters 3-10) is presented. This top-down approach will help clarify the contents of the rest of this dissertation. The steps of the top-down strategy are as follows.

1. Initially, a brief survey on existing methods to detect line-to-ground faults (both voltage and current signature based) to familiarize the reader with the available solutions is presented.

2. Next, models for the systems described in section 2.1 are introduced. These models are simple and provide a better understanding of the power electronic conversion that is happening. Furthermore, they are useful tools to analyze the system and extract information of interest that will help in the development of a reliable line-to-ground fault detection method.

3. The next step is to point out issues, non-idealities or difficulties that need to be addressed in order to construct a reliable method to detect line-to-ground faults. The models developed in Chapter 4 are utilized to simplify the analysis. The first difficulty found is how to set the threshold to be used to compare the signature utilized to detect the occurrence of a line-to-ground fault. This is discussed in Chapter 5.

Another and more subtle issue is then addressed: the electro-magnetic interaction of multiple ground loops. There is a geometric and spatial effect that has been ignored in the specialized literature and in Chapter 6 this is addressed.

Recommendations from chapters 5-6 are: 1) HRG value 2) how to set a voltage/current threshold, 3) specific harmonic content (signature) to track in order to detect a line-to-ground fault.

4. The next step is to determine if voltage or if current is the more appropriate signature to detect the occurrence of a line-to-ground fault. Primarily, reliability and the ability to detect the faulted drive in a multi-drive system are used to evaluate the more appropriate method. Existent methods and proposed methods based on voltage/current signature measurements are discussed in Chapter 7. The model developed in Chapter 4 is used with success to aid in the understanding and development of the methods proposed. The recommendation from this step is that current rather than voltage should be measured to maintain the reliability of the line-to-ground fault method for systems comprised of multiple drives.

5. The next step is the formulation of an algorithm that encompasses findings and recommendations made in the previous steps. The algorithm has an on-line version
and an off-line one, which are covered in Chapter 8. Along with this algorithm, a filter to track changes in the frequency of specific harmonic(s) is introduced.

Fig. 2.15. Common DC-bus / Multi-drive system
3. SUMMARY OF PREVIOUS LINE-TO-GROUND FAULT DETECTION TECHNIQUES

Aging, overvoltage, parasitic currents, and high-current-drawing events are responsible for cable insulation breakdown, which lead to electric faults. The energy released during a fault can generate process interruptions, equipment damage, and, even worse, fire and explosion risk for personnel. Incorporating HRG in an electric system provides the advantage of avoiding unscheduled shutdowns of the system and further damage to the system.

Reliability, continuous operation, and controlled shutdown of power are regarded as desirable, if not mandatory, characteristics of IPCS. Fig. 3.1 depicts a simple IPCS with only one ASD and one load (a motor in this case). Such an IPCS is connected to a grid represented by a generator through an isolation transformer. The primary of the isolation transformer has been set to 13.2 kV. The secondary of the same transformer has been arbitrarily set to 480 V, a standard for low-voltage systems. This simple IPCS is used to describe the existing line-to-ground fault detection methods in HRG systems.

![Fig. 3.1. Simplified network](image)

In Fig. 3.2 a more detailed diagram of the situation depicted in Fig. 3.1 is illustrated. Line-to-ground faults are depicted as occurring between the front-end converter (diode rectifier or PWM converter) and the isolation transformer (mains side) or between the inverter and the load (load side). This work is only concerned with the detection of a first line-to-ground fault at the load side of the ASD. Such a method, however, as discussed in the previous chapter will be extended to systems comprised of multiple ASD.
3.1. Detection of line-to-ground faults in HRG systems background

The identification of line-to-ground faults in HRG systems is performed by analyzing the voltage signature or the current signature [4]. Depending on the location of the fault, voltage or current through the resistor between neutral and ground of the isolation transformer of the IPCS might or might not provide accurate information about the occurrence of the first line-to-ground fault in the system. This is explored in Chapter 8. A line-to-ground fault too close to the neutral of the load might not provide a sufficient fundamental or DM current signature level to identify the presence of a fault. Moreover, asymmetric magnetic coupling could eliminate differential mode current and voltage through the fault path (Chapter 7). The next sections briefly discuss detection methods based on voltage and/or current.

3.1.1. Voltage signature-based line-to-ground fault detection

There are several well-documented methods for detecting the presence of a line-to-ground fault that employ voltage detection across the grounding resistor or the voltage-to-ground at each phase [42]. A single-processor system can monitor line-to-neutral voltages with the voltage transformers that would be used for normal system voltage measurement. With the line-to-ground voltages identified, the grounded phase should be discernable [4].

Cyclic pulsing fault location [7] provides information about the occurrence of a line-to-ground fault in an IPCS with HRG. The location of such a fault, however, requires an operator to manually test each individual ASD. For systems without ASDs, it is recommended to set the threshold of CMV above the charging current for line-to-ground parasitic capacitance of downstream feeder circuit, times the impedance of the HRG. For IPCS with ASDs, however, this recommendation does not hold, since the topology and/or start of new ASDs has an effect on the total CMV present in the system [5].
A solution that includes voltage sensors at the terminals of each ASD could be adequate to identify the occurrence of a line-to-ground fault. Moreover, this solution would provide information of which phase and what ASD is faulted. It is necessary to understand the advantages and disadvantages of methods based on voltage measurement. They are further explored in Chapter 7.

3.1.2. Current-signature-based line-to-ground fault detection

Five current-signature-based line-to-ground fault detection methods are revisited:

1) Detection at the HRG [4]: This method is depicted in Fig. 3.3. Detecting a line-to-ground fault by measuring the current that flows in the HRG requires dedicated hardware and signal-processing capabilities. In complex IPCS, to service this fault would require an operator to manually find it. This could be difficult depending on the particular system.

2) Detection based on tracking of particular current signature [17]: This method is depicted in Fig. 3.4. A diagnostic signal is injected to the IPCS system at the location of the HRG. This diagnostic signal is detected at the terminals of the inverter side of each ASD. This method is modular and inserts a CMV signal to the system. However, the signal must be relatively high. This translates into a significant signal processing power requirement. In addition, it is difficult to set a threshold if the system is reconfigurable (each ASD turns on or off at non-defined instants).

3) Detection based on the sum of the inverter side currents [16]

This method is depicted in Fig.3.5. The detection mechanism is a current transformer placed around the 3 lines at the inverter side of the ASD. A threshold is selected for the maximum permissible of fundamental current that is allowed to circulate. This needs to be adjusted, which is difficult [5]. In Chapter 6, it is demonstrated that the magnetic coupling between
lines at the inverter side could hide the occurrence of a line-to-ground fault. The line-to-ground fault detection method described, therefore, needs to be carefully implemented.

Fig. 3.4. Line-to-ground fault detection at the inverter-side of an ASD based on tracking of particular injected current signature

Fig. 3.5. Line-to-ground fault detection based on the sum of the inverter side currents

4) Detection through integrated DC inductor [15]
This method is depicted in Fig. 3.6. It is based on the current signature at the positive rail or at the negative rail of the DC-link. It is claimed that it allows for detection of line-to-ground faults at the DC-link through the mains 3rd harmonic current component found in the ripple of either DC-link rail. It is also claimed that faults at the inverter side of the ASD can be detected by tracking the carrier. However, this method requires extra hardware and special magnetic design of DC-link choke. Moreover, tracking the carrier of the inverter is not an easy task. The current flowing to ground through parasitic capacitance might make adjusting a threshold difficult and demand significant digital signal processing that increases the cost of the solution. Finally, it is observed that this method might be limited to ASD with a diode-
rectifier as front-end. This is because in an ASD with an Active-Front-End, the mains ripple and carrier are usually attenuated by converter control and synchronizing the carriers of the converter and the inverter.

5) Detection through integrated AC inductor [15]

This method is similar to the one described in 4). Instead of an integrated DC inductor, an integrated AC inductor is used, as it is illustrated in Fig. 3.7.

In the next chapter, some limitations of existing techniques to detect line-to-ground fault currents at the inverter side of ASDs are discussed. These limitations were mentioned in Chapter 1 and include 1) sensor-related problems and 2) magnetic coupling-related problems.
4. POWER CONVERTER MODELS FOR INDUSTRIAL SYSTEMS

The objectives of this chapter are to gain understanding and to develop a model of Voltage Source ASDs (VSASD) for fast evaluation of effects that harmonic components of interest have on a VSASD. Special emphasis is given to maintaining integrity of Common Mode Voltage (CMV) and Differential Mode Voltage (DMV) present in the exciting voltage source such that the developed model can be utilized to analyze the effect of the occurrence of a line-to-ground fault in an ASD. This model can be used to extend the analysis to more complex systems comprised of several ASDs integrated in larger power systems, as it is discussed in Chapter 7.

VSASDs or simply ASDs are comprised of a converter front-end, a DC-link and an inverter. Also some passive filtering to reduce Total Harmonic Distortion (THD) and/or provide a known path for switching frequency harmonics (and/or common mode current) can be included at either the input side (between grid and converter), the DC-link or the output side (between ASD and load).

The DC-link in most VSASDs is designed to provide effective isolation between mains and load. This is achieved by appropriately sizing the capacitor bank, boosting the DC-voltage (active front-end) and/or controlling the modulator of the inverter to mitigate bus ripple [20]. The effect of decoupling mains and load is that, under certain conditions, an ASD can be approximated by interconnecting separate models of converter and inverter. The power converter models should maintain the integrity of the common mode and differential mode networks such that fault paths are maintained.

4.1. Converter: diode-rectifier front-end
Fig. 4.3 depicts a diode-rectifier configuration wherein the inverter and load are simplified. The development of an equivalent major component model that retains important converter characteristics is desirable for the analysis and protection of industrial systems. Line filtering has been lumped as an inductor on the DC-side of the converter.

The load can be modeled by the two resistors $R_{pos}$ and $R_{neg}$. A fault is modeled by switch closure through $R_f$. Modeling the load by two resistors allows for modeling various fault conditions on the load side. For example, setting $R_{pos} = R_{neg}$ corresponds to the case of a 3-phase fault on the load side of the power converter; the fault is either a bolted fault ($R_f = 0$) or one through fault resistance $R_f$. In this case, the only contributor to ground current is CMV. Cases in which $R_{pos} \neq R_{neg}$ correspond to unsymmetrical faults like a line-to-ground fault. As is shown below, the fault in this case is excited by both common and differential dc link sources.

These basic conclusions are important when applying the complete model for a power converter because the dominant common and differential mode signatures are maintained. These signatures allow for developing enhanced fault detection, protection and diagnostic algorithms. Furthermore, they contribute to the extension of symmetrical components to include power converters.

![Diode Rectifier Diagram]

Fig. 4.3. Test circuit for equivalent model of the diode-rectifier

The upper diodes portion of a diode-rectifier connected to a voltage source is depicted in Fig. 4.4. At any time, at least one of the diodes is required to conduct in order to avoid open-circuit condition of the inductor (current source). The upper diodes within the rectifier can be modeled by a 3-throw switch connecting the 3-phase source to the positive rail of the DC-bus as depicted in Fig. 4.5. Then, if $d_{ap}$, $d_{bp}$ and $d_{cp}$ are defined as the time intervals within one cycle of the fundamental of the AC voltage sources when $D_1$, $D_3$ and $D_5$ conduct, respectively, then continuous current (1-logical) is maintained through the inductor as established in (4.1). Therefore, voltage sources and upper switches of the rectifier can be replaced and represented by (4.2) and (4.1). Similarly, the source interacting with the lower-part of the rectifier can be represented by (4.3). In (4.2-3), the sources $v_p$ and $v_n$ can be
thought as the ripple on the positive rail and on the negative rail of the DC-link plus half of
the differential voltage, respectively, measured from the virtual neutral of the diode-rectifier.
They are indicated in Fig. 4.7
\[ d_{op} + d_{op} + d_{cp} = \text{1 - logical} \] (4.1)
\[ v_p = \begin{bmatrix} d_{op} & d_{op} & d_{cp} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \] (4.2)
\[ v_n = \begin{bmatrix} d_{op} & d_{on} & d_{cn} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \] (4.3)

Fig. 4.4. Diode-rectifier: a) upper switches

The reference to ground is established by connecting \( R_n \) to the equivalent circuit. This is
fundamental to keep common voltage characteristics or return of line-to-ground fault current
to source. The neutral point of the 3-phase voltage source, \( N \), and the virtual neutral of the
sources \( v_p \) and \( v_n \) are at the same potential. The corresponding state-space equations can be
written by selecting 3 states: the currents through the inductors \( (i_p \text{ and } i_n) \) and the voltage in
the capacitor \( (v_{cap}) \). These equations are given in (4.4)-(4.6).

\[ p_i_p = -\frac{2}{L} \left[ \left( R_{pos} + R_f + R_n - \frac{R_{pos}^2}{R_{pos} + R_{neg}} \right) i_p + \left( R_f + R_n + \frac{R_{pos} R_{seg}}{R_{pos} + R_{seg}} \right) i_n + \frac{R_{pos}}{R_{pos} + R_{neg}} v_{cap} - v_p \right] \] (4.4)

\[ p_i_n = -\frac{2}{L} \left[ \left( R_f + R_n + \frac{R_{pos} R_{seg}}{R_{pos} + R_{neg}} \right) i_p + \left( R_f + R_n + R_{seg} - \frac{R_{seg}^2}{R_{pos} + R_{seg}} \right) i_n + \frac{R_{seg}}{R_{pos} + R_{seg}} v_{cap} - v_n \right] \] (4.5)

\[ p v_{cap} = \frac{1}{C} \left[ \frac{R_{pos}}{R_{pos} + R_{neg}} i_p - \frac{R_{neg}}{R_{pos} + R_{seg}} i_n - \frac{1}{R_{pos} + R_{seg}} v_{cap} \right] \] (4.6)
Fig. 4.5. Diode-rectifier upper switches equivalent switching function

Equivalently, the 3-phase topology can be seen as a 1-phase circuit, as illustrated in Fig. 4.6. Presenting this system in this form, it is easy to visualize its symmetry. It can be demonstrated that the connection of $R_n$ to $N$ holds as long as the commutation intervals of the diode-rectifier are small, which is the case for most normal converter operation designs. The load can be modeled by the two resistors $R_{pos}$ and $R_{neg}$. A fault is modeled by switch closure through $R_f$. Modeling the load by two resistors allows for modeling various fault conditions on the load side. For example, setting $R_{pos}=R_{neg}$ corresponds to the case of a 3-phase fault on the load side of the power converter; the fault is either a bolted fault ($R_f=0$) or one through fault resistance $R_f$. In this case the only contributor to ground current is CMV. Cases where $R_{pos} \neq R_{neg}$ correspond to unsymmetrical faults like the case in which a line-to-ground fault occurs. As is shown below, the fault in this case is excited by both common and differential DC link sources.

These basic conclusions are important when applying the complete model for a power converter because the dominant common and differential mode signatures are maintained. These signatures allow for developing enhanced fault detection, protection and diagnostic algorithms. Furthermore, they contribute to the extension of symmetrical components to include power converters.

An expression for the voltage between 0 and $N$, $v_{0N}$, would be useful to tie converter and inverter, as it will be shown later. From Fig. 4.6, it can be demonstrated that $v_{0N}$ takes the form shown in (4.7). It establishes that $v_{0N}$ is a function of positive and negative voltage sources and the rate of change of the current that circulates on the line-to-ground fault path, $i_f$. Moreover, as it has been shown, the line-to-ground fault current $i_f$ is sourced by differential and CMV sources. Therefore, the voltage $v_{0N}$ is a function of differential voltage and CMV sources, which means that $v_{0N}$ is not simply CMV.

$$v_{0N} = \frac{v_p + v_n}{2} - \frac{L}{4} \frac{d}{dt} i_f$$  \hspace{1cm} (4.7)
If the e.m.f. induced across the inductors depicted in Fig. 4.6 is small in comparison with the voltage stored in the capacitor, the voltage $v_{0N}$ can be approximated to the converter CMV. Using the model derived, this expression can be written as in (4.8).

$$v_{0N} \approx CMV_{\text{conv}} = \frac{v_p + v_n}{2}$$  \hspace{1cm} (4.8)

In Fig. 4.7, $v_p$ and $v_n$ are the upper and lower portions of the 3-phase voltage sources; $\theta$ is the angle of the mains voltage. The approximated value of twice the converter CMV, $CMV_{\text{conv}}$, is also indicated. $CMV_{\text{conv}}$, therefore, represents the effect that the converter has on the ASD system besides its purpose of transmitting usable power to the load. It is a potential source of energy that requires a circuit path to close around it to drive any current.

A Fourier series for the converter CMV would be useful to identify the harmonic components of the voltage that could drive current harmonic components through the line-to-ground fault path. From the relations given in (4.2-3), expressions for $v_p$ and $v_n$ can be found. They are given in (4.9-10). Notice that this converter CMV has quarter-wave, odd symmetry. Then, only the $b_k$ (odd) coefficients of a Fourier series expansion are non-zero. Such coefficients are given in (4.13).
The resulting diode-rectifier CMV Fourier expansion is given in (4.14). This is an infinite series of harmonics of the fundamental: 3rd, 9th, 15th, 21st, 27th, etc. that will source currents through the CMV circuit. The harmonics found in Fig. 4.7 correspond to this case.

\[ v_p = V \sin \left( \theta + \frac{2\pi}{3} \right), \quad 0 < \theta \leq \frac{\pi}{6} \]  
\[ v_n = V \sin \left( \theta - \frac{2\pi}{3} \right), \quad 0 < \theta \leq \frac{\pi}{6} \]  
\[ b_k = \frac{4}{k} \int_0^{\theta} \sin (kx) \frac{V \sin \left( \frac{x + 2\pi}{3} \right) + V \sin \left( \frac{x - 2\pi}{3} \right)}{2} \, dx \]  
\[ \sin \left( \frac{x + 2\pi}{3} \right) + \sin \left( \frac{x - 2\pi}{3} \right) = 2 \sin \left( \frac{x}{3} \right) \]  
\[ b_k = -V \frac{3}{\pi k^2 - 1} \sqrt{3} \sin \left( \frac{k\pi}{2} \right), k = 1, 3, 5, \ldots \]  

The resulting diode-rectifier CMV Fourier expansion is given in (4.14). This is an infinite series of harmonics of the fundamental: 3rd, 9th, 15th, 21st, 27th, etc. that will source currents through the CMV circuit. The harmonics found in Fig. 4.7 correspond to this case. The expression in (4.14) is called Low-Frequency Converter CMV (LFCMVconv). This use of the term low-frequency (since (4.14) has a theoretical infinite spectrum) is useful to facilitate the writing of this dissertation.

The quasi-triangular waveform indicated by (4.14) is illustrated in Fig. 4.7. The fundamental of such a quasi-triangular waveform is a 3rd harmonic of the fundamental of the input voltage sources. Notice that this almost triangular waveform has been obtained by adding portions of sinusoidal waveforms.

In following sections 4.1.2-3, possible refinements to the model presented are indicated. They are beyond the scope of this dissertation and left for future research.

4.1.2. Effect of a line reactor and line impedance on the diode-rectifier CMV

When certain conditions, given in the previous section, are satisfied, \( v_{0W} \) can be approximated by (4.14). For such a calculation, the inductance was assumed to be lumped at the DC-side of the diode-rectifier. If instead of the DC-link choke, a line reactor and source impedance were included, then the calculation of \( v_p \) and \( v_n \) would have to account for it.

4.2. Inverter model

The focus of this section is to find a model for the circuit depicted in Fig. 4.11. The inverter is fed by 2 stiff DC voltage sources, each at a potential \( v_{Conv}/2 \) as indicated. If the stiff sources were replaced by capacitors as in the DC-link of an ASD, calculating the duty cycles of each
switch of the inverter through actual measurement of the DC-link would allow for effective isolation between converter and inverter [20]. This is commonly known as riding the bus. A line-to-ground fault is represented by $R_f$. A return path for the line-to-ground fault current through the middle point between the DC voltage sources is established through $R_n$.

![Diagram](image)

*Switching State: 100 (T_1 active, T_3 and T_5 inactive)*

Fig. 4.11. Inverter in a particular state

Similar to the case in which the converter was a diode-rectifier, a virtual neutral could be established for the inverter depicted in Fig. 4.11. The potential of this virtual neutral can be made the potential of the middle point of the DC-link voltage displaced by the CMV generated by the inverter. The circuit constructed can be depicted as in Fig. 4.12. The virtual neutral of this model of the inverter is named $N_v$. Further simplifications to this system are not easy since this kind of line-to-ground fault is asymmetric.

The voltage sources depicted in this model can be calculated. They are a function of the modulation. Voltages sources $v^*_U$, $v^*_V$ and $v^*_W$ form the basis for the DMV of the inverter. The voltage source $v_0$ represents the CMV of the particular PWM modulator technique used. Since it is not the purpose of this dissertation to study the particularities of every modulator, one modulator in particular is chosen and used to obtain the desired model of the PWM inverter. The interested reader can refer to [20], [43], [44], [45], [46] to understand the details of any other particular continuous or discontinuous modulator.

The particular modulator used in this dissertation is the well-known Space-Vector-Pulse-Width-Modulator (SVPWM) and it was originally presented in [47] and later in [48], from which it took the name. The source $v_0$ is generated for the case in which the modulator used is the SVPWM by employing the minimum magnitude test, in which the magnitudes of the three reference signals are compared; and the signal of minimum magnitude is selected; then, it scales down this signal by 0.5. Notice that if the inverter operates within the linear region of the modulator, this $v_0$ is identical to the negative of the diode-rectifier CMV, as defined in (4.14) for the specified constraints, for the case in which the mains voltages and the inverter
voltage sources are in phase and of the same magnitude. For instance, if (4.15) holds, then the inverter CMV can be calculated as in (4.16). Similar relationships are established for \( v_0^* \) and \( v_w^* \). In Fig. 4.13, typical SVPWM waveforms before the modulation is applied are depicted.

\[
|v_0^*| \leq |v_u^*| |v_w^*| \\
v_0 = 0.5v_u^* 
\]  

(4.15)  
(4.16)

Fig. 4.12. Equivalent circuit to the one depicted in Fig. 4.12

If the amplitude of the average line-to-virtual-neutral voltages sourced by the inverter is given as \( V \), and its period as \( 3T \), \( v_0 \) can be expanded as a Fourier series. The waveform has periodic, odd, quarter-wave symmetry. Similarly to (4.14), then, \( v_0 \), which will also be called Low-Frequency Inverter CMV (LFCMV\(_{\text{INV}}\)), can be written as in (4.17).

\[
v_0(t) = V \frac{3}{\pi} \sum_{k=1,3,5,...} \frac{1}{9k^2 - 1} \sqrt{3} \sin \left( \frac{k \pi}{2} \right) \sin \left( \frac{k \pi t}{T} \right) 
\]  

(4.17)

The effect of the modulation can be added to the system depicted in Fig. 4.12. A 2-level inverter has 8 switching states: 1) 6 active states (100, 110, 010, 011, 001, 101), and b) 2 zero states (111, 000). The numerals correspond to the state of the upper switches of the inverter (\( T_1, T_3, T_5 \) as depicted in Fig. 4.11). Active switches are represented by a 1-logical. Inactive switches are represented by a 0-logical. Fig. 4.14 depicts possible scenarios for the switching of the IGBTs and the corresponding inverter CMV when the effect of such switches is considered. The inverter CMV or \( CMV_{\text{INV}} \) has a spectrum much richer than the one of (4.17). This CMV is due to having the virtual neutral of the inverter never fixed but switching between different voltage levels. Since the common mode distributes symmetrically around the level set by the middle point of the DC-link capacitor, 4 possible \( CMV_{\text{INV}} \) levels are feasible as depicted in Table 4.1 and in Fig. 4.20. The \( CMV_{\text{INV}} \) can be calculated as in (4.18).

\[
CMV_{\text{INV}} = \frac{1}{3} (V_{no} + V_{vo} + V_{wv}) = V_{no} 
\]  

(4.18)
Notice that (4.18) assumes symmetric cable and load in the system depicted in Fig. 4.12. To measure the inverter CMV, an ideally infinite Y-connected resistor can be connected right at the terminals of the inverter. The inverter CMV is the potential difference between the neutral of such a Y-load and the middle point of the DC-link.

Specific harmonic components of the DMV and the CMV of the inverter can be calculated in the frequency domain. In Appendix D, details of the frequency-domain calculations for the inverter model are provided.

The inverter low-frequency CMV \( (LFCMV_{INV}) \) corresponds to the harmonics of (4.17). The high-frequency CMV \( (HFCMV_{INV}) \) corresponds to the switching frequency and sidebands due to intermodulation of switching frequency and \( LFCMV_{INV} \). Notice that \( LFCMV_{INV} \) and \( HFCMV_{INV} \) are arbitrary names and have been given to facilitate the writing of this dissertation.

Very-high-frequency CMV phenomena (generated by fast rise and fall edges of IGBT’s switching) like reflected wave (in the order of MHz) [22], [23] might affect the voltage levels defined for several component of \( HFCMV_{INV} \). On applications in the field, either appropriate cable length [24], [29], or a terminator [23] can be utilized to attenuate such high frequency effect.

The total CMV sourced by the inverter can be written as the sum of \( LFCMV_{INV} \) and \( HFCMV_{INV} \) as shown in (4.19). \( v_{CMV\_INV} \) will also be called simply inverter CMV.

\[
v_{CMV\_INV} = LFCMV_{INV} + HFCMV_{INV}
\] (4.19)

Fig. 4.13. Typical SVPWM waveforms before modulation is applied
32

Switching logic

\[
\begin{align*}
T_1 & : 0 1 1 1 1 1 0 \\
T_3 & : 0 0 1 1 1 0 0 \\
T_5 & : 0 0 0 1 0 0 0
\end{align*}
\]

Common mode

\[
\begin{align*}
\frac{v_{\text{Cap}}}{2} \\
\frac{v_{\text{Cap}}}{6} \\
-\frac{v_{\text{Cap}}}{6} \\
-\frac{v_{\text{Cap}}}{2}
\end{align*}
\]

Potential of middle point of capacitor

Fig. 4.14. IGBT switching cases and resulting common mode

Table 4.1. CMV levels for active and inactive states

<table>
<thead>
<tr>
<th>State</th>
<th>CMV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>$\pm \frac{v_{\text{Cap}}}{6}$</td>
</tr>
<tr>
<td>Zero</td>
<td>$\pm \frac{v_{\text{Cap}}}{2}$</td>
</tr>
</tbody>
</table>

In Fig. 4.15, the p.u. spectrum (p.u. base $= 2/\sqrt{3}v_{\text{Cap}}$, $M = 0.9$) of the inverter CMV is depicted for the particular case when the ratio of the carrier frequency and the modulated waveform frequency is 32. The x-axis represents the harmonic number. Only a few of the harmonics are tagged. The first CMV component and its baseband components are the $3^{\text{rd}}$, $9^{\text{th}}$, $15^{\text{th}}$, $21^{\text{st}}$, $27^{\text{th}}$... harmonics of the fundamental. Carrier components include the carrier $f_c$ and sidebands at $f_c \pm 6f_{\text{mod}}$, $f_c \pm 12f_{\text{mod}}$, $f_c \pm 18f_{\text{mod}}$ and so forth and so on. The next set centers around $2f_c$ and appears at $2f_c \pm 3f_{\text{mod}}$, $2f_c \pm 9f_{\text{mod}}$, $2f_c \pm 15f_{\text{mod}}$, etc. Notice that the first carrier sideband harmonics are even multiples of the third harmonic of the fundamental. This occurs because the triangular common mode voltage injection contains multiple triplen harmonics. The higher order triplen components increase the magnitude of the outer sideband harmonics. Then, when calculating the magnitude of a particular harmonic frequency, all harmonics that have the same resultant frequency should be added, as phasor quantities. This could lead to reinforcement or cancellation of some harmonics. Moreover, the increased lower-end carrier first sideband harmonics of the CMV can lead to intrusion of fundamental-
frequency sub-harmonics. This is more severe when lower $f_c / f_{mod}$ ratios are defined. Other harmonics can be generated due, purely, to the effect of the kind of sampling used.

![Inverter CMV (fcarrier/fmodulated=32)](image)

Fig. 4.15. Magnitude spectrum of the inverter CMV

The case in which the ratio between carrier and modulated waveforms is small enough (i.e., carrier sideband harmonics capable of creating subharmonics), should be avoided in practical implementations. Having a non-integer ratio between carrier and modulated waveform should be treated in a similar way (i.e., avoiding small $f_{carried}/f_{modulated}$ ratios). In Chapter 5, the $v_{CMV_{INV}}$ spectrum is further explored and compared with the spectrum of line-to-line voltage measurements.

In practical implementations, there are other problems to be aware of. Some of these are: 1) sampling and PWM implementation, 2) DC-link ripple, 3) dead-time, 4) IGBT switching characteristics. These could create an even richer harmonic spectrum than the one depicted in Fig. 4.15, due to intermodulation. These effects are outside the scope of this dissertation; and they are left aside for future research.

A reconstruction in time-domain requires knowledge of the relative phase of the constituting harmonics. This can be easily calculated from the magnitude spectrum given in Appendix D using the discrete Hilbert transform, for instance. Only the magnitudes of the corresponding harmonics, however, are utilized in this dissertation. This is because the real advantage of this frequency based model is the ability of independently considering the effect of each harmonic component or a few selected components. For the case in which the added effect of several harmonics is required, only an RMS calculation is considered.
4.3. Diode-rectifier-inverter system model

As it was established at the beginning of this chapter, the model derived for the diode-rectifier-inverter system should maintain the integrity of the common mode and differential mode currents that flow through the line-to-ground fault path, for the case in which a line-to-ground fault occurs on the inverter side of a diode-rectifier-inverter system. If the diode-rectifier-inverter system is isolated (i.e., no other 3-phase loads are connected at the PCC), joining the models found for the diode-rectifier and for the inverter, under the constraints specified for the diode-rectifier (i.e., no diode discontinuous conduction), can be done using the expression derived in (4.14) and in (4.7-8).

In (4.14), an expression is given for the voltage between the potentials 0 and N, $v_{0N}$, when it can be approximated by the $CMV_{CONV}$. Also, the inverter side model has been referred to the potential 0. Therefore, a model of an isolated diode-rectifier-inverter system that can be used to qualify and quantify the line-to-ground fault current, under the restrictions given, is depicted in Fig. 4.16.

Fig. 4.16. Proposed equivalent model of the diode-rectifier-inverter system

The current through the line-to-ground fault path is sourced by the converter CMV and by the voltage sources $v_{U0_{INV}}$, $v_{V0_{INV}}$ and $v_{W0_{INV}}$. The rest of this dissertation follows assuming the model depicted in Fig. 4.16 holds for the case in which the system is comprised by a diode rectifier, inverter, electric cable and load.

4.5. Simulation and experimentation results

The magnitude of the harmonic components that comprise the current through the line-to-ground fault path from the test-beds 1 and 2 described in Chapter 2 and the models introduced in this chapter are compared with the purpose of validating the equivalent circuit model developed before. In Fig. 4.18, the measured current through the fault path for Test-bed 1 in time-domain is depicted. The total resistance from the point the line is faulted to the
neutral of the isolation transformer is 60 Ω. The mains operates at 60 Hz. The inverter operates at 50 Hz. The control algorithm is updated every 250 μs. The electric cable used is a 50 ft, 4-wire, asymmetrical non shielded 12 AWG.

![Experimental current through fault path at 50 Hz operating speed](image)

Fig. 4.18. Current through line-to-ground fault path Test-bed 1 in the time domain

In Fig. 4.19, the comparison of magnitude spectra of the current through the fault path in the experimental setup and the model elaborated in this chapter is depicted. The electric cable utilized for this experiment is only 20 ft and expected not to affect significantly the current signature in the frequency range of interest.

As expected from the model developed in this chapter, there are harmonic components at the fundamental frequency, the 3rd harmonic of the mains frequency, the 3rd harmonic of the inverter operating frequency, the respective 9th harmonics, etc. Also, there is a harmonic component at 4 kHz, and at its corresponding sidebands. In Table 4.2, a few representative harmonics of Fig. 4.19 are presented.
Fig. 4.19. Comparison of the current through line-to-ground fault path in the diode-rectifier-inverter Test-bed 1: a) experimentation setup and b) simulation

Table 4.2. Comparison between the experimentation setup and the simulation setup of harmonics of the current through the line-to-ground fault for Test-bed 1

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>50 Hz</th>
<th>150 Hz</th>
<th>180 Hz</th>
<th>3900 Hz</th>
<th>4000 Hz</th>
<th>4200 Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exp</td>
<td>Sim</td>
<td>Exp</td>
<td>Sim</td>
<td>Exp</td>
<td>Sim</td>
<td>Exp</td>
</tr>
<tr>
<td>4.2</td>
<td>4.18</td>
<td>0.82</td>
<td>0.87</td>
<td>0.97</td>
<td>1.10</td>
<td>0.47</td>
</tr>
</tbody>
</table>
The major differences between harmonics are in the carrier and in the sideband components of the carrier. They could be due to modeling errors since the motor model used does not account for magnetizing saturation, neither stator and rotor leakage saturation, nor distributed circuit effects in the rotor which affect current and torque ripple predictions [49]

4.6. Closing remarks
The value of the model developed in this chapter is the insight that it provides in the workings of power converter systems. The contributions of this model are: 1) preservation of common mode and differential mode within certain accuracy that are function of assumptions made, 2) simple formulation of the contribution of the front-end diode rectifier to the system voltage/current signature and 3) fast evaluation of effects of selected signature on the system that can be used for analysis of line-to-ground faults. The models developed in this chapter can be used in larger power systems that include power electronic components. They constitute an extension of other tools like symmetrical components that are commonly used in those systems.
5. COMPARISON BETWEEN POWER CONVERTER MODELS OF CHAPTER 4 AND DETAILED MODEL

In this chapter, the model proposed in Chapter 4 is compared back-to-back to a detailed model (i.e., a simulation model that includes power switches such as diodes and IGBT). Simulation setups are presented to follow. For all cases, voltages \( v_R, v_S \) and \( v_T \) form a 60 Hz 3-phase balanced set with amplitude 277.129 V. The motor is a 20 HP machine which parameters are given in Appendix B. The electric cable is a 300 m, 14 AWG which parameters are given in Appendix A. Other parameters used in the simulation are \( L_R=0.1 \) mH, \( r_R=1 \) m\( \Omega \), \( r_L=1 \) m\( \Omega \), \( L=1.41 \) mH, \( C=1260 \) \( \mu \)F, \( R_n=106 \) \( \Omega \), \( R_f=10 \) \( \Omega \).

The line-to-ground fault for all cases occurs right at the terminals of the motor. This scenario amplifies the effects of stray capacitances.

5.1. Simulation setups

5.1.1. Simulation Setup #1

In Fig. 5.1, the detailed model is depicted. The converter is a diode-rectifier and the inverter is a 6-switch IGBT bridge. The power switches utilized can be found in the Universal Bridge block of the Power Systems Toolbox of Simulink®. Snubber parameters for the switches are the ones by default.

![Diagram of Setup #1: Detailed model](image)

5.1.2. Simulation Setup #2

In Fig. 5.2, the proposed model for the converter is connected to the same inverter than in Setup #1. Notice that the DC-link capacitors have been replaced by DC voltage sources which have the effect of isolating the inverter. The \( CMV_{CONV} \) voltage source can easily be generated using the magnitude test utilized for modulators with adequate phase. The magnitude is scaled appropriately. By comparing voltages and currents sourced by this model.
set of waveforms correspond to the difference between the sum of the 3 output currents of Setup #1 and Setup #2.

![Diagram](image)

**Fig. 5.3. Setup #3: Proposed model of converter and inverter**

The inverter is operated at 30 Hz to limit FFT calculation error. The carrier frequency of the SVPWM modulator is 4000 Hz. The spectra are linear and the magnitude of the calculated harmonics is RMS. The spectra are normalized as percentage of the fundamental of the operating frequency of the inverter at 60 Hz (i.e., 28 A).

For the error between inverter output currents for Setup #1 and Setup #2, the fundamental illustrated is 30 Hz. The THD calculated for each spectrum is referred to this fundamental.

In Fig. 5.4, the waveform in time domain and corresponding spectrum for the error between output currents of Setup #1 and Setup #2 (non-faulted phase) before the occurrence of the line-to-ground fault are depicted. At 30 Hz, this error is 0.2564 A which is about 0.9% of the 1 p.u. base = 28 A. **Was the current at 1 p.u.?**

In Fig. 5.5, the waveform in time domain and corresponding spectrum for the error between output currents of Setup #1 and Setup #2 (non-faulted phase) after the occurrence of the line-to-ground fault are depicted. At 30 Hz, this error is 0.1827 A which is less than 0.7% of the 1 p.u. base = 28 A.
with voltages and currents corresponding to Setup #1, under constraints discussed in Chapter 4, the validity of Setup #2 is tested.

Fig. 5.2. Setup #2: Proposed model of the converter and detailed model of the inverter

5.1.3. Simulation Setup #3
In Fig. 5.3, the proposed models for the converter and inverter are utilized. The CMV\textsubscript{CONV} is the same as in Setup #3. The CMV\textsubscript{INV}, as discussed in Chapter 4 and in Appendix D is comprised of high-frequency and low-frequency (with high-frequency and low-frequency terms equally used as explained in Chapter 4). Though the whole spectrum could be reconstructed, the purpose of the modeled developed is to help study the effect of selected harmonic signature. Hence, for CMV\textsubscript{INV}, v\textsubscript{A}, v\textsubscript{B} an v\textsubscript{C} selected signature is chosen.

5.2. Comparison between simulation setups
In this section, the 3 setups presented are compared. First, Setup #1 and Setup #2 are compared. Then, Setup #1 and Setup #3 are compared.

5.2.1. Comparison between Setup #1 and Setup #2
Comparing Setup #1 and Setup #2 allows for quantification of the effect of commutation inductance and DC-link choke, as it was discussed in Chapter 4. The electric systems are discretized (T\textsubscript{s}=1 \mu s) and solved using the fixed-step ODE45 (Dormand-Prince) solver with a step size of 0.1 \mu s. The simulation is run up to t = 0.7 s. The line-to-ground fault is asserted at t=0.5 s.

The transient between t = 0 s and t = 0.3 s correspond to the charging of the DC-link capacitors (initial voltage V\textsubscript{C} = 339 V). Since the constraint for the model proposed is decoupling of the inverter side, the transient between t = 0 s and t = 0.3 s is non-transcendent for purpose of comparison between models.

A first set of waveforms correspond to the error between inverter output currents of Setup #1 and Setup #2. The spectra presented correspond to these waveforms before and after the occurrence of the fault (in red in corresponding time domain). Furthermore, 2 inverter output currents are analyzed corresponding to 1 non-faulted phase and the faulted phase. A second
Fig. 5.4: Non-faulted phase before fault: a) Error between output currents of Setup #1 and Setup #2, b) Spectrum for waveform in red

Fig. 5.5: Non-faulted phase after fault: a) Error between output currents of Setup #1 and Setup #2, b) Spectrum for waveform in red

In Fig. 5.6, the waveform in time domain and corresponding spectrum for the error between output currents of Setup #1 and Setup #2 (faulted phase) before the occurrence of
the line-to-ground fault are depicted. At 30 Hz, this error is 0.2578 A which is about 0.9% of the 1 p.u. base =28 A.

![Diagram](image)

**Fig. 5.6:** Faulted phase before fault: a) Error between output currents of Setup #1 and Setup #2, b) Spectrum for waveform in red

In Fig. 5.7, the waveform in time domain and corresponding spectrum for the error between output currents of Setup #1 and Setup #2 (faulted phase) after the occurrence of the line-to-ground fault are depicted. At 30 Hz, this error is 0.186 A which is about 0.6% of the 1 p.u. base =28 A. Notice that most of the error for this case is at the carrier frequency (less than 1.5%) and first harmonics of the carrier frequency. Notice, also, that there is about 1.3% error at the 16th harmonic of the carrier frequency.

In Fig. 5.8, the waveform in time domain and corresponding spectrum for the error between the sum of the 3 inverter output currents of Setup #1 and Setup #2 before the occurrence of the line-to-ground fault are depicted. At 4000 Hz (carrier), this error is 0.1399 A which is less than 0.5% of the 1 p.u. base =28 A. The energy of the error concentrates at the carrier frequency and harmonics of the carrier frequency. The largest calculated harmonic was at 20 KHz. The RMS value of such a harmonic was about 1.1% of the p.u. base.
In Fig. 5.9, the waveform in time domain and corresponding spectrum for the error between the sum of the 3 inverter output currents of Setup #1 and Setup #2 after the occurrence of the line-to-ground fault are depicted. At 4000 Hz (carrier), this error is 0.3984 A which is about 1.4% of the 1 p.u. base = 28 A. The energy of the error concentrates at the carrier frequency and harmonics of the carrier frequency. The largest calculated harmonic was at 20 KHz. The RMS value of such a harmonic was about 0.3% of the p.u. base.

5.2.2. Comparison between Simulation Setup #1 and Simulation Setup #3
The selected harmonic signature to be reconstructed for the inverter of Setup #3 is chosen to be the low-frequency CMV of the inverter (i.e., quasi-triangular CMV), carrier without sidebands and the fundamental of the inverter operating frequency. Then, harmonics reconstructed before the occurrence of the fault and after the occurrence of the fault are compared in tables 5.1-2.
Fig. 5.8: Sum of the 3 inverter output currents before fault: a) Error between the sum of 3 inverter output currents of Setup #1 and Setup #2, b) Spectrum for waveform in red

Table 5.1. Comparison of several harmonics of the sum of 3 inverter output currents of Setup #1 and Setup #2 before the occurrence of the fault: (D) stands for detailed model or Setup #1, (P) stands for proposed model or Setup #2

<table>
<thead>
<tr>
<th>f (Hz)</th>
<th>180</th>
<th>540</th>
<th>3640</th>
<th>4000</th>
<th>4180</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mag (D)</td>
<td>0.02</td>
<td>0.01</td>
<td>0.03</td>
<td>1.66</td>
<td>0.01</td>
</tr>
<tr>
<td>Mag (P)</td>
<td>0.02</td>
<td>0.01</td>
<td>0.01</td>
<td>1.53</td>
<td>0</td>
</tr>
<tr>
<td>Phase (D)</td>
<td>88.1</td>
<td>262.1</td>
<td>166.5</td>
<td>56.6</td>
<td>59.6</td>
</tr>
<tr>
<td>Phase (P)</td>
<td>88.4</td>
<td>265.8</td>
<td>0</td>
<td>61.3</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 5.2. Comparison of Sum of several harmonics of the 3 inverter output currents of Setup #1 and Setup #2 after the occurrence of the fault: (D) stands for detailed model or Setup #1, (P) stands for proposed model or Setup #2

<table>
<thead>
<tr>
<th>f (Hz)</th>
<th>30</th>
<th>90</th>
<th>180</th>
<th>270</th>
<th>450</th>
<th>540</th>
<th>630</th>
<th>900</th>
<th>1260</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mag (D)</td>
<td>1.69</td>
<td>0.35</td>
<td>0.69</td>
<td>0.03</td>
<td>0.01</td>
<td>0.07</td>
<td>0.01</td>
<td>0.02</td>
<td>0.01</td>
</tr>
<tr>
<td>Mag (P)</td>
<td>1.68</td>
<td>0.35</td>
<td>0.7</td>
<td>0.03</td>
<td>0.01</td>
<td>0.07</td>
<td>0.01</td>
<td>0.02</td>
<td>179.7</td>
</tr>
<tr>
<td>Phase (D)</td>
<td>120.6</td>
<td>179.7</td>
<td>179.7</td>
<td>180.7</td>
<td>179.9</td>
<td>179.4</td>
<td>182.7</td>
<td>178.5</td>
<td>0.01</td>
</tr>
<tr>
<td>Phase (P)</td>
<td>120.5</td>
<td>179.9</td>
<td>179.7</td>
<td>179.5</td>
<td>179.4</td>
<td>179.1</td>
<td>178.7</td>
<td>179.5</td>
<td>178.1</td>
</tr>
<tr>
<td>f (Hz)</td>
<td>3700</td>
<td>3760</td>
<td>3820</td>
<td>3880</td>
<td>3940</td>
<td>4000</td>
<td>4060</td>
<td>4180</td>
<td>4240</td>
</tr>
<tr>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>Mag (D)</td>
<td>0.01</td>
<td>0.02</td>
<td>0.02</td>
<td>0.16</td>
<td>0.22</td>
<td>2.91</td>
<td>0.22</td>
<td>0.02</td>
<td>0.02</td>
</tr>
<tr>
<td>Mag (P)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2.87</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Phase (D)</td>
<td>48.9</td>
<td>109.5</td>
<td>-9.9</td>
<td>229.4</td>
<td>109.1</td>
<td>-8</td>
<td>228.8</td>
<td>-10</td>
<td>219.4</td>
</tr>
<tr>
<td>Phase (P)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-6.6</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Fig. 5.9: Sum of the 3 inverter output currents after fault: a) Error between the sum of 3 inverter output currents of Setup #1 and Setup #2, b) Spectrum for waveform in red

The closeness between magnitude and phase of Setup #1 and Setup #3 indicates that the proposed model that separates common mode and differential mode can be used to quantify the effect of a line-to-ground fault on the inverter-side of a converter-inverter system.

Again, my main complaint is that your committee will want to see model predictions, not just the difference between the predictions.
6. SETTING THRESHOLD

Independent of the method to be used to detect the occurrence of a line-to-ground fault on the inverter-side of an IPCS that could be comprised of several ASDs, there is a need to establish a voltage/current threshold that would be used to compare measured voltage/current signature to. In this chapter, the problem of determining such a voltage/current threshold is addressed.

The specialized technical literature only discusses a method to determine a current threshold for the current measured through the HRG resistor, $R_m$, based on the appropriate sizing of the resistor $R_m$ for HRG systems with sine-wave voltage sources [12]. This method is briefly discussed in this chapter as it will be extended to accommodate sources that include PWM switching events.

The scope of the research made for this chapter is limited to the case in which the mains is a balanced set of voltage sources; and the operating frequency of the inverter can be commanded in the interval from 0 Hz – 400 Hz. Considerations and terminology used for this chapter are:

- Due to switching losses and Electro-Magnetic Interference (EMI) considerations the switching frequency of the IGBT is chosen to be within 1.6 kHz – 20 kHz and the rise time of the PWM pulses is assumed to be at least 200 ns. This is only a reference.
- The modulator used in this chapter is the SVPWM as described in Chapter 2
- Terms low-frequency and high-frequency are utilized somewhat loosely. As discussed briefly in the previous chapter, the term low-frequency refers to the spectrum of the converter CMV, $LFCMV_{CONV}$, and to the spectrum of the modulating signal of the inverter, $LFCMV_{INV}$. The term high-frequency refers mainly to the carrier band of interest ($CMV_{INV}$ without the frequency content of $LFCMV_{INV}$), unless otherwise indicated.
- The terms converter CMV, or CMV of the converter refer only to that part of the total CMV that is sourced by the converter. The term inverter CMV, or CMV of the inverter, refer only to that part of the total CMV that is sourced by the inverter. Finally, the terms CMV, or converter-inverter CMV, or diode-rectifier-inverter system CMV refer to the CMV sourced by converter and inverter.

The outline of this chapter is as follows: First, a brief discussion about the existing method to determine a current threshold on an HRG system with sine-wave voltage sources is done. Second, the method discussed in the first part of this chapter is extended to HRG systems with PWM voltage sources. Third, a threshold for selected voltage/current signature is calculated.
6.1. HRG systems on sine-wave voltage sources

Abundant literature [50]-[69] has been written on HRG system design and application characteristics for sine-wave sources. Findings have been formalized in ANSI/IEEE standards, National Electric Code (NEC) articles, Underwriters Lab (UL) and Canadian Standards Association (CSA) standards.

Guidelines for selecting $R_n$, ground fault relays and protective coordination are found in ANSI/IEEE standards [70]-[74]. NEC 2008 Code Article 250.20(E) permits use of HRG neutral systems for low and medium voltage while Section 250.36 sets down requirements for use and installation on low voltage systems. IEEE-32 standard [75] contains specifications for manufacture of $R_n$, as well as zig-zag grounding transformer if used, further citing UL and CSA for permissible $R_n$ temperature rise under short time and continuous duty cycle.

Insulation selection guidelines [76]-[77] imply thickness requirements by defining % of insulation levels as time to clear the line-to-ground fault. In [78] and in [79] the number of years in service is calculated based on the peak sine-wave voltage.

The aim of this section is to specify $R_n$. It implies estimating the current that circulates through $R_n$, which is a current threshold for HRG systems with sine-wave voltage sources.

6.1.1. Determining cable charging current

To achieve the benefits of high-resistance grounding for systems with sine-wave voltage sources, the level of system ground-fault current must be equal to or greater than the system capacitance charging current. When an AC voltage is applied to conductors, small current flows to ground through capacitance as depicted in Fig. 6.1. For a balanced 3-phase system, the capacitance charging currents of the 3 phases are equal and displaced from each other by 120 degrees. The currents of the 3 phases thus add to zero. Fig. 6.2 illustrates the phasors for this balanced system. However, when a ground fault occurs on a system, things change as it is depicted in Figs. 6.3-4. First, on the grounded phase, the ground shorts out the capacitance and no charging current flows in that phase. Second, the voltage to ground on the ungrounded phases increases by $\sqrt{3}$; thus, the charging current of these 2 phases also increases by $\sqrt{3}$. Finally, the 2 remaining capacitive charging currents are no longer at 120° angle to each other, but at 60°. When the phasors representing these 2 currents are added vectorially, the resulting total system charging current is $\sqrt{3}$ times each of the 2 currents, or 3 times the original per-phase system charging current of the unfaulted system. In Fig. 6.5, this condition is depicted.

6.1.2. Selection of $R_n$

The selection of $R_n$ depends on the parasitic capacitance $X_{c0}$ to ground with a criterion to minimize over-voltage during ground fault [65]. The fault current through $R_n$, from Fig. 6.5,
is made larger than the maximum capacitive charging current $3i_{c0}$ to avoid neutral over-voltage resonances as explained later in this section. Substituting $I_{Rn} = V_{in}/R_n$ and $I_{c0} = V_{in}/X_{c0}$ the impedance criteria is obtained [79] as presented in (6.1).

$$|I_{Rn}| \geq 3|I_{c0}| \quad R_n \leq X_{c0}/3$$  \hspace{1cm} (6.1)

---

**Fig. 6.1.** HRG system voltage and charging current during normal non-fault operation

**Fig. 6.2.** Normal non-fault operation

The value of $R_n$ must be low enough to allow enough current to flow such that it can be detected. Higher values of $R_n$, however, imply less damage or no damage to the core of the faulted motor. Charging current $3i_{c0}$ is calculated under conditions previous to the occurrence of a line-to-ground fault. The assumption made is that the impedance on which $\sqrt{3} V_{in}$ is applied is largely dominated by the impedance of the parasitic capacitance [55], [57]. This is a rather conservative approach whose effect is the specification of a higher threshold. Depending on the cable size and insulation characteristics, current normalized by the length...
of the cable and the size of the motor has been calculated as in [57] and condensed in Table 6.1. For low-voltage systems, such a threshold is usually found to be < 1 A [57] under conditions previous to the occurrence of a line-to-ground fault. Thus, $R_n$ is usually specified to provide $i_{RN}$ between 1 A and 5 A and to have well damped resonances. This definition of threshold current is for the RMS value of the current, which occurs at fundamental frequency for HRG systems with sine-wave voltage sources. To follow a the brief description of methods found in the literature to calculate $R_n$ are presented.

Fig. 6.3. HRG system voltage and charging current during Phase A line-to-ground fault

Fig. 6.4. Phase A line-to-ground fault condition voltages $V_{AB}=V_B-V_A$, $V_{CA}=V_C-V_A$
Fig. 6.5. Phase A line-to-ground fault currents

The method based on the current condition of (6.1) is depicted. For the case which is portrayed $|U_{Rn}| = 3|I_{cd}| = \sqrt{2}$ A is the limit current condition. Points to the right of the vertical line, as $|U_{Rn}|$ becomes larger than $3|I_{cd}|$, comprises well-damped HRG designs. Points to the left of the vertical line comprises designs that approach ungrounded systems behavior.

In Fig. 6.6, the method based on the current condition of (6.1) is depicted. For the case which is portrayed $|U_{Rn}| = 3|I_{cd}| = \sqrt{2}$ A is the limit current condition. Points to the right of the vertical line, as $|U_{Rn}|$ becomes larger than $3|I_{cd}|$, comprises well-damped HRG designs. Points to the left of the vertical line comprises designs that approach ungrounded systems behavior.

![Diagram showing current conditions](image)

Fig. 6.6. Current condition of (6.1) [65]

<table>
<thead>
<tr>
<th>Equipment description</th>
<th>Current per unit length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cables</td>
<td></td>
</tr>
<tr>
<td>350 to 500 MCM in conduit</td>
<td>0.10 A/1000 ft of 3-wire cable</td>
</tr>
<tr>
<td>2.0 to 3.0 AWG in conduit</td>
<td>0.05 A/1000 ft of 3-wire cable</td>
</tr>
<tr>
<td>2.0 to 3.0 AWG in tray</td>
<td>0.02 A/1000 ft of 3-wire cable</td>
</tr>
<tr>
<td>6 AWG 3-wire with ground wires</td>
<td>0.05 A/1000 ft of 3-wire cable</td>
</tr>
<tr>
<td>Motors</td>
<td>0.01 A/1000 HP</td>
</tr>
</tbody>
</table>

In Table 6.1, data for estimating charging current in 480 V systems are shown.
In Fig. 6.7, the method based on the impedance condition of (6.1) is depicted. For the case which is portrayed $R_n = 3X_{c0}$ generates a peak for the line-to-ground voltage 2.6 times larger than the rated line-to-neutral peak voltage which implies resonances in the series circuit comprised of parasitic capacitance, series inductance (transformer, motor winding) and HRG $R_n$.

Another way to visualize the effect of the resonance for not well-damped HRG systems is given in [65] and shown in Fig. 6.8. The line-to-ground voltage as percentage of the nominal line-to-neutral voltage is plotted versus the ratio of inductive and capacitive reactance for different values of the current through ground resistance. For this particular case, a 350% over-voltage for $|I_{Rn}| = 0.63$ A is calculated. If $|I_{Rn}| = 6.5$ A, the resulting line-to-ground voltage is 180% of the nominal line-to-neutral voltage $V_{ln}$, and close to the minimum possible value of $\sqrt{3} \times 100\%$ of the nominal line-to-neutral voltage.

Finally, the preferred method of the author of this dissertation is shown in Fig. 6.9 [12]. It is assumed that the line-to-ground fault path is inductive which results in a more severe line-to-ground fault (i.e., major risk for line-to-ground overvoltage). The inductive path, for instance, cable inductance and/or stator inductance. The x-axis in Fig. 6.9 represents the inductive impedance. The resonant circuit formed by inductance and parasitic capacitance creates resonances such that the amplitude of the voltage across $R_n$ takes values depicted in Fig. 6.9. Values for $R_n$ between 111 $\Omega$ – 333 $\Omega$ translate in well damped resonances. In 480 V low-voltage systems, for $R_n = 111$ $\Omega$, $|I_{Rn}| = 2.5$ A and for $R_n = 333$ $\Omega$, $|I_{Rn}| = 0.8$ A. Thus,
typical $I_{R_n}$ values are selected between 1 A to 5 A. The advantage of this method is that a large range of values for the inductive part is considered; therefore, it is not as critical to analyze ground fault resonance over-voltages on every system.

![Image](image_url)

Fig. 6.8. Percentage of nominal voltage

### 6.1.3. Maximum voltage stress on insulation

The value of $R_n$ should be determined considering the maximum allowable stress on the electric cable and motor insulation as well as the maximum removal time duration during persistent line-to-ground fault condition. In [57], an early study performed in the late 70s of different cable insulations and rules of thumb for the duration a line-to-ground fault should be permitted are discussed. In the mid 80s to mid 90s, insulation evaluation standards incorporating multifactor thermal and voltage stress testing under line-to-ground faults were proposed. These have been mostly withdrawn or considered obsolete. In [79], a line-to-ground fault survival of a 300 HP, 600 V, 449 T frame random wound motor having Class B temperature rise with Class F insulation materials was investigated for 3 motor failure mechanisms: 1) immediate insulation breakdown of motor materials, 2) short term Corona Inception Voltage (CIV) failure mechanism and 3) long term dielectric aging under voltage-thermal stress. The conclusion of such a study was that the closer the line-to-ground voltage can be controlled to the minimum over-voltage $\sqrt{3} V_{in}$, the greater the chance of the ensuring motor insulation material’s long term survival. This criterion will be the one considered in
the next section when extending the existing HRG guidelines for systems on sine-wave voltage sources to HRG systems on PWM voltage sources.

![Resonances in an inductive-path line-to-ground fault](image)

**Fig. 6.9.** Resonances in an inductive-path line-to-ground fault

### 6.2. HRG systems on PWM voltage sources

In this section, the guidelines provided for HRG systems with sine-wave voltage sources presented in the previous section are extended to HRG systems with PWM voltage sources. In particular, the objective is to verify that the value for $R_n$ recommended for HRG systems with sine-wave voltage sources is applicable for the case of HRG systems with PWM voltage sources. Using this value for $R_n$, a voltage/current threshold will be established for a specific harmonic of the sum of the 3 line currents. Which harmonic is used is also determined in this section.

This section is organized as follows: First, using cable and motor models presented in Chapter 2 together and the design guidelines for $R_n$ from the previous section, a range for the value of $R_n$ for HRG systems on PWM voltage sources is determined. Second, three possible definitions of threshold are discussed: 1) true RMS based, 2) level based, 3) specific harmonic level based. A preference for option 3) is shown. Third, a threshold for a specific harmonic of the current flowing to ground/voltage-to-ground is calculated and results from experimental implementation are presented to back calculations. Fourth, a simple and practical method to calculate the threshold is introduced. The method is backed with experimental results which are thoroughly discussed.

#### 6.2.1. Calculation of $R_n$

The major challenge herein is to encompass effects within a broad range of harmonic components. Only simulation tools will be used to facilitate the analysis. The system
depicted in the previous chapter in Fig. 4.23, and repeated for convenience in Fig. 6.9, is used to calculate the adequate range of values of $R_n$. Since $R_n$ will be determined for the spectrum content defined in Chapter 2 (1.6 MHz) of the inverter, voltage sources $v_{W0,INV}$, $v_{V0,INV}$, $v_{w0,INV}$ can be replaced by the detailed (switches-based) model of the inverter.

Initially, the line-to-ground fault path given by $R_f$ is restricted to be purely resistive and a range of values between 0 $\Omega$ and 100 $\Omega$ is assumed. This range encompasses, for instance, cases like a line-to-ground fault through 1 strand of the copper in one phase or a steel tool accidentally placed between a phase and ground. The line-to-ground fault occurs in phase C.

Two simulation cases are examined using Test-bed 1: 1) 300 m of 14 AWG 4-wire symmetric cable as described in Chapter 2 with parameters given in Appendix A. A 4 KW (5 HP) motor described in Chapter 2. Motor parameters are given in Appendix B and 2) 300 m of 2 AWG 4-wire symmetric cable as described in Chapter 2 with parameters given in Appendix A. A 45 KW (60 HP) motor as described in Chapter 2 with parameters given in Appendix B. The line-to-ground fault occurs right at the terminals of the motor.

From the recommendation for HRG systems with sine-wave sources, the range of values of $R_n$ is within the 100 $\Omega$ - 300 $\Omega$ range. In the setup corresponding to the first simulation case, a line-to-ground fault was asserted at $t = 0.1$ s. The non-faulted phase-to-ground voltage $V_{ag}$ is depicted for $R_n = \{100, 200, 300\}$ $\Omega$. It is observed from Fig. 6.10 that the larger the value of the resistance $R_n$, the less damped the non-faulted phase-to-ground voltage $V_{ag}$ appears.

![Graph showing non-faulted phase-to-ground voltage $V_{ag}$ for different values of $R_n$.](image)

**Fig. 6.10.** Non-faulted phase-to-ground voltage $V_{ag}$ for setup comprised of 300 m of 14 AWG cable and 4 KW motor

The maximum stress voltage on insulation criterion discussed in the previous section established the need for keeping $V_{ag}$ as close as possible to a value of $\sqrt{3} V_n$. To follow, this is analyzed. The first step is to verify if the maximum stress voltage on insulation criterion can be satisfied instantaneously. In Figs. 6.11-12, peaks of non-faulted phase-to-ground
voltages $V_{ag}$ for both simulation setups, as $R_n$ and $R_f$ are varied during the occurrence of a line-to-ground fault are depicted. $R_n$ is varied in the range of $[0 - 120] \, \Omega$. It is observed that the most severe fault scenario occurs for values of $R_f = 0 \, \Omega$ as shown in the projections of non-faulted phase-to-ground voltage $V_{ag}$ vs. $R_n$ (6.11b, 6.12b). Furthermore, it is observed that the smaller $R_n$ becomes, the smaller the peaks of voltage $V_{ag}$ are. Therefore, the maximum stress voltage on insulation criterion can only be satisfied for small values of $R_n$ (i.e., less than 20 $\Omega$ or so). Though, such smaller values of $R_n$ are feasible for large size ASDs, smaller size ASDs require the fault current be limited to much smaller values to ensure continuous operation.

![Graph showing $V_{ag}$ peak voltage vs. $R_f$ and $R_n$ for 14 AWG cable and 4 KW motor setup](image)

Fig. 6.11. Non-faulted phase-to-ground voltage $V_{ag}$ vs. $R_n$ and $R_f$ for 14 AWG cable and 4 KW motor setup: a) 3-D, b) projection

The next step is to verify if the maximum stress voltage on insulation criterion can be satisfied for the RMS value of the non-faulted phase-to-ground voltage $V_{ag}$ during the occurrence of a line-to-ground fault. The RMS value calculated for the current through the line-to-ground fault path is depicted in Fig. 6.13 for the second simulation setup. In Figs. 6.14.a)-c), RMS calculated values for $V_{ag}$, $V_{bg}$ and $V_{cg}$, respectively are depicted.

Notice that only for values of $R_n$ smaller than 1 $\Omega$ and bolted line-to-ground fault is the maximum stress voltage on insulation criterion satisfied. However, observe that only very large ASDs would handle this RMS current through $R_n$. From observations made for instantaneous and RMS phase-to-ground voltages and RMS current through the fault path, it is recommended to make $R_n$ as small as possible. Establishing such a value should consider
the current that the ASD could handle without tripping in over-current mode. If possible, values for $R_n$ in the range of $40 \Omega - 60 \Omega$ should be preferred.

![Graph](image)

**Fig. 6.12.** Non-faulted phase-to-ground voltage $V_{ag}$ vs. $R_n$ and $R_f$ for 2_0 gauge cable and 45 KW motor setup: a) 3-D, b) projection

![Graph](image)

**Fig. 6.13.** RMS value of current through the line-to-ground fault path

### 6.2.2. About the threshold for HRG systems with PWM voltage sources

From the system depicted in Fig. 4.23, and repeated for convenience in Fig. 6.15, a threshold is discussed. The assumptions made for this system are that the converter side is a diode-rectifier front-end with symmetrical voltage sources and electric cables; the commutation
interval is negligible; there is always diode conduction; there is effective isolation between grid and load; and the cable and load are symmetrical. Under these assumptions, the converter can be represented by a CMV source which is similar (not in magnitude), except possibly for the phase, to the inverter low-frequency CMV. The electric cable and motor, as discussed in Chapter 2, have capacitive coupling to ground. Therefore, the current through the fault path is equal to the vector sum of the current through the resistance $R_n$ and the current through parasitic capacitances.

![RMS value of $V_{sg}$](image1)

Fig. 6.14.a) RMS value of non-faulted phase-to-ground voltage $V_{sg}$

![RMS value of $V_{bg}$](image2)

Fig. 6.14.b) RMS value of non-faulted phase-to-ground voltage $V_{bg}$