Orthogonal Filter Frequency Followed by LNA Linearity Tuning for Efficient Instinctual GaN Receiver Front-End

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***Abstract*— This work presents an interference-adaptive Gallium Nitride (GaN) low-noise amplifier (LNA) front-end with orthogonal frequency and linearity tuning for applications in communication base stations, radar and electronic warfare (EW). The system operates between 2-6 GHz and provides a sub 5 ms tuning time for an input power tuning range of 40 dB. The orthogonal tuning consists of two phases: 1. frequency tuning with four tunable bandpass and bandstop filters for interference rejection, 2. linearity tuning with a combination of coarse tuning through look-up table (LUT) and fine-tuning through incremental adaptation to trade off power with linearity. GaN LNA's linearity can be adjusted between $P_{1dB,IN}$ = -10 and 1.5 dBm with output P_{1dB} up to 25 dBm (11.5 dB range) with the LNA power changing from 500 mW to 2 W (x4 increase). The average LNA power with orthogonal frequency and linearity tuning decreases by 56% as compared with the system operating at the worst-case no tuning condition. Two systems involving commercial filters and custom cavity resonator-based filters were constructed. The filters further increase the system $P_{1dB,IN}$ by the filter rejection of the interference signal. The rest of the controls consume about 10% of the worst-case condition LNA power.**

***Index Terms*— GaN LNA, interference-adaptive, orthogonal frequency and linearity tuning.**

I. Introduction

AS THE technologies progress, the frequency spectrum becomes more saturated, and more devices are operating at the same time, such as in the fields of communication, radar, and electronic warfare (EW). In such fields, unintentional interferences due to the nearby devices are becoming more prevalent to saturate the receiver which requires the receivers to have high power handling capabilities and high linearity requirements. Without high power handling capabilities, RF limiter is often added to save the components under the stress of high input power which adds additional loss and noise figure (NF). Contrary to RF limiters, GaN LNAs have been widely researched to have higher power handling than GaAs and CMOS LNAs due to the inherent nature of higher bandgap [1]. Further, GaN LNAs provide higher linearity for a better chance of recovering the signal with the presence of a blocker.

To minimize the saturation caused by the unwanted interference, many receivers are designed to operate at the worst-case condition to minimize saturation at the cost of high power consumption [2]. In the cases of radar arrays, high power consumption often translates to a substantial amount of cooling. One of the solutions to alleviate excessive power consumption is to incorporate a tunable receiver that can reject interferences and adapt to different input levels.

Traditional front-end architecture rejects interference through bands of fixed BPF which are high cost as shown in Fig. 1(a) [3]. While the filters provide considerable rejection, blockers can still leak through and saturate the LNA. Other adaptive front-ends with interference rejection are shown in Fig. 1(b)-(d). Fig. 1(b) shows the maximum interference detector consisting a feedforward loop to detect the reference frequency and tune the bandstop filter (BSF) through a field programmable gate array (FPGA) [4], [5]. The interference

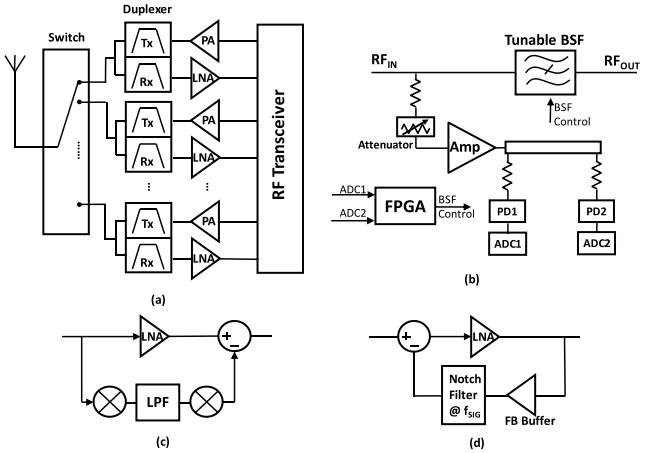

Fig. 1. (a) Traditional front-end architecture. (b) Max interference detector. (c) Feedforward interference rejection. (d) Feedback interference rejection.

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frequency is detected by creating a unique ratio from the measurements of two points on the standing wave pattern on an open-circuit stub for different frequencies. Since no feedback network is present, an incorrect filter tuning will not be able to be corrected. Moreover, the MID can only detect one large interference signal, further detection for other interference signals can be implemented by cascading more MID which increases the complexity of tuning, area and power consumption. Fig. 1(c) shows the feedforward technique for interference cancellation by replicating the interferences and subtracting at the output of the LNA [6]. This method does not reduce the interference at the input node, thus LNA may still be saturated. Since the feedforward path also sees the interference signal, the components in the feedforward path also require high linearity and high power handling. Fig. 1(d) shows the feedback technique for interference cancellation by feeding back the interference at the input node. This method reduces the interference at the input node which helps with LNA's input linearity; however, the amplified input signal will need to pass both the buffer and the notch filter which require even higher linearity and power handling. Both feedforward and feedback techniques may also incur significant power consumption on the loop.

Many of the works focus on providing tunability to different components. References [7], [8], and [9] provides different kinds of tunable filters such as multiband bandpass filter (BPF) and bandstop filter (BSF), BPF with out-of-band BSF, and BPF with in-band BSF respectively. Another work in [4] presents an interference detector to engage the tunable band-stop filter at the interference frequency. References [10], [11], [12], and [13] presents different ways of tuning the gain and linearity of the LNA. References [14], [15], [16], and [17] presents different power detectors across a wide range of frequencies with relatively low power. The above works demonstrate the possibility of tunable components being involved in an RF receiver system; however, a complete system-level implementation combining sensing, tuning, and closed-loop control demonstrating fast-time tuning is missing from the literature.

Some adaptive systems have been simulated in works [18], [19]. Additional works are focused on forming useful algorithms to tune the front end to work in a minimum power consumption mode for a tolerable performance in different channel conditions [20], [21]. These works are mainly simulation-based. Another work focused on creating a tunable transmitter depending on different path loss and receiver performances through actor-critical neuro-controller [22]; however, the receiver is not tunable. Other related works can be found in [23], [24], [25], and [26].

Many of the tunable Rx integrated circuit (IC) works are operating in a narrower frequency range with the help of N-path filters and do not involve high power handling components [27]. This paper aims to provide a wide-band tunable GaN receiver front-end with complete system-level demonstration to show the capability of fast real-time adaptation in the 2-6 GHz range with minimal increase in control power. Fig. 2 shows the proposed work with orthogonal frequency and linearity tuning. This work alleviates the effect of interference in the system first by interference detection and rejection through frequency tuning, next through the linearity and power tradeoff of the GaN LNA.

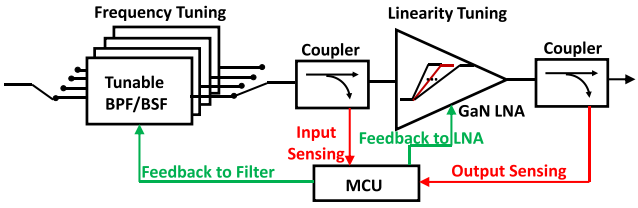

Fig. 2. Proposed work through three stages: (1) sensing from the input and output, (2) processing through the MCU and (3) feedback to filter-frequency tuning and feedback to the LNA-linearity tuning.

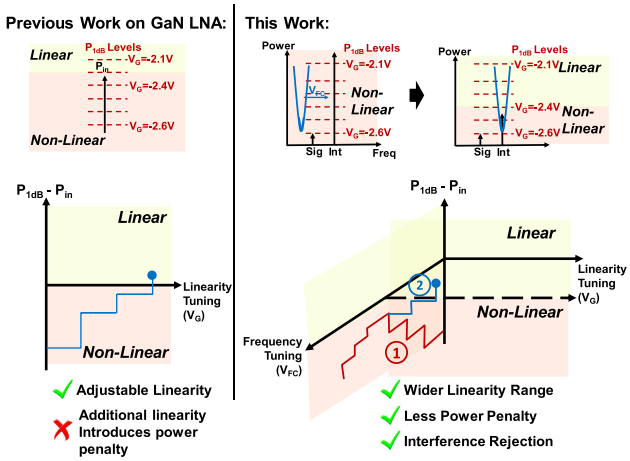

Fig. 3. Previous work on adaptive GaN LNA [28], [29] shows only one degree of tuning (linearity tuning) at which power is at the trade-off. This work builds upon the previous work and introduces a second degree of tuning. The orthogonal frequency and linearity tuning presents a way to improve linearity without any power increase or less increase than it is in previous work.

A. Proposed Solution

As shown in Fig. 3, our previous work presents interference adaptive RX based on the LNA linearity and power consumption trade-off [28], [29]; however, without any frequency tuning to minimize the interference, the adaptation range is significantly limited. This work further involves orthogonal frequency and linearity tuning to the interference adaptive front-end. Instead of directly trading power with linearity, this work first performs frequency tuning to reject the interference with no penalty on the LNA power. If frequency tuning is insufficient to bring the receiver out of saturation, linearity tuning is then used to increase the linearity of the LNA at the cost of power, note that the amount of power needed would be much less than if only linearity tuning were used.

This work adds the following contributions:

- This work implements **orthogonal frequency and linearity tuning** in a 2-6 GHz interference-adaptive GaN LNA front-end that incorporates 1) **sensing** through two degrees of observability and tunable filter for frequency information without a spectrum analyzer, 2) **processing** using onboard microcontroller with the goals of minimizing GaN LNA power consumption and fast tuning time, 3) **feedback** to the LNA for linearity tuning and the filters for frequency tuning. Overall, the system achieves sub 5 ms of tuning time with a discrete implementation that

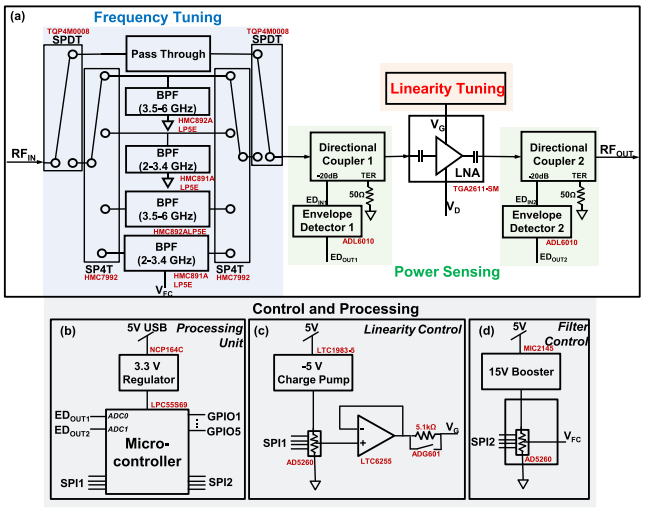

Fig. 4. (a) System architecture of the RF path with the commercial filters. (b) Microcontroller processing unit. (c) Linearity control schematic. (d) Filter control schematic.

can be reduced further with on-chip implementation. The system provides a wide input RF power tuning range of 40 dB and an average LNA power decreased by 56% from the worst-case condition.

- This work presents two RF front-end implementing the commercial filters and the customized filters along with all of the controls and processing units on board.
- System tuning algorithm is formulated to minimize both the tuning time and GaN LNA power consumption.
- System timing is analyzed for the commercial filter front-end implementation to provide an understanding of future improvements.

The paper is organized as follows: Sec. II provides an overview of the control loops and component characterization; Sec. III investigates different design considerations such as the design of directional coupler, frequency and linearity tuning controls; Sec. IV describes control algorithm for different tuning and timing analysis for the front-end with commercial filters; Sec. V presents the measurement results; Sec. VI presents the future directions of this work and Sec. VII concludes the paper.

II. Hardware Description and Characterization

A. RF Front-End With COTS Filters

Fig. 4 shows the overall system architecture constructed on a printed circuit board (PCB) with commercial off-the-shelf (COTS) components listed in Table I. The RF components are chosen to be 50 Ω matched, and capable of high power handling. The microcontroller is chosen to have a high-resolution analog-to-digital converter (ADC) and sufficient general-purpose input/output (GPIO) pins. The board is roughly made up of four sections: 1. the filters, 2. the sensing elements, 3. the gain stage, and 4. the controls. The filters, directional coupler and the GaN LNA establish the front-end of the system. As shown in Fig. 4(a), the filters section performs frequency tuning with five paths: pass-through, higher frequency tunable BSF, lower frequency tunable BSF, higher frequency tunable BPF, and lower frequency tunable BPF. The BSF are constructed by shunting the BPF to the ground.

TABLE I
Component Specifications

Component	Part Number	Specifications
GaN LNA	TGA2611-SM [32]	2-6GHz, 1dB NF, 22 dB Gain, -4dBm $P_{1dB,IN}$
2-3.4 GHz BPF	HMC891 [33]	50Ω matched, 200ns t_{settle}, 0-14V tuning, IL=8dB, RFin,max=27dBm
3.45-6 GHz BPF	HMC892 [34]	50Ω matched, 200ns tsettle, 0-14V tuning, IL=9.5dB, RFin,max=27dBm
Envelope Detector	ADL6010 [35]	0.5-43.5GHz, 47us trise, 1.6mA 0.01V-3V Vout, 50Ω matched P_{IN}=-30∼15dBm
SPDT Switch	TQP4M0008 [36]	0.1-6 GHz, $P_{IN,MAX}$=33dBm, IL<1dB, Isolation>26dB
SP4T Switch	HMC7992 [37]	0.1-6 GHz, $P_{IN,MAX}$=33dBm, IL<1.5dB, Isolation>30dB
Micro -controller	LPC55S69 [38]	16 bit ADC, 1MHz $f_{sample(ADC)}$ 150MHz f_{CLK}, 64 GPIO, 10 single-ended ADC

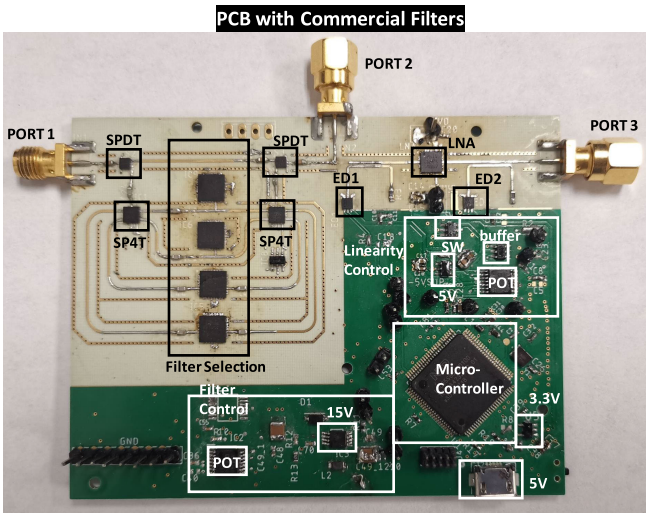

Fig. 5. Board diagram with the commercial filters. Black rectangles are components in the RF path, white rectangles are components in the control and processing unit.

The sensing elements form two observability points at the input and output of the gain stage with directional coupler and envelope detector pairs. The directional couplers employ 20 dB coupling to a U-shape trace with one side connecting to the envelope detector and the other to a 50 Ω termination. The gain stage involves a GaN LNA which by adjusting the gate bias, the linearity can be improved with higher power consumption. Lastly, the controls involve a microcontroller to perform decision-making for frequency and linearity tuning. The linearity tuning architecture has a -5 V inverting charge pump, potentiometer, op-amp, and switch-resistor parallel pair which is custom designed to compensate for the high power effects of the GaN LNA. The filter tuning architecture has a 15 V boost converter along with a potentiometer to control the filter frequency tuning voltage from 0-14 V. Further details on the controls will be discussed on Sec. III.

1) PCB Layout: The PCB is shown in Fig. 5. The system is designed on a four-layer PCB with Rogers 4350 dielectric.

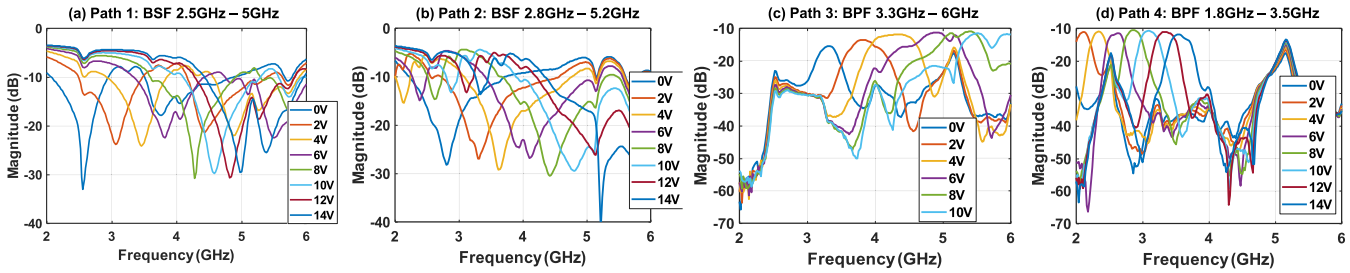

Fig. 6. S21 characteristics with different control voltages for (a) path 1 BSF, (b) path 2 BSF, (c) path 3 BPF, (d) path 4 BPF.

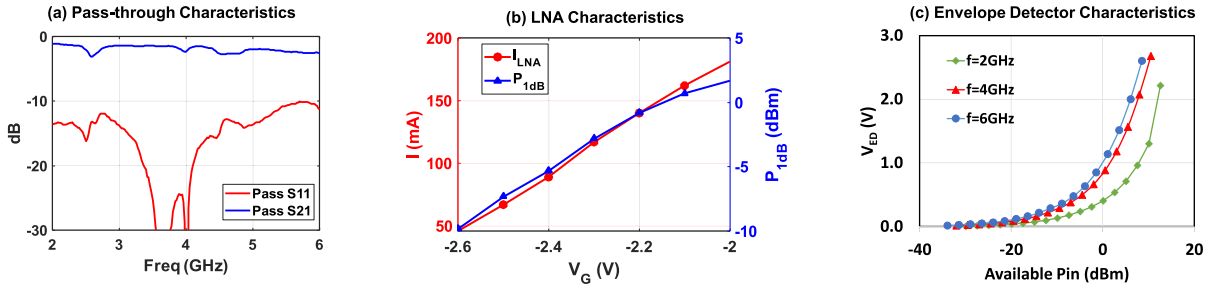

Fig. 7. (a) Pass-through path S11 and S21 characteristics. (b) GaN LNA characteristics when input is at 3 GHz, VD = 10 V. (c) Envelope detector output voltage with respect to available input power at different frequencies.

The first layer has all the RF traces and the control system; the second layer is dedicated as the RF ground plane; the third and fourth layers are used for routing for the control system. The RF traces are calibrated to 50 Ω with the dielectric thickness being 0.254 mm between the first and second layers. Additionally, the RF traces are mostly straight or curved to minimize insertion loss and reflection [30]. The solder mask on top of the RF traces is removed to avoid extra dielectric loss. To avoid undesired coupling, via fences between the traces are added to reduce radiation and coupling [31]. The decoupling capacitors required by the switches are chosen to have low loss and high Q.

2) Component Characterization: Since the filters are being placed parallelly, switches become necessary for different configurations. The frequency responses of the pass-through path and the filter tuning paths are measured using Vector Network Analyzer (VNA) from port 1 to port 2. Filter characterizations with different bias voltages are shown in Fig. 6. To simplify the algorithm, the bias voltages for the filters are quantized to integer voltages. As the tuning voltage increases, the center frequency also increases. Note that the passband losses for the BSFs (5∼10 dB) are lower than the BPFs (∼10 dB). There are some unintended notches mostly due to the additional reflections from the switches. The BSF frequencies are not the same as the BPF because the BPFs are not designed to function as BSF, so along with the switches, decoupling capacitors, and the stub connecting to the input of the filter, the BSF frequency is altered to be roughly around 2.5 GHz to 5.2 GHz for both BSF.

The initial pass-through characteristics are shown in Fig. 7(a). Instead of a smoothly increasing insertion loss with frequency, the response shows some more small notches such as ones at 2.7 GHz and 4 GHz due to the switches which are also apparent in the filter response. The overall insertion loss (S21) is less than 3 dB and return loss (S11) less than -10 dB. Fig. 7(b) shows LNA characteristics with both power and linearity (P_{1dB}) being strong functions of gate voltage (V_G). As V_G increases from -2.6 V to -2 V, GaN LNA power increases from 50 mA to 200 mA (4x) and linearity increases from -10 to 1.5 dBm (11.5 dB). Fig. 7(c) shows an exponential relationship between the input envelope detector (ED) power and the output DC voltage. The difference in the different frequency responses can be minimized through incremental adaptation during tuning [29].

B. Front-End With Customized Filter

Fig. 8 shows another RF front-end implemented with a customized BSF filter. Fig. 8(a) shows the board diagram with the customized filter. The customized BSF filter utilizes the idea of cavity filters and has a tuning range of 2.1∼2.9 GHz [5], [39], [40], [41]. The BSF is attached at the bottom of the 4-layer PCB with a shared patterned ground plane. The filter is controlled by forward or reverse biasing five pairs of PIN diodes. The wires on the backside of the BSF are used for controlling the PIN diodes. Fig. 8(b) shows the control for driving the five pairs of PIN diodes involving five sets of PMOS with a drain and source resistor. Fig. 8(c) shows that as the code increases, the BSF center frequency decreases. Fig. 8(d) shows the filter characteristics. The filter has a low pass band loss of about 1 dB, the board adds around 2-3 dB and notches in S21 due to the switches and caps. The rejection of the filter ranges from 6-16 dB, whereas on the board, the rejection ranges from 7-29 dB.

III. Design Consideration and Trade-Offs

A. Directional Coupler

Directional coupler is necessary for reducing the power input to below the power limit of the envelope detector and not

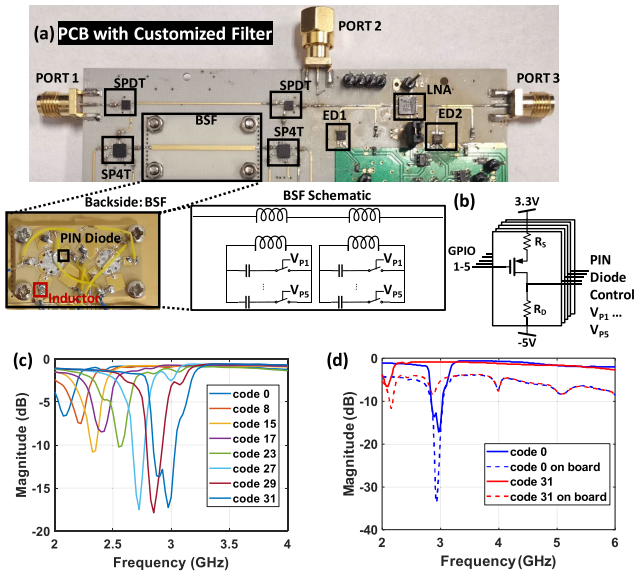

Fig. 8. (a) RF front-end board diagram with customized BSF filter. (b) control scheme to the customized filter. (c) Filter only S21 characteristic. (d) BSF filter S21 characteristics for when there's only the filter (solid line) vs. when the filter is implemented on the board (doted line).

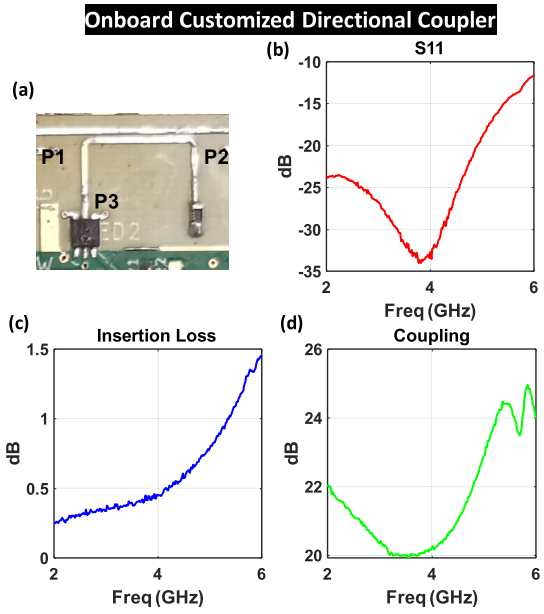

Fig. 9. The onboard directional coupler's (a) PCB implementation diagram (b) return loss (S11) (c) Insertion loss (S21) (d) coupling from the main trace to P3.

to diverge extra power from the signal path for measurement purposes. In our prior work [28], we utilized COTS directional coupler components to provide the measurement path. To minimize space and loss, this paper takes advantage of onboard microstrip design for the directional coupler which avoids extra transition from the board to the component similar to [29]. The microstrip directional coupler schematic is shown in Fig. 9(a). The measurements for the directional coupler are shown in 9(b)-(d). The S11 shows return loss with measurements below −10 dB over the frequency from 2 to 6 GHz. The insertion loss (S21) increases from 0.38 dB to 1.3 dB with frequency. The coupling (S31) ranges from 20 dB to 25 dB.

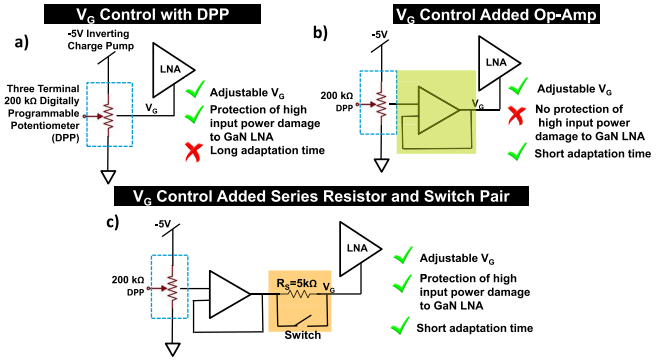

Fig. 10. (a) V_G controller with only the digitally programmable potentiometer; (b) V_G controller with a digitally programmable potentiometer with a buffer; (c) current V_G controller design with buffer and resistor and switch pair to accommodate both low and high input power to the LNA [29].

B. Commercial Filter Considerations/Controls

To provide frequency tuning over the entire band, tunable filters are crucial for the design. To the best of the authors' knowledge, tunable BPF in the frequency range of 2-6 GHz are available, but tunable BSF at this range are not readily commercially available. With the available tunable BPF, the design consists of two adjusted BSF by shunting the BPF parallel to the ground. The filters are placed in parallel, with the arrangement of higher frequency BSF, lower frequency BSF, higher frequency BPF and lower frequency BPF. The consideration behind the arrangement is that since BSF has a wider passband, less signal loss would present over the wide band. Also since higher frequencies have a higher loss, higher frequency filters are designed to have a shorter RF path with a lower line loss.

The control of the filter is provided using a 15 V boost converter connected to a potentiometer to change the voltage between 0-14 V as shown in Fig. 4d). The potentiometer is controlled using SPI on the microcontroller. Since the control node on the filters is high impedance, a buffer is not necessary.

C. GaN LNA Considerations and Linearity Control

GaN LNA is widely used in cases of high power handling. Compare to a more general GaAs material, GaN benefits from the wider band gap and increases the max power input by tens of dB [32]. Different from the GaAs LNAs' low tolerance to the breakdown voltage, GaN LNA's high power effects is more apparent in an exponentially increasing gate current (I_G). Due to a Schottky diode between the gate and source of the GaN LNA, as the input power increases, portions of the sinusoidal voltage can cause the diode to turn on and I_G to increase exponentially which induces a decreasing V_G that can exceed the breakdown voltage and an increased noise figure [42], [43]. At the same time, the device life time can be shortened [1].

The high power effects of the GaN LNA such as the excessive I_G and the subsequently excessive V_G are considered in the linearity tuning design as from our previous work as shown in Fig.10 [29]. To minimize the high power effects of a GaN LNA, increasing series resistance to the gate bias can reduce the excess current on the feedforward diode [1]; however, as the resistance increase, settling time will increase. As shown in Fig.10(a), the series resistance is added with a

digitally programmable potentiometer(DPP) to the gate bias. Next, a buffer is added in Fig.10 to decrease the settling time, but the advantage of the large series resistance is diminished. Thus a parallel network shown in Fig.10(c) is utilized where the series resistance to the gate can be switched between the switch resistance (low) and series resistance (high) for a trade-off between RC settling time and excessive gate current. The high series resistance will be switched in when high input power is detected. The series resistance is chosen to be 5.1 kΩ to significantly reduce the gate current while the gate voltage will drop to -10 V with a significant margin to the limit of -20 V breakdown voltage [43]. Analysis of the high power effects on the system with the V_G tuning circuitry can also be found in our previous work [29].

IV. Orthogonal Frequency and Linearity Tuning

The system flow chart is shown in Fig. 11(a). The system is initially set to the pass-through path with the LNA being set at the lowest linearity and power state (V_G = -2.6 V). The RF input will first go through the pass-through path and the LNA; meanwhile, the first envelope detector (ED1) will determine the power level and the microcontroller will decide whether the input level is out of the linearity range for the LNA. If the microcontroller decides that the input is too high and out of the linearity range, the input will be switched to the known BPF to pass the signal and reject the interference. If the microcontroller decides that the filtered input still exceeds the linearity level, the BPF will tune around the center frequency to tune out inband interference. If the interference level remains high, BSF will be switched on to perform jump search. After a series of BSF searching, the BSF will be set to reject the interference. After all of the frequency optimization, if the microcontroller determines that the linearity is not achieved, linearity tuning will be activated on top of the filter that gave the best interference rejection. Linearity tuning is done by tuning the V_G of the LNA. After a series of tuning, ADC output will be carefully monitored to determine if the interference is no longer present and retract back to the initial state.

A. BPF Tuning Algorithm

The idea of the BPF tuning is shown in Fig. 11(b). Since the interference frequency is unknown, consideration of an in-band interference becomes necessary. The initial BPF is tuned directly to pass the signal frequency; however, when an in-band interference is present, passing the signal may also pass the interference. Therefore, the BPF is tuned around the signal frequency with a little offset such that the signal is not compromised too much and more of the interference is rejected. The BPF tuning can help when the system is borderline linear with an in-band interference, the extra rejection in the interference can bring the system back to linearity.

B. BSF Tuning Algorithm

The idea of the BSF tuning is shown in Fig. 11(c). Fig. 11(c) shows the BSF output ADC measurement when the interference occurs at 4 GHz at a level of -5 dBm and the signal occurs

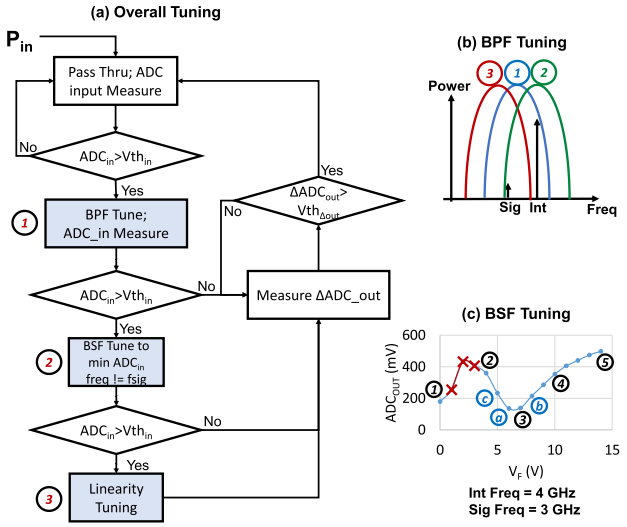

Fig. 11. (a) Overall tuning flow diagram. (b) Details to the steps of BPF tuning. (c) Details to the steps of BSF Tuning with jump search.

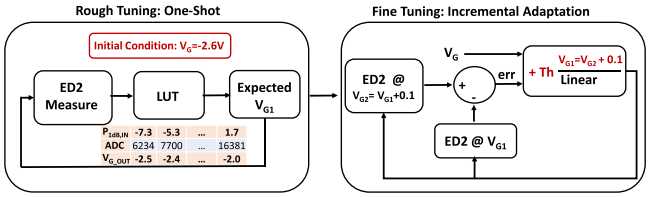

Fig. 12. Linearity tuning diagram with one-shot and incremental adaptation.

at 3 GHz at a very low level. From previous characterization, we know that the filter characterization is far less ideal than a single notch, so a jump search becomes necessary to formulate a general idea of the measurements across frequency tuning voltage (V_F) in order to not mistakenly use a different notch. Also from the characterization done beforehand, we know that V_F of 1 V to 3 V introduces significant rejection at the signal frequency, thus during the jump search, that part is skipped since the rejection of the signal is unwanted. After the jump research generating points 1 to 5, another search would be performed around the lowest point 3 until we decide that point a gives the deepest notch (lowest ADC output) at the interference frequency.

C. Linearity Tuning Algorithm

Linearity tuning involves two tuning stages: coarse tuning through one-shot and fine tuning through incremental adaptation [29]. The tuning is shown in Fig. 12. Linearity is achieved when the input power of the LNA is less than the $P_{1dB,\,IN}$. For the coarse tuning, a look-up table (LUT) is constructed with the ADC measurement at ED2 when the inputs are $P_{1dB,\,IN}$ and associated V_G. So that after ADC measurement, the system will decide which V_G will achieve LNA linearity. For example, for a ADC measurement of 7000, following the LUT in Fig. 12, only a $V_G \geq$-2.4 V will linearize the system. Note that the results from the LUT will be an underestimate because the system needs to operate over a wide frequency range and accommodations for frequencies with low loss is necessary.

Following the underestimation, further tuning with incremental adaptation is utilized. Incremental adaptation

increments the V_G by ΔV_G and compares measurements of V_G+ΔV_G and V_G (ΔV_G = 0.1 V in this implementation). If the measurement increase is greater than the threshold, then linearity is not achieved and further adaptation is required. If the measurement increase is less than the threshold, then the system was already linear, thus the original V_G is outputted.

Since minimizing power consumption is the goal, the current linearity tuning method starts from the minimum linearity and power. If the goal is to minimize the bit error rate (BER), the linearity tuning method can start from the maximum linearity and power. For a balance between the power and BER, the linearity tuning method can start with medium linearity and power.

D. Tuning Time Analysis

The minimum tuning time for frequency tuning (FT) with both BPF and BSF is given by

$$T_{FT} \geq N_{FREQ} * (\tau_{sys} + T_{micro}) + N_{SW} * (\tau_{SW} + T_{SW}) \quad (1)$$

with

$$\begin{aligned} \tau_{sys} &= \tau_{LNA} + \tau_{ED} + \tau_{V_F} \\ T_{micro} &= T_{ADC,samp} + T_{SPI(V_F)} + T_{MISC} \end{aligned} \quad (2)$$

where N_{FREQ} is the number of cycles for frequency tuning; τ_{sys} is the settling time for the system which involves τ_{LNA}, τ_{ED}, and τ_{V_F} representing the settling time of the LNA, ED, and V_F tuning components respectively; T_{micro} is the microcontroller processing time involving $T_{ADC,samp}$, $T_{SPI(V_F)}$ and T_{MISC} representing analog-to-digital converter (ADC) sampling time, SPI communication time to change V_F and miscellaneous processing time respectively; N_{SW} is the number of times the paths needs to be switched, τ_{SW} and T_{SW} are the switch settling time and digital switching time from the MCU respectively.

The overall minimum tuning time for linearity tuning is given by

$$T_{LT} \geq (N_{IA} + 1) * (\tau_{sys} + T_{micro}) \quad (3)$$

with

$$\begin{aligned} \tau_{sys} &= \tau_{LNA} + \tau_{ED} + \tau_{V_G} \\ T_{micro} &= T_{ADC,samp} + T_{SPI(V_G)} + T_{MISC} \end{aligned} \quad (4)$$

where N_{IA}+1 represents the number of cycles in the incremental adaptation and one more for the LUT step, τ_{V_G} is the settling time for the V_G tuning components, and $T_{SPI(V_G)}$ is the SPI communication time to change V_G from the MCU.

Table II shows the measured timing for each of the terms in Eq. 1-4. Fig. 13 shows the total tuning time with respect to processing time with $N_{IA} = 4$ for linearity control, $N_{FREQ} = 12$ and $N_{SW} = 3$ for frequency control. The total tuning time is calculated by adding frequency tuning time from Eq. 1 and linearity tuning time from Eq. 3. With the current operating point, processing time dominates, which is also shown in the table. If a faster processor is used to reduce the processing time to less than 10 μs, the overall tuning time can reduce by a factor of 6 and becomes limited by the system settling time, specifically from the V_F and V_G tuning components. Further improvements in timing are discussed in Sec. VI.

TABLE II
TIMING CHARACTERISTICS FOR FRONT-END WITH COMMERCIAL FILTERS

	Component Settling Time		Instruction Processing Time	
	Timing Item	Time(us)	Timing Item	Time (us)
Frequency Control	τ_{VF}	50	$T_{SPI(VF)}$	38
	τ_{SW}	0.5	$T_{Digital(SW)}$	<1
	τ_{SYS_FC}	50.5	T_{micro}	115
Linearity Control	τ_{LNA}	<0.001	$T_{ADC,Samp}$	76
	τ_{PD}	0.025	$T_{SPI(VG)}$	12.4
	τ_{VG}	7	—	—
	τ_{SYS_LC}	7	T_{micro}	114

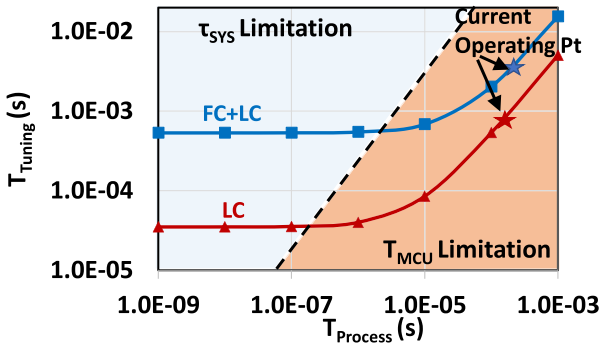

Fig. 13. Total frequency and linearity control tuning time vs. processing time with respect to a varying processing time with $N_{IA} = 4$ for linearity control, $N_{FREQ} = 12$ and $N_{SW} = 3$ for frequency control.

V. MEASUREMENT

A. Commercial Filter Dynamic Measurement

Fig. 14 shows the dynamic response of the system when a large out-of-band interference presents with a small signal. Note that intentional delay is added initially for easier capture of the waveforms. In this case, the signal level is -20 dBm which is significantly lower than the interference level at 14 dBm. The associated filter voltage tuning over time is also included. Initially, SIR and SNR are both low due to the interference overloading the amplifier causing a gain compression. Next, BPF is turned on to reject the interference and pass the signal. The BPF has a passband loss of around 10 dB and a rejection of about 30 dB. Consequently, the gain compression is alleviated, SIR improves by about 15 dB and SNR improves by 7 dB. As the microcontroller determines that the input power is still saturating the LNA, BSF tuning starts to find the point with the most rejection of the interference power. Through the tuning of the BSF, we can see the fluctuation in the SIR and SNR. Eventually, the microcontroller decides the interference is minimized with BSF; however, the input power continues to saturate the LNA, thus linearity tuning is required. After linearity tuning, SIR shows 31 dB improvement and 13 dB in SNR improvement. By calibrating the loss of the filter and switches to around 3 dB, the overall SNR improvement is 16 dB.

Fig. 15 is provided to enhance the understanding of the benefit of showing the dynamic response of the system when

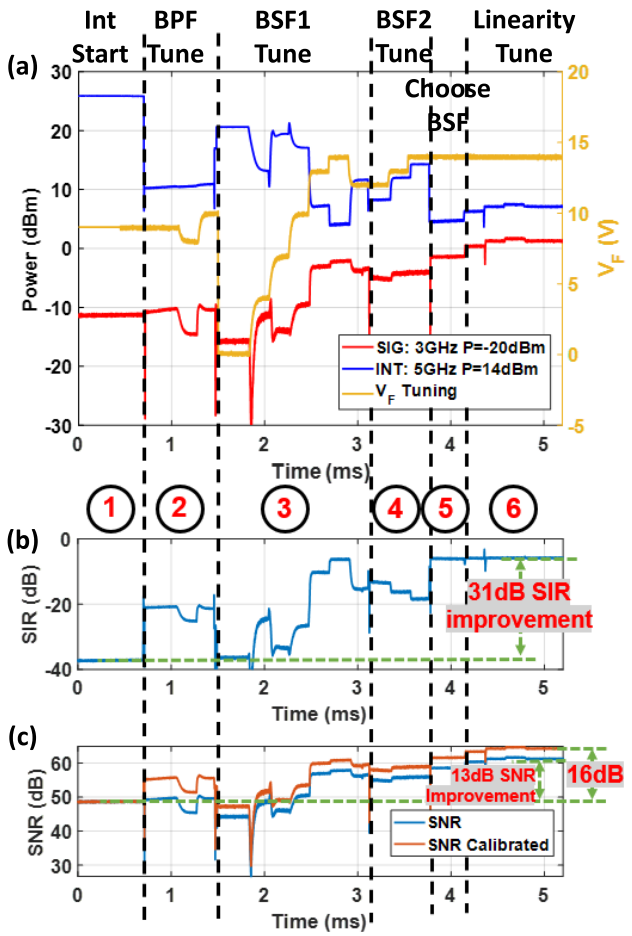

Fig. 14. Dynamic characteristics for the implementation of the commercial filter when signal at 3 GHz with -20 dBm power and interference at 5 GHz with 14 dBm power. Time domain measurements for (a) Signal and interference power levels and associated filter control voltage, (b) Signal to interference ratio (SIR), and (c) Signal to noise ratio (SNR).

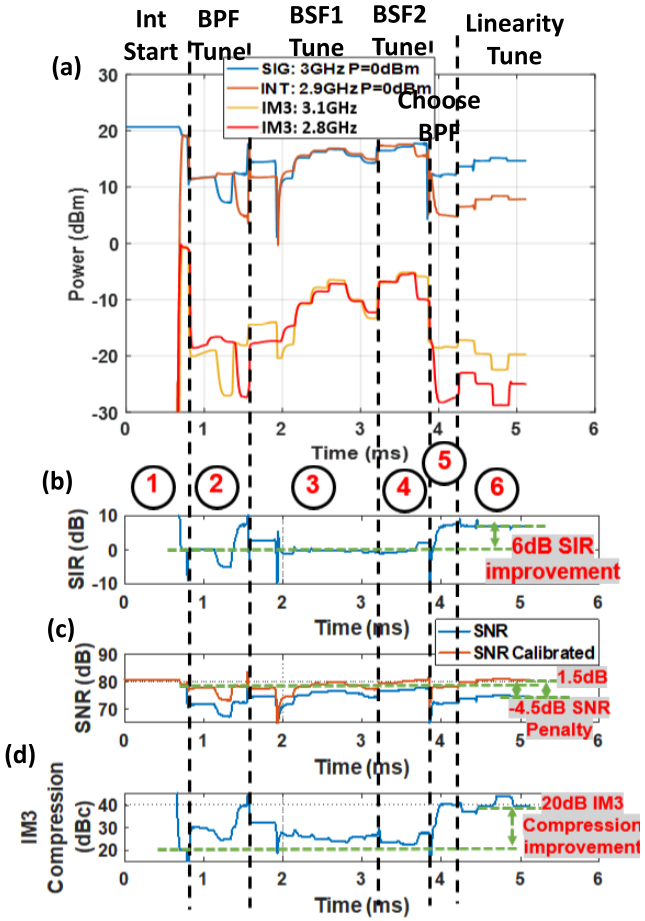

Fig. 15. Dynamic characteristics for the implementation of the commercial filter when signal at 3 GHz with 0 dBm power and interference at 2.9 GHz with 0 dBm power. Time domain measurements for (a) Signal and interference power levels and 3_{rd} order intermodulation product (IM3), (b) Signal to interference ratio (SIR), (c) Signal to noise ratio (SNR), and (d) IM3 compression.

the signal and in-band interference have similar power levels. The system eventually decides that by tilting the BPF to a little higher frequency, the interference is minimized with the signal largely unaffected. After going through the frequency tuning and linearity tuning, SIR shows a 6 dB improvement, SNR shows a 4.5 dB degradation, adjusted SNR by adjusting the filter and switch loss to 3 dB shows a 1.5 dB improvement and IM3 compression shows a 20 dB improvement. Because the input level is lower than in Fig. 14, the improvement in the SIR and SNR are less because the gain compression of the LNA is less. The reason that the SNR shows a degradation is that the inherent filter loss is more than the gain compression, thus by assuming the filter loss is less, SNR is improved. As shown in the plot, the IM3 compression at 3.1 GHz has improved by 20 dB whereas the IM3 compression at 2.8 GHz has improved by 24 dB. The difference in the IM3 components is because the signal level at the end is higher than the interference level, so the IM3 component close to the signal frequency would be higher.

B. Custom Designed Filter Dynamic Measurement

Fig. 16 shows the dynamic response of the customized filter system when the interference power is 10 dBm with frequencies of 2.9 GHz and 2.5 GHz. With the interference at 2.9 GHz which is at the edge of the customized BSF tuning range from 2.1-2.9 GHz, the tuning is faster because of fewer points to sweep around. Also because the rejection at 2.9 GHz is higher, linearity tuning was not required. On the other hand, the rejection at 2.5 GHz is much lower, thus linearity tuning is required.

C. Other System Metric

The NF for the commercial filter board in the pass-through path, board with only linearity tuning, and the datasheet measurement is shown in Fig. 17. Due to the extra switch losses and the directional coupler losses, the NF has degraded about 2-3 dB for the commercial filter board.

Fig. 18 shows SIR performance after the system finishes tuning when the difference between the signal and interference frequencies increases. As expected, when the interference is in-band, the interference becomes harder to filter out showing a SIR improvement of less than 10 dB. When the interference moves further away from the signal in frequency, the filters are able to filter out more interference showing a SIR improvement greater than 10 dB.

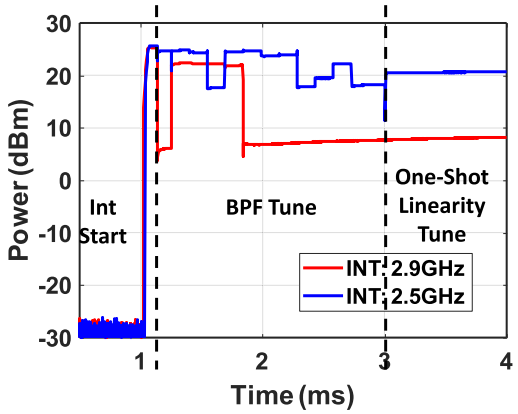

Fig. 16. Dynamic characteristics for the customized filters for when the interference frequency is at 2.9 GHz and 2.5 GHz. Both interferences have an input power of 10 dBm.

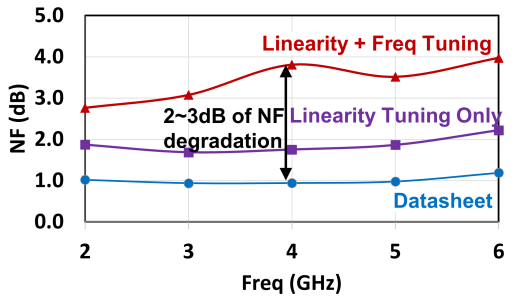

Fig. 17. Noise figure (NF) measurement comparison between datasheet, linearity tuning only implementation and linearity + frequency tuning implementation.

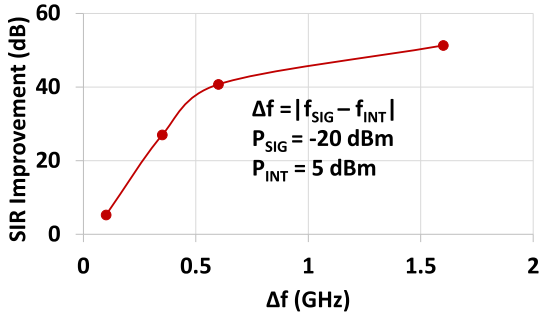

Fig. 18. SIR improvement vs. Δf where Δf is the difference between the signal and interference frequencies when the interference (5 dBm) is much stronger than the signal (-20 dBm).

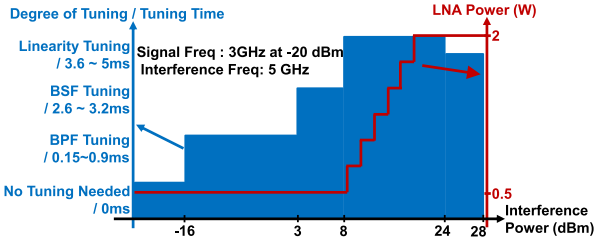

Fig. 19. Degree of tuning and approximate LNA power vs. interference power.

Fig. 19 shows the amount of tuning required and tuning time as well as the LNA power consumption with respect to the interference level. In this case, the interference is at 5 GHz, with a signal at 3 GHz and -20 dBm. As shown in the plot, when the interference level is less than -16 dBm, no tuning is required and the LNA would be able to work in the minimum power mode with enough linearity to be not saturated and gain compressed. Between the interference levels of -16 to 8 dBm, only frequency tuning is required with a tuning time of less than 3.2 ms. Note that the frequency tuning does not add any power penalty to the LNA. Between the interference levels of 8 to 24 dBm, linearity tuning would be required and increases the total tuning time to anywhere between 3.6-5 ms. When linearity tuning is required, LNA power would be traded for higher linearity, thus we see an increase in the LNA power. As the interference level exceeds 24 dBm, only one-shot of the linearity tuning will be activated to give the LNA max linearity and max power, thus reducing the tuning time.

The comparisons between the systems of 1. LNA operates at worst-case conditions without any tuning, 2. LNA with linearity tuning only and 3. LNA with frequency and linearity tuning are shown in Fig. 20. Overall, the system with the frequency and linearity tuning has the advantages over the no-tuning LNA, such as lower average LNA power, wider power tuning range, and higher max input while maintaining LNA linearity. Average LNA power is the average power that the LNA would consume over the input power range from -20 dBm to 28 dBm. Average LNA power has improved by 56%. For the power tuning range, the linearity and frequency tuning system enable tuning over a 40 dB range as compared to no tuning range when LNA is at the worst-case condition. The maximum input power that the frequency and linearity tuning system can obtain without the saturation of the LNA is 21.5 dB higher than the system with no tuning. The max input power improvement allows linearity to be achieved close to the max power handling of the system. The penalties of the frequency and linearity tuning system are the lengthened tuning time to a max of 5 ms, increased pass-through path loss to 3 dB due to the losses from the switches, directional coupler, and filters, degradation of about 2.5 dB NF, and extra control power of 200 mW which is about 10% of the LNA power operating at worst-case.

D. Comparison Table

Table III shows the different works that contribute to adaptive transceivers with different implementation methods. Note that the system power can be separated in two parts: the RF component power and the system power required to perform all the sensing and tuning. Since this work focuses on high-power handling components, the GaN LNA power is much higher than the state of the arts. Many of the state of the arts do not report system power due to the lack of a fully integrated system with the sensing and feedback on board. The tuning time is slower than [4] and [5] mainly due to the choice of the processor, and slower than [29] due to the additional degree of tuning with the frequency. The trade-off between [29] and this has been explained and shown in Sec. V-C and Fig. 20.

VI. Future Works

Future work can be done on minimizing the losses and extra return loss such as using better switches or integrating the

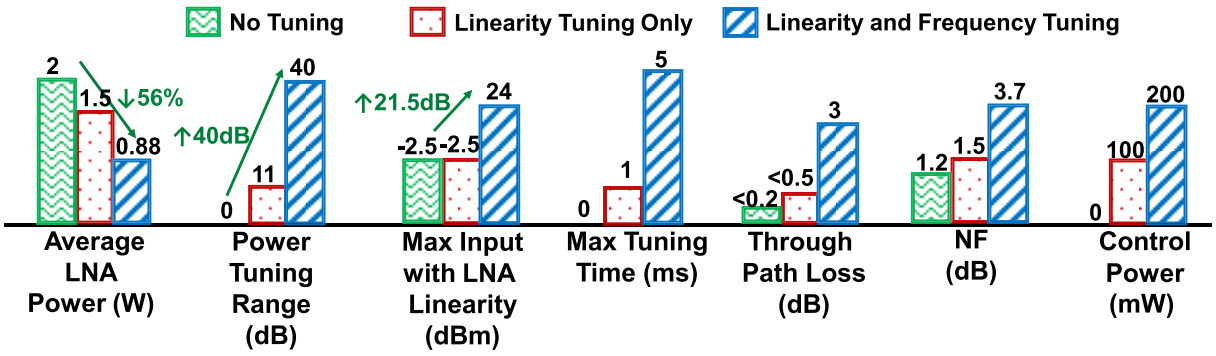

Fig. 20. Comparison between no tuning LNA, linearity tuning only implementation, and linearity with frequency tuning implementation. Power tuning range and max input with LNA linearity data taken with signal at 3 GHz and interference at 5 GHz. Through path loss and NF data taken at 6GHz.

TABLE III
COMPARISON TABLE

	Multi-Octave Interference Detectors [4] [5] MWCL'22 TMTT'22	Blocker Cancellation LNA [6] TMTT'22	Computation Communication Trade-off [22] JSSC'22	Blocker Tolerant with Harmonic Rejection Front-end [23] JSSC'18	Multi-Parameter Adaptation Receiver [24] TCASI'14	Pro-VIZOR [19],[25] DAC'08 TCAD'14	Data Priority vs Energy Priority Adaptative Transceiver [26] TCAD'15	GaN Linearity-Power Tradeoff Front-end [28] [29] MWCL'21 TMTT'23	**Orthogonal Frequency and GaN Linearity Tuning Front-End This Work**
Implementation*	COTS + PCB	IC (65nm)	IC (65nm)	IC (65nm)	IC (180nm) + COTS	COTS	COTS	Integrated PCB	**Integrated PCB**
Control Goal	Max Interference Detection	Blocker cancelation	Optimize energy, latency and BER	Harmonic rejection	Noise, linearity and power trade-off	Power optimization	High Throughput ↔ Low energy/bit	LNA Linearity ↔ Power	**1. Interference Detection & Rejection 2. GaN LNA Linearity ↔ power**
Control Mechanism	Bandstop filter bias bias	LNA with another feedforward path with N-path filter mixers to notch signal and copy blocker to subtract after LNA	Actor-critical neuro-controller for processing depth, PA power out and error correction code	Harmonic rejecting N-path filters with LNA	Tuning knob and automatic gain control tuning while maintaining minimum SNIR	PAR reduction at Tx, supply and bias for LNA and mixer at Rx with BER limitations	LUT for Transmitter parameters	LNA V_G Bias	**Filter Frequency Bias & LNA V_G Bias**
Detection Parameter	Frequency + Power of the highest interference	----	Path-loss, noise power, network size, information content	----	SNIR	EVM	EVM	Power	**Power**
Detection Method	Power detectors + ADCs at different points on an open circuit stub	----	On chip calculations	----	FPGA SNIR measurement	Baseband EVM calculation in MATLAB	Baseband EVM calculation in MATLAB	Envelope detector + ADC	**2x (Envelope detector + ADC)**
Processor	FPGA	----	On chip DNN processing elements	----	FPGA	PC MATLAB	PC MATLAB	Microcontroller	**Microcontroller**
Power Handling	High with coupler	Low	Low	Low	Low	Low	Low	High	**High**
System Power (mW)	System: 800	LNA : 20	----	LNA: 33.8 ~ 43.8	----	LNA + Mixer : 20 ~ 150	-----	LNA: 500 ~ 2000 System: 100	**LNA: 500 ~ 2000 System: 200**
Frequency (GHz)	1-16	1.35 ~ 2.7	2.4	0.2 ~ 1	0.6	2.4	2	2~6	**2~6**
Tuning Time	500 ns	----	----	-----	----	----	-----	1 ms	**<5 ms**
Comment	Stub area limitation	Chip measurement only	----	Chip measurement only	----	Not integrated on one PCB	Not integrated on one PCB	Controls can be implemented on IC to improve tuning performance	**Controls Can be implemented on IC to improve tuning performance**

* IC+COTS: Custom IC with COTS connected through SMA connector. COTS: COTS connected through SMA connector. COTS+PCB: some custom microwave components connected with some components integrated into the PCB. Integrated PCB: components are integrated into one PCB without any SMA connections to other components.

switches into customized filters. With a better filter response, linearity tuning can be simplified to a LUT sorted by different frequencies since the interference frequency can be determined by which BSF gives the minimum reading. Furthermore, 40% of the power consumption comes from the microcontroller, so with a microcontroller such as the Ambiq Apollo4 [44] with a power efficiency of 5 μA/MHz. Another future work can involve designing an application-specific integrated circuit (ASIC) for a smaller form factor to use in mobile devices which can bring significant cost savings on the filters with the implementation of tunable filters. A greater reduction in tuning time can be achieved with a processor with higher clock speeds, and a lower RC time constant for V_G by using a lower overall resistance in the potentiometer and V_F by including an operational amplifier as a buffer.

VII. CONCLUSION

Overall, this paper provides a wide-band tunable GaN receiver front-end for high-power applications with complete system-level demonstration to show the capability of fast real-time adaptation in the 2-6 GHz range with minimal increase in control power. The interference adaptive GaN LNA front-end utilizes orthogonal frequency and linearity tuning through onboard processing with a microcontroller. The system provides 40 dB of tuning range up to a max linear input power of 24 dBm with average LNA power decreased by 56% from the worst-case operating point of the LNA. The system consumes a power of 10% of the worst-case LNA power for an LNA linearity increase from -10 to 1.5 dB. Tuning algorithms are formulated to minimize tuning time and power consumption from the GaN LNA. A timing analysis of

the current commercial filter setup is presented with an overall timing of sub 5 ms. The system has been implemented with both commercial filters and a customized BSF.

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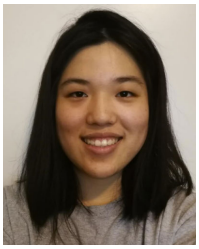

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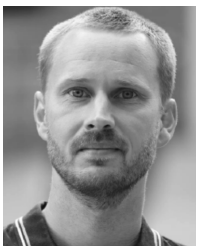

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