Instinctual Interference-Adaptive Low-Power Receiver With Combined Feedforward and Feedback Control

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***Abstract*— Highly adaptive, instinctively interference-tolerant radio frequency (RF) receivers are in high demand today. To achieve high-interference robustness at low average power, receivers need to be dynamically configured to operate in low-power mode in the absence of interference and a high-power interference-tolerant mode as an "instinctual" response to the blocker. In this letter, we present an interference-adaptive receiver with a control loop and on-board commercial off-the-shelf (COTS) components that adapt a 2–6-GHz low-noise amplifier (LNA) from a low-power mode (−10-dBm $P_{1\,dB,IN}$ and ≈280-mW power) to high-linearity mode (1.5-dBm $P_{1\,dB,IN}$ and ≈1.4-W power) where the linearity is increased by 11.5 dB (>14×) with a 5× increase in consumed power. With no interference, the control loop automatically brings the LNA back to the low-power mode.**

***Index Terms*— Adaptive, front end, interference robust, low-noise amplifier (LNA).**

I. Introduction

With increasing number of standards and bands that co-exist today for wireless communication, interference is fast becoming the primary bottleneck in radio frequency (RF) receiver (Rx) design. When the Rx is designed for worst case interference scenarios (or for interference cancellation), the power consumption increases significantly [1]–[3]. The dynamic nature of the interference calls for bio-inspired interference-adaptive radio design, which would consume additional energy to demonstrate interference tolerance only when necessary.

Current efforts on demonstrating an interference-tolerance system focus more on the circuit-level design of the low-noise amplifier (LNA) [4]–[6]. Our group's earlier works on VIZOR, Pro-VIZOR, adaptive LNA integrated circuit design, system-level receiver optimization, and adaptive transmitter act as the background to the present work [7]–[14]. This letter presents a system-level control loop switching the LNA between the low-power mode and high-linearity mode. Fig. 1 shows the conceptual idea of a control loop that helps in improving the quality of the received data. When the interference is large compared to the signal, the control loop helps in alleviating gain compression (increasing the linearity of the receiver). In the presence of multiple interference frequencies, the control loop would also help minimizing the in-band third-order intermodulation component (IM3) that would have otherwise been significant. A fast interference-detection scheme using hardware techniques is one of the main contributions of this work.

The rest of this letter is organized as follows. Section II describes the proposed board design and the characterization of individual components for fast interference detection. Section III presents the working principle and performance of the control loop. Our contributions are summarized in Section IV.

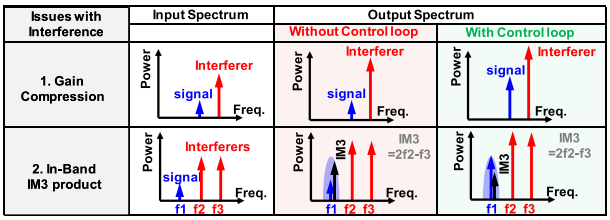

Fig. 1. Motivation of instinctual interference adaptation in an RF Rx with help of a control loop for when interference is large and when multiple blockers are present.

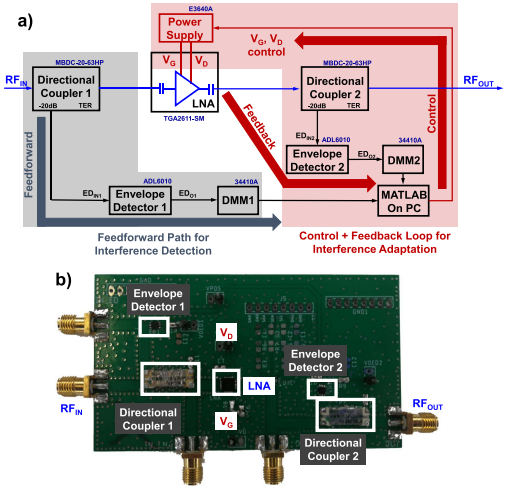

Fig. 2. (a) Architecture of the interference-adaptive Rx. (b) PCB design.

Manuscript received February 21, 2021; accepted February 25, 2021. Date of publication March 22, 2021; date of current version June 7, 2021. This work was supported in part by SAAB AB, Sweden, and in part by SAAB Inc., USA. *(Corresponding author: Jie Yang.)*

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This article was presented at the IEEE MTT-S International Microwave Symposium (IMS 2021), Atlanta, GA, USA, June 6–11, 2021.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWC.2021.3067912.

Digital Object Identifier 10.1109/LMWC.2021.3067912

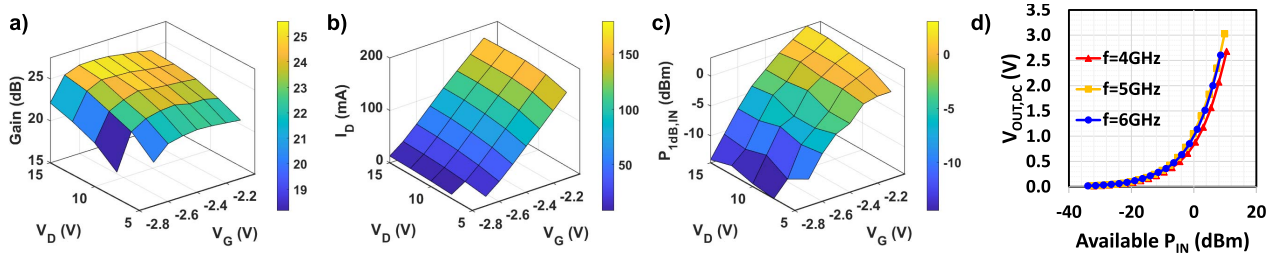


Fig. 3. Measured performance characterization of the components used: (a) LNA gain versus V_D and V_G at 4 GHz, (b) LNA drain current (I_D) versus V_D and V_G at 4 GHz, (c) LNA input $P_{1\,dB}$ ($P_{1\,dB,IN}$) versus V_D and V_G at 4 GHz, and (d) dc output voltage of the envelope detector (ED) versus available input power to the ED.

TABLE I
SYSTEM ARCHITECTURE AND PCB IMPLEMENTATION

Component	Part Number	Specifications
LNA	TGA2611-SM (Qorvo) [16]	2-6GHz, 1dB NF, 22dB Gain, -4dBm $P_{1dB,IN}$, 1W nominal power
Coupler	MBDC -20-63HP [17]	2-6GHz, 0dB (through), -20dB (coupled), 100W max, 50Ω
Envelope Detector	ADL6010 [18]	0.5-43.5GHz, 4ns rise time, 1.6mA, 2.1V_{OUT}/$V_{PEAK,IN}$, 50Ω

II. HARDWARE DESCRIPTION AND CHARACTERIZATION

A. System Architecture and PCB Design

For proof-of-concept demonstration of the interference-detecting control loop, an FR4 PCB is developed with commercial off-the-shelf (COTS) components. The system architecture and the details of the board are presented in Fig. 2. The RF input signal is passed through the directional coupler 1, with the through port (up to 0.25-dB insertion loss within 2–6 GHz) connected to a 2–6-GHz GaN LNA, the −20-dB coupled port connected to envelope detector 1 (ED1), and the isolated port terminated with 50 Ω. The LNA's gain, power consumption, and linearity can be controlled by its supply voltage (V_D) and gate bias (V_G) [15], which would be utilized by a control loop containing feedforward and feedback paths.

The control loop as shown in Fig. 2(a) is implemented in MATLAB on a personal computer (PC), which receives the output of ED1 through a digital multimeter (DMM1) using GPIB connections. The output of ED1 represents the strength of the input signal (and hence, any high-amplitude interference present would manifest itself as a high dc voltage at the output of ED1, thereby detecting the blocker in a feedforward manner). The 20-dB reduction through the directional coupler is necessary due to the input power constraints of the envelope detector used. The through ports of the two directional couplers, along with the LNA, consist of the RF front end, which would be connected to a mixer and subsequent baseband stages in a standard RF Rx. The control loop in MATLAB determines V_D and V_G of the LNA according to the characterization data of the components and in the presence of interference. The output of the LNA connects to the same MATLAB script through directional coupler 2, envelope detector 2 (ED2), and DMM2. The information from ED2 is processed as feedback information for achieving high linearity, as will be shown in Section III. The PCB implementation is also shown in Fig. 2(b). The COTS components used are described in Table I.

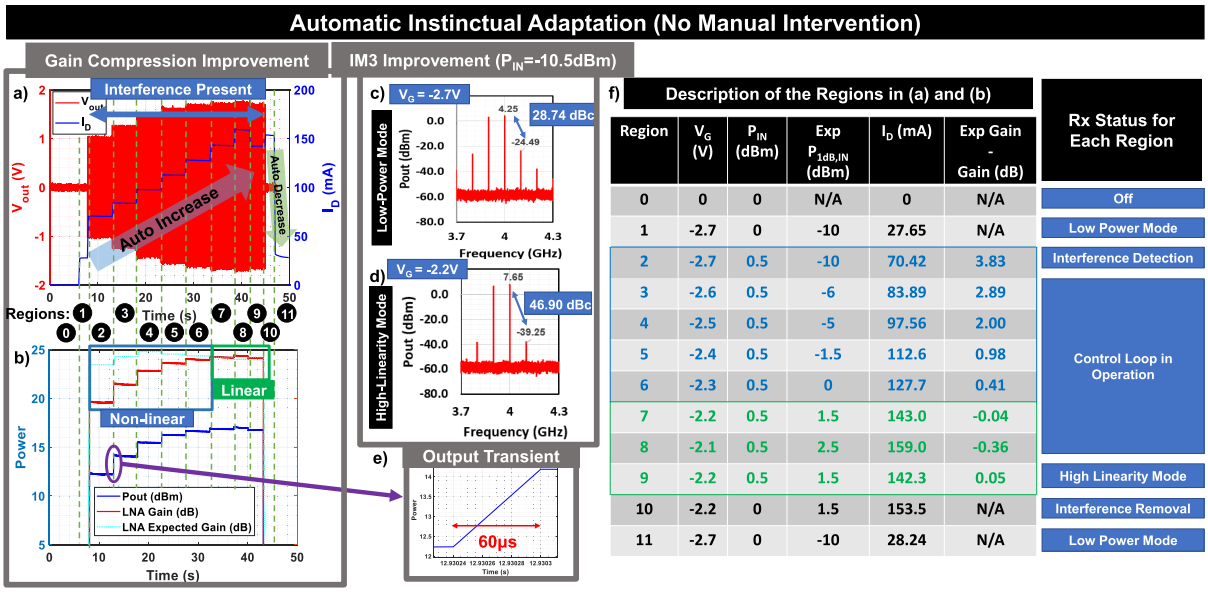
B. Characterization of PCB Components

The PCB components were characterized in the range of 2–6 GHz to cover LTE, sub-6-GHz 5G, and the Internet of Things (IoT) applications. During the characterization process, the losses due to SMA cables and the FR4 PCB are calibrated carefully. Fig. 3(a)–(c) shows the characterization data for the LNA at 4 GHz of frequency. As the supply voltage (V_D) increases from 5 to 15 V, the gain of the LNA increases by 2.5–4.5 dB depending on the value of V_G. As V_G increases from −2.8 V, the gain initially increases and then saturates for $V_G \approx -2.5$ V. The gain increases by 2–6 dB depending on V_D. After saturation, the gain gradually degrades by ≈1 dB when V_G reaches −2.1 V. The interdependence of both V_G and V_D makes the LNA gain a weak function of both V_D and V_G. The supply current and linearity, however, are strong functions of V_G (and extremely weak functions of V_D). As V_G varies from −2.8 to −2.1 V with V_D of 10 V, the supply current changes from about 20 to about 180 mA (increases by 9×). With the same range of V_G and V_D of 10 V, the input $P_{1\,dB}$ ($P_{1\,dB,IN}$) of the LNA varies from −14 to 2.5 dBm (increases by 16.5 dBm or ≈45×). This analysis signifies that the LNA's bias voltage can be utilized as a tuning knob to increase linearity at the cost of power in the presence of interference.

To detect the presence of interference, the combination of directional coupler 1 and ED1 is used. The output dc voltage of ED1 ($V_{OUT,DC}$) is plotted against the input signal power at frequencies of 4, 5, and 6 GHz in Fig. 3(d). The plot shows an exponential trend of $V_{OUT,DC}$ with increasing input power, and the minimum detectable signal is around −30 dBm with $V_{OUT,DC} \approx 20$ mV. Since the received desired signal is typically $\ll$−10 dBm and is further reduced by 20 dB at the coupled port of the directional coupler 1, any $V_{OUT,DC} >$ 20 mV would be considered as the presence of interference.

III. DEVELOPMENT OF THE CONTROL LOOP

Utilizing the characterization data of individual components, the real-time control loop is developed in MATLAB, and note that the timing of each step is lengthened to clearly see the transitions. In a future work, this control loop would be developed using an on-board ADC (representing DMM1 and DMM2) and a microcontroller. Fig. 4(a) and (b) shows the timing diagram of the control loop in action with V_D fixed at 10 V. In region 1, no interference is present and the LNA operates in low-power mode ($I_D \approx 28$ mA and $P_{1\,dB,IN} = -10$ dBm). In region 2, ED1 detects the presence of interference in the feedforward path. After detecting the interference, in regions 3–8, the feedback controls V_G to automatically step up to find the lowest V_G that achieves necessary linearity. In the effort of achieving linearity, V_G increases from −2.7 to −2.3 V, in steps of 0.1 V, and eventually determines that



Region	V_G (V)	P_{IN} (dBm)	Exp $P_{1dB,IN}$ (dBm)	I_D (mA)	Exp Gain - Gain (dB)
0	0	0	N/A	0	N/A
1	-2.7	0	-10	27.65	N/A
2	-2.7	0.5	-10	70.42	3.83
3	-2.6	0.5	-6	83.89	2.89
4	-2.5	0.5	-5	97.56	2.00
5	-2.4	0.5	-1.5	112.6	0.98
6	-2.3	0.5	0	127.7	0.41
7	-2.2	0.5	1.5	143.0	-0.04
8	-2.1	0.5	2.5	159.0	-0.36
9	-2.2	0.5	1.5	142.3	0.05
10	-2.2	0	1.5	153.5	N/A
11	-2.7	0	-10	28.24	N/A

Fig. 4. Measured timing diagram of the control loop in action. (a) RF output voltage (V_{OUT}) and LNA supply current (I_D) versus time. (b) LNA measured output power, measured gain, and expected gain (from characterization data) versus time. (c) LNA output spectrum at $V_G = -2.7$ V. (d) LNA output spectrum at $V_G = -2.2$ V. (e) Output transition time. (f) Description of the regions: from low-power mode to high-linearity mode through automated control loop.

V_G of -2.2 V is sufficient for the receiver to be linear. The determination of required V_G is done using the feedback control using ED2 to measure the voltage difference of the output of the LNA as V_G increases. From $V_G = -2.7$ to -2.6 V, the change in P_{OUT} is 1.8 dB, which is relatively large because of the greater gain compression when $V_G = -2.7$ V. As V_G keeps on increasing, the change in P_{OUT} becomes smaller, and eventually at the transition of $V_G = -2.2$ to -2.1 V, the change is only 0.12 dB. The gradual decrease in the change in output level is also apparent in the V_{OUT} versus time plot in Fig. 4(a). A change of 0.12 dB is considered insignificant from the characterizations of the individual components, and thus, the control loop determines that $V_G = -2.2$ V is sufficient as shown in region 9. Region 10 shows that V_G continues to be at -2.2 V as interference is no longer present due to the delays of using DMM1 for measuring ED1 output. In a more advanced implementation with a fast ADC and microcontroller, the delay shown in region 10 would be significantly minimized (also each of the section durations will be scaled down). In region 10, ED1 determines that the interference is no longer present and turns V_G back to low-power mode in region 11. As shown in Fig. 4(b) as well as highlighted in blue in Fig. 4(f), in the nonlinear region, as V_G increases, the difference of the expected (from characterization) and measured gain gradually decreases [and becomes $\ll$1 dB in the linear region, which is also highlighted in green in Fig. 4(f)]. The decrease in gain difference shows reduced gain compression and ensures lower IM3 in the linear region. As shown in Fig. 4(c) and (d), the IM3 components are reduced by $>$18 dB in a two-tone test by moving from the low-power mode to the high-linearity mode. Fig. 4(e) shows that the transition time for the output signal is about 60 μs. Fig. 4(f) shows the details of each region and the status of the receiver.

With this technique, the LNA can operate at 280 mW instead of the nominal 1-W power as specified in the datasheet for most of the time (without interference) and can switch to a 1.4-W mode when interference is detected. The overall power consumption in the additional circuitry (two passive directional couplers, two envelope detectors consuming 10 mW each, and an estimated 40 mW for the ADC and microcontroller in an advanced implementation) is $\approx$60 mW, which is only a 6% overhead when interference is present, but saves 60% power in the absence of interference. As shown in Fig. 5, if the interference is present for $\approx$1%–10% of the time during normal operation, the power savings would be in the range of 60%–50%. In Fig. 5, region 1 shows that when interference is present for up to $\approx$60% of the time for normal operation, the Rx would save average power while increasing linearity when required; region 2 shows that 4 dB better linearity than nominal can be achieved at 30% power overhead.

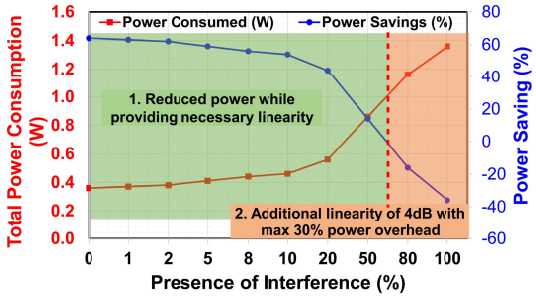


Fig. 5. Power savings using the control loop: the overall power savings (with respect to the nominal 1-W operation of the LNA) and total power consumption versus the amount of time interference are present during normal operation (in %).

IV. Conclusion

This letter presented an interference-detection scheme with both feedforward and feedback control and with on-board COTS components that dynamically adapt the operating point of a 2–6-GHz LNA from a low-power mode (-10-dBm $P_{1\,dB}$ and 280-mW power) to a high-linearity mode (1.5-dBm $P_{1\,dB}$ and 1.4-W power). In the absence of interference, the control loop brings the LNA back to the low-power mode. The high-linearity mode reduces the effects of gain compression and improves IM3 by $>$18 dB, leading to a linearity improvement of $\approx$11.5 dB.

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