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Theoretical Analysis of Multi Integrating RX Front-Ends for Lossy Broad-Band Channels

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ABSTRACT Recent advances in wire-like communication channels without a physical wire has seen the emergence of wireline-like broadband channels but with atypical high loss. Communication links using such channels (e.g., Proximity Communication, Human Body Communication) are typically broadband, like wireline systems but noise-limited like wireless systems. Hence, employing broad-band communication through such emerging channels calls for new research on analyzing, designing and finding the theoretical limits for receiver topologies suitable for *lossy broad-band channels*. In this paper, we present a theoretical analysis framework for various broadband receivers in combination with low-noise amplifiers and proposed multi-integrator cascade, which provides significant gain with relatively lower power consumption than the standard gain elements. Through 1) derivation of new noise analysis of integrating-sampling receivers, 2) proposal of a new circuit topology (multi-integrating receiver, MIR) and 3) development of a thorough design space exploration framework, including use of a combination of wireless-inspired Low-noise amplifiers (LNA) with wireline-inspired strong-ARM latches, and the newly proposed MIRs, this paper demonstrates the optimum design choices for some common scenarios. Maximum achievable data rate and optimum energy-efficiency for various channel losses have been obtained theoretically for different topologies revealing their advantages and limitations, intended to serve as a guide for future receiver designs for *lossy broad-band channels*. All the circuits have been designed in 65 nm CMOS process with a 1 V supply voltage.

INDEX TERMS Current integrating amplifier, broad-band communication, noise, channel loss, wireline-like channels.

I. INTRODUCTION

With the incessant increase in the demand of flexible, efficient and secure communication between electronic devices, several communication standards, schemes and PHYs (or, physical layer transceivers) have emerged and many more are expected to come in future. The primary focus of any type of communication remains on the optimization of energy-efficiency, i.e., the energy spent on transmitting a single bit, as well as maximizing the data rate. Among different types of communication, wireline communication through electrical links and wireless communication through air-medium are two of the prominent. In wireless communication, due to the practical form-factor of antennas and FCC limitations of usable frequency bands, modulation or frequency up-conversion in the Transmitter (TX) followed by a demodulation or frequency down-conversion in the Receiver (RX) are of absolute necessity. Due to deployment of modulation/demodulation schemes, high channel loss ($\sim 60-80$ dB) of wireless channel and the need for high carrier frequencies for manageable antenna sizes providing efficient radiation, the power consumption is sufficiently high in wireless transceivers. In popular wireless techniques such

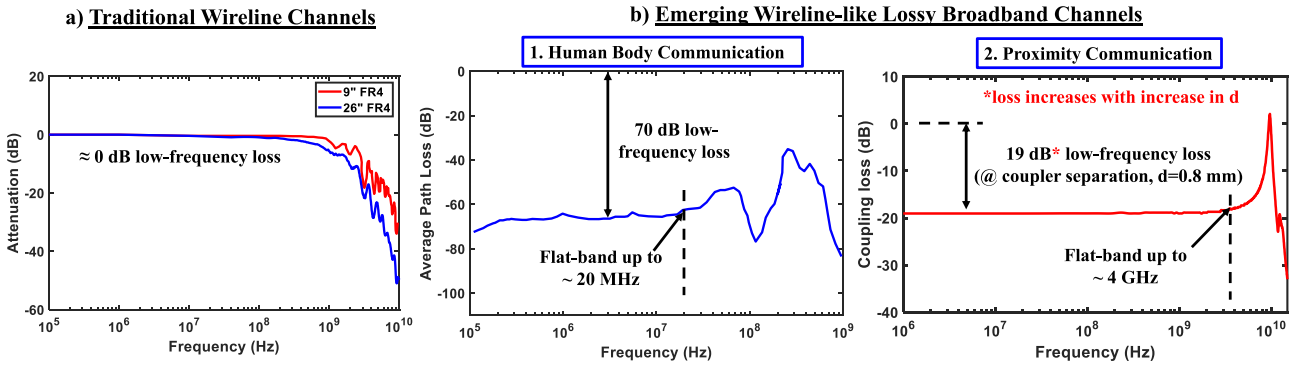


FIGURE 1. Channel characteristics of different broadband channels: (a) Traditional wireline-channels ([2], [3], [4]) having ≈ 0 dB low-frequency channel loss and hence, offering very small signal attenuation. Figure shows the loss characteristics of a 9" and a 26" FR4 PCB traces; (b) Emerging wireline-like lossy broadband channels with large low-frequency channel loss. Human Body Communication ([11]–[22]) and mm-scale Proximity Communication ([6], [7]) are typical examples of such applications.

as Wi-Fi, near-field communication (NFC), ZigBee, BTLE etc. the best energy-efficiency that can be achieved is close to or sometimes significantly greater than few nJ/bit [1]. On the other hand, in wireline communication through electrical links, availability of a flat-band low-loss channel upto a certain frequency that is dedicated for each link and does not interfere with others, enables broad-band communication alleviating the need for upconversion/down-conversion in most cases. This along with a small low-frequency channel loss reduces the transceiver energy consumption drastically and increases the data rate. For typical wireline applications such as backplane, ethernet, USB etc. the energy efficiency has been reported to be as low as $\approx 1-10$ pJ/bit ([2], [3], [4]), while the data rate has been pushed even up to 60 Gb/s in recent works [5].

In the recent years, there have been emerging examples of electrical communication that do not have a physical wire (similar to wireless) but achieve wireline-like *broad-band channels*, except one key difference, i.e., *much higher loss*, even at very low frequencies. Specific examples include μm to mm-scale *Proximity Communication* ([6]–[10]) and meter-scale *Human Body Communication* (*HBC*) ([11]–[22]). In the former case, the channel behaves like a simple capacitive divider giving a maximally-flat frequency response and hence, a proximity connector can utilize wireline-like broad-band signalling and mixed-signal processing for energy-efficient implementation. However, unlike typical wireline channels, in proximity communication the channel offers significant low-frequency attenuation to the transmitted signal due to the division of the air capacitor and receiver capacitor. The amount of low-frequency loss further increases with increase in coupler separation. For the latter case (i.e., HBC), two wearable devices placed on two different locations of the human-body communicate among themselves by utilizing the conductivity property of the human body and using it as the communication medium. Capacitive HBC is the most widely used form of HBC for wearable devices, for which the channel response is strongly governed by the parasitic return path capacitance [22], [28], [29]. The other primary factor, which determines the channel response, is the termination on the receiver end. A 50 Ω termination at the receiver end results in high loss at low frequencies and hence a high pass response ([23]–[27]). However, a high impedance capacitive termination at the receiver end [15], [17] enables a flat-band response with low frequency roll off at frequencies $<$100kHz. This flat frequency response enables broad-band signaling through human body channel resulting in energy-efficient implementation of HBC transceivers [20].

Fig. 1 shows the typical channel transfer functions of different channels exploited for broad-band communication. A wireline channel typically has $\approx$ 0 dB low-frequency channel loss and a flat-band up to a certain frequency (Fig. 1(a)) resulting in simple implementation of wireline transceivers for lower data rates. However, for higher data rates of transmission, wireline channels, due to the high frequency roll-off, offer frequency dependent attenuation to the transmitted signal causing inter-symbol interference (ISI). Hence, while designing transciever circuits for wireline links, which are typically *ISI-limited but not noise-limited* major emphasis is given in mitigation of ISI which limits the maximum achievable data rate. In a typical wireline channel, as the low-frequency channel loss is very small, the input signal is not highly attenuated. In that case, the data rate can be ideally pushed closed to the channel bandwidth (or up to the speed where the loss at Nyquist frequency is still low) without incurring any significant ISI. After such data rate, the data-eye starts closing due to significant ISI and signal amplitude becomes comparable with the noise limiting the data rate. On the other hand, for the emerging applications utilizing wireline-like *lossy broad-band channels* for communication (i.e., the idealistic channel considered in this work), the signal becomes comparable with noise even in the absence of any ISI. In that scenario, the channel can be referred as noise-limited and not ISI-limited. Hence, it can be understood that for any channel, the low-frequency channel loss determines whether a channel is noise-limited or not. Fig. 1(b) shows the channel responses for a typical HBC channel and a proximity communication channel, as two examples of *lossy broad-band channels*. Though it's

very challenging to figure out the exact HBC channel characteristics for higher frequencies, recent advancements in this field confirm the HBC channel to be flat-band upto $\approx$ 20 MHz [30] along with a flat-band channel loss as high as $\approx$ 70 dB. Similarly, in case of proximity channel, the flat-band can extend upto $\sim$ 4 GHz (Fig. 1(b)) with a flat-band loss of 19 dB as reported in [8] for a coupler separation of 0.8 mm. This flat-band loss is largely dependent on the coupler separation and increases with increase in the coupler separation. For example, being able to support $>$ 40dB flat band loss for mm-scale proximity communication will increase the range of these couplers by 10$\times$. Note that, as mentioned earlier, in traditional wireline links the speed limitation primarily comes from ISI and not from the integrated noise due to sufficiently small signal-attenuation. However, for the *lossy broad-band channels*, the maximum achievable data rate is often limited by noise and not by ISI as the typical speed of operation remains much lower than the bandwidth of the channel and the channels typically do not exhibit simple low-pass behaviour. For example, [20] achieves a data rate of 30 Mb/s for an HBC channel with $\sim$ 60 dB flat-band channel loss. Therefore, employing broad-band communication through *lossy broad-band channels*, calls for a new paradigm, analyzing, designing and finding the theoretical limits for wireline-like channels that are noise-limited, instead of ISI-limited. This work, for all the analysis and topology evolution, considers two key assumptions, namely i) the channel under consideration is flat-band from DC up to a high frequency (i.e., the channel loss is uniform throughout and it is not bandwidth limited) and ii) the flat-band channel loss is significantly high (20-100 dB) as opposed to the typical wireline channels. Although idealistic, these two assumptions make the analysis more general while ignoring the application-specific requirements and idiosyncratic channel characteristics. This paper goes through the derivation of new noise analysis of integrating-sampling receivers, proposal of new circuit topology (multi-integrating receiver, MIR) and a thorough design space exploration, including use of combination of wireless-inspired Low-noise amplifiers (LNA) with wireline-inspired strong-ARM latches and the newly proposed MIRs, utilizing a theoretical framework to demonstrate the optimum design choices for the above mentioned channel.

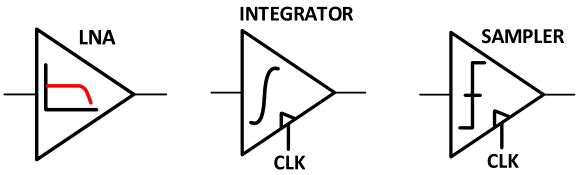
The **key contributions** of this work are as follows:

1) *Noise Theory for Strong-ARM + Integrator:* The work proposes a new procedure to find the input-referred noise of a strong-ARM latch and integrator theoretically, which is not available in any literature so far. Please refer to Section III-A for more details.
2) *Multi-Integrating Receivers (MIR):* The concept of cascading multiple integrators to improve the front-end gain with low power consumption along with detailed theoretical analysis, presented for the first time in literature, and can serve a very important role in any broad-band communication front-end where the flat-band channel loss is high. Such time-domain mixed-signal MIRs allow significant gain with much lower power than LNAs. An accurate expression for the gain of integrators has been derived and extended for multi-integrator cascades. Please refer to Sections III-C and III-D for further details.
3) *Optimum topology for Lossy Broad-band Channels:* An extensive theoretical analysis of noise, speed and power for various combinations of different signaling blocks, such as sampler, multiple integrators and LNA, has been carried out to find their suitability for high-loss broad-band channels. Both performance and power consumption of all the signaling blocks have been optimized for each data rate of operation and hence, given any particular channel loss and power budget, the user can easily choose any of the topology mentioned in this work. This design space exploration should not only serve for creating the theoretical basis for MIR but also should serve as a great place to start a design for designers working with *emerging* lossy broad-band channels.

Rest of the paper is organized as follows: Section II expounds different plausible RX topologies suitable for these kinds of channels. Section III deals with deriving closed-form equations and a rigorous performance analysis of different signaling blocks used in the RX topologies in terms of gain, integrated noise and power consumption. Section IV utilizes the analyses of Section III to find out the performance of different RX topologies with different channel loss followed by their comparison in Section V. Section VI concludes the paper.

II. RX TOPOLOGIES FOR LOSSY BROAD-BAND CHANNELS

The first important decision is the choice of a suitable signaling scheme for the type of channel assumed in this work. In current-mode signaling the driver output impedance is high, which is only possible when the pertaining driver or load transistors operate in saturation region. This limits the output voltage swing of the driver for current-mode signaling. Hence, in state-of-the-art high-speed links, current-mode signaling is adopted for very high data rate due to smaller signal swing which leads to small rise-time and fall time of the data. On the other hand, in voltage mode signaling the output impedance of the driver is very low and the driver/load devices typically operate in the triode region. Hence, a very large signal swing can easily be achieved in this type of signaling. As mentioned earlier, in any broad-band communication technique where the flat-band or low-frequency channel loss is sufficiently high ($>$ 20 dB), the transmitted signal gets highly attenuated while reaching the RX front-end. Hence, to maximize the swing of the transmitted signal, voltage mode signaling with rail-to-rail transmitted signal swing and a simple non-return to zero (NRZ) modulation scheme have been utilized in this work. Note that, for the ideal ISI-free lossy channel considered in this work, a simple non-return to zero (NRZ) modulation scheme is expected to



	LNA	INTEGRATOR	SAMPLER
Power Consumption	60 μW	20 μW	22 μW
Gain	10	5	-
i/p referred noise	80 μV	300 μV	300 μV

FIGURE 2. Different signaling blocks, required in the RX front-end for NRZ communication through lossy broad-band channels. Typical simulated performance of each block is shown for a 1 V supply in 65 nm CMOS technology. The numbers are obtained by optimally sizing the transistors in each block for a band-width of 1 GHz and using a load capacitor of 10 fF.

show superior BER performance over multi-level schemes such as four-level pulse amplitude modulation (PAM-4), duobinary etc. In the applications mentioned earlier, integrating front-end has been utilized for serving specific purposes associated with the particular type of channel, i.e., to deal with self-resonance frequency (SRF) in proximity communication [8] and cancelling environmental interference in human-body communication [11]. However, the fact that *current-integrating amplifiers* or *integrators* can be utilized as gain elements with sufficiently lower power consumption, remains relatively unexplored in literature with a dearth of closed-form equations capturing the same. Charge-steering logic based front-ends [31] have been explored as low-power alternatives to integrating front-ends. However, the higher gain provided by integrating front-ends as compared to the charge-steering front-ends makes it more suitable for lossy broadband applications.

In NRZ communication, a sampler or clocked comparator serves as the simplest RX. However, for practical samplers (e.g., a strongARM latch [32]) the maximum sampling frequency depends on the input signal swing which decreases with increase in channel loss. Also, for applications with very high channel loss, the signal may become comparable with the input-referred noise of the sampler and can degrade the bit-error rate (BER) drastically. A low-noise amplifier (LNA) can be used before the sampler which serves two important purposes, i.e., it amplifies the RX input signal and exhibits significantly lower input-referred noise. However, being a continuous time amplifier its power consumption is large and increases linearly with the required bandwidth. A *current-integrating amplifier* [33], [34], [35], on the other hand can provide gain comparable to an LNA with lower power consumption but at the cost of relatively higher input-referred noise.

Fig. 2 summarizes the typical performance of all these blocks (in 65 nm CMOS) in terms of gain, input-referred noise and power consumption for 1 Gbps data rate (i.e., 1 GHz clock frequency). Various RX front-end topology based on these three key signaling blocks are shown in Fig. 3 with the sampler as a mandatory part in each topology. In the following discussion, a detailed analyses for all these signaling blocks are done and the next section delineates the optimum performance of each topology for different channel losses. For each individual signaling block, an additional $5fF$ load capacitance has been conservatively added to account for the metal routing parasitic capacitance.

A. SAMPLER OR CLOCKED COMPARATOR

StrongARM latch is the most common type of sampler widely used in different applications including wireline receivers, analog-to-digital converters and memory bit-line detectors. The reason for its widespread popularity is zero static power consumption and rail-to-rail output swing. A double-tail latch type SA [36] is another alternative to the strongARM latch which also shows similar behavior with added degree of freedom for better optimization. Charge-steering latches [31] on the other hand, although more power efficient than the above mentioned latches, produce low-swing output signals and hence, need to be followed either by a strongARM latch or a double-tail latch type SA to produce rail-to-rail output. In this work a strongARM latch has been used as the sampler.

The strongARM latch shown in Fig. 4 has four phases of operation [37]. In the reset phase (phase-I), CLK is low and nodes P, Q, X and Y are pre-charged to V_{DD}. When CLK goes high, amplification phase begins and the input differential voltage at the inputs of M_1 and M_2 gets converted to differential drain current which is integrated at the parasitic capacitances at nodes P and Q amplifying the input signal until V_P and V_Q drop to $V_{DD}-V_{THN}$ (Fig. 5(a)). At this point M_3 and M_4 are turned on, output nodes X, Y start discharging and the circuit enters into the third phase with continuing amplification by M_1 and M_2 and a little regenerative gain provided by M_3 and M_4. The final regeneration phase begins when nodes X and Y drop below $V_{DD}-V_{THP}$ turning M_5 and M_6 on. To understand the timing performance of the strongARM latch for applications with high channel loss where input differential voltage can be quite small, one must carefully consider the dependencies of duration of each phase over the input voltage and also the total input-referred noise of the strongARM latch.

1) TRANSIENT PERFORMANCE (LATCHING TIME CONSIDERATION)

Fig. 5(a) shows the transient behaviour of the strongARM latch in the sensing phase (i.e., when CLK becomes high). From the analyses in [38] and [39], duration of different phases can be expressed as

$$t_a = \frac{2C_{P,Q}V_{TH3,4}}{I_O} \tag{1}$$

$$t_o = \frac{2C_{X,Y}V_{TH5,6}}{I_O} \tag{2}$$

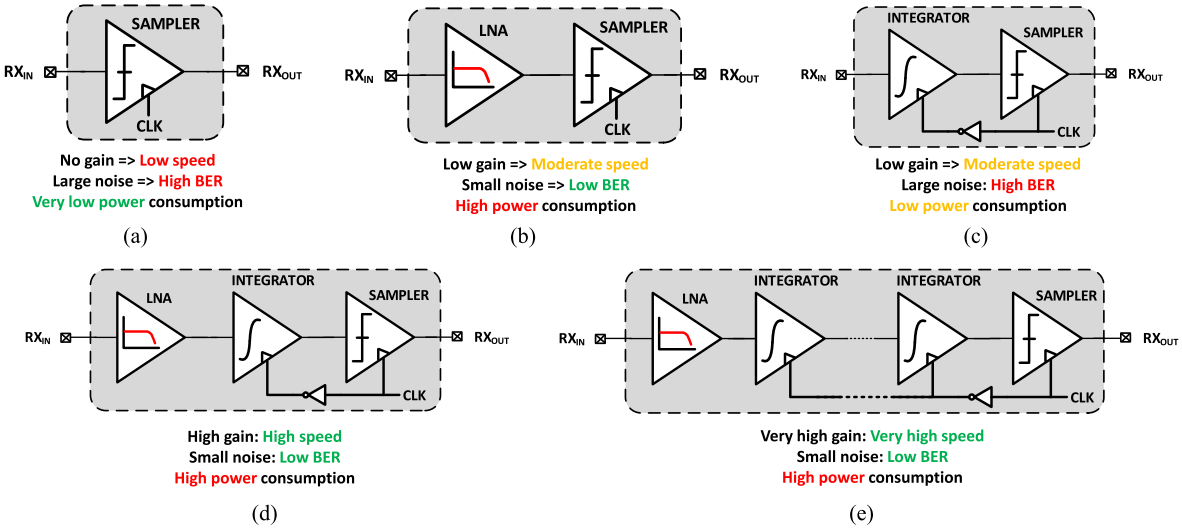


FIGURE 3. Different possible topologies of the RX front-end based on signaling blocks shown in Fig. 2: (a) Only sampler, (b) LNA + sampler, (c) integrator + sampler, (d) LNA + integrator + sampler, (e) LNA + multi-integrator cascade + sampler (MIR).

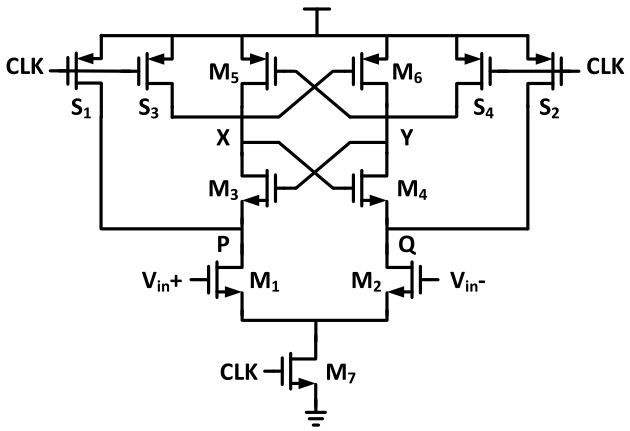


FIGURE 4. Widely used strongARM latch topology [37].

$$t_{latch} = \frac{C_{X,Y}}{g_{m,latch}} \ln\left(\frac{1}{V_{TH5,6}}\sqrt{\frac{I_O}{2\beta}}\frac{\Delta V_{latch}}{\Delta V_{IN}}\right) \tag{3}$$

where $I_O(= g_{m1,2}V_{ov1,2}/2)$ is the quiescent current provided by M_7 once CLK goes high, $g_{m,latch}$ is the sum of the transconductances of M_3 and M_5 in the regeneration or latching phase (i.e., phase-III), β is the transconductance parameter of M_1 and M_2 and ΔV_{IN} is the input differential voltage to the strongARM latch. Note that the regeneration phase is characterized by t_{latch} which in turn is governed by ΔV_{latch} as shown in [38]. The output of the strongARM latch is converted to NRZ data using a D-flip-flop which demands close to rail-to-rail input signal swing for proper operation. As there is no closed-form expression for the exact settling time of a strongARM latch, a spice-simulation based approach is adopted to find the minimum clock frequency. Fig. 6 shows the ratio of the 10% output settling time, (t_{settle}) and $(t_a + t_o + t_{latch})$ for different input voltages. Although this ratio is smaller than 2 in typical process corner, the ratio

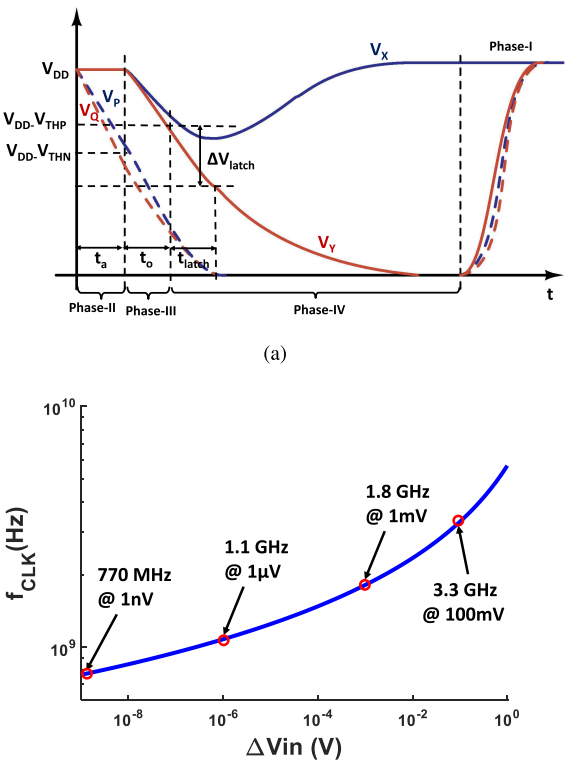


FIGURE 5. (a) Transient behaviour of a strongARM latch in the sensing phase (i.e., phase-II,III and IV) showing the transition between different phases of operation, (b) Variation of the maximum operation frequency of strongARM latch with input voltage.

increases in ss-corner due to slow transistors. Also, the output needs to be settled at-least before the setup time of the D-flip-flop for avoiding any metastability issue. Considering this fact, duration of phase-(II+III+IV) is conservatively chosen to be $3 \times (t_a + t_o + t_{latch})$ which gives the minimum time

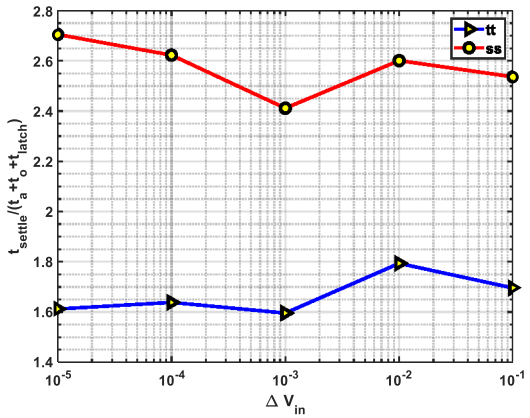


FIGURE 6. Variation of the relative settling time of the strongARM latch with input voltage for tt and ss process corners.

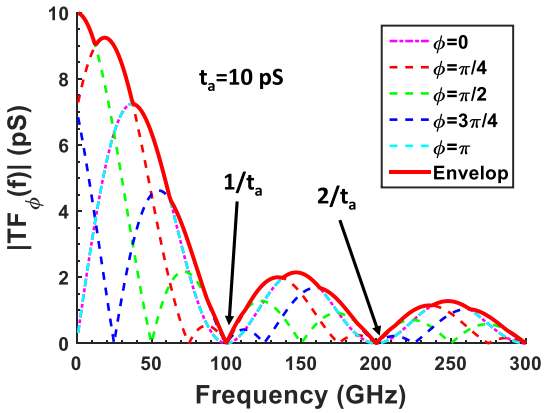


FIGURE 7. Plot of the function $TF_\phi(f)$ which shapes the noise spectrum in strongARM latch. In this case, the envelop is shown considering only 5 different values of ϕ.

period of *CLK* to be

$$T_{CLK,min} = \frac{1}{f_{CLK,max}} = 6(t_a + t_o + t_{latch}) \tag{4}$$

From eq. (3), it can be seen that as the input differential voltage ΔV_{IN} reduces, the maximum operating frequency of the strongARM latch decreases logarithmically. Fig. 5(b) shows the variation of maximum operating frequency ($f_{CLK,max}$) with ΔV_{IN} obtained by extracting all the parameters in eq. (1)-(3) for a typical design in 65 nm CMOS technology. As can be seen, for very small ΔV_{IN} ($\approx$ 1 nV), $f_{CLK,max}$ can be as small as 0.8 GHz and for larger ΔV_{IN} ($\approx$ 100 mV), the value reaches up to 3.3 GHz. From Fig. 5(b), it may seem that with signal amplitude of even a few μV, the strongARM latch can be operated at a speed close to 1 GHz, but practically for sub-mV signal swing, final decision will be significantly affected by the internal noise of strongARM latch. Hence, it is important to find out the total input-referred noise which is addressed in the following subsection.

2) NOISE PERFORMANCE (SNR CONSIDERATION)

It is interesting to note that in the reset phase, the pre-charge action of the switches ($S_1 - S_4$) nullifies effect of all the noise contributed by different transistors. It is when the *CLK* goes high, that the noise contributions of different transistors come into picture. Moreover, most of the input-referred noise originates from M_1 and M_2 in the amplification phase [39] because all other transistors start acting after phase-II when a significant gain has already accrued between nodes P and Q which then gets regenerated in rest of the phases. Hence, the input-referred noise of strongARM latch would be simply the output referred noise at the end of amplification phase divided by the gain of the amplification phase given by $g_{m1,2}t_a/C_{P,Q}$. In [40], a stochastic analysis of this noise has been done. Here we show a time domain analysis based on the *ergodicity property* of thermal noise.

Note that in the amplification phase, as M_3 and M_4 are turned off, strongARM latch behaves like an integrator, integrating the drain currents of M_1 and M_2 over the parasitic capacitance C_P and C_Q at nodes P and Q respectively. Hence, assuming the output resistance at nodes P, Q to be very large, the final differential output referred noise at the end of the amplification phase can be found by integrating the differential channel noise current i_n (whose $PSD = 8KT\gamma g_{m1,2}$) of M_1 and M_2 for a duration of t_a. This gives the final noise voltage to be

$$V_{n,O} = \frac{1}{C_{P,Q}} \int_0^{t_a} i_n(t)dt \tag{5}$$

To evaluate this integral, let us first assume $i_n(t)$ to be a *sine* wave with amplitude A, frequency f and initial phase ϕ, i.e., $i_n(t) = Asin(2\pi ft + \phi)$. For this simplest scenario, $V_{n,O}$ can be found out to be

$$V_{n,O} = \frac{A(cos(\phi) - cos(2\pi ft_a + \phi))}{2\pi fC_{P,Q}} = \frac{A}{C_{P,Q}}.TF_\phi(f) \tag{6}$$

From eq. (6), it can be seen that if $i_n(t)$ be a sinusoid with frequency f and initial phase ϕ, result of the integral in eq. (5) would be $TF_\phi(f)$ times its amplitude. But in reality, $i_n(t)$ in the time interval 0 to t_a, contains all the frequency components and hence different frequency components would have different multiplication factor depending on their initial phases. Hence, the final noise voltage can be found by summing the contributions of all the frequencies present in $i_n(t)$. Fig. 7 shows the plot of $TF_\phi(f)$ for 5 different values of ϕ. The rms value of the component of $i_n(t)$ obtained by passing it through a band-pass filter of bandwidth Δf centered around frequency f can be given by $\sqrt{8KT\gamma g_{m1,2}\Delta f}$. But as the initial phase corresponding to this component at frequency f can eventually be anything, by pessimistic assumption we can consider the multiplication factor to be $max(TF_\phi(f) : \phi\epsilon[0 : 2\pi])$ which is essentially the envelop ($TF_{env}(f)$) of all the curves governed by different ϕ. Hence, considering the noise contribution of all the components in i_n, the final rms noise voltage square ($V^2_{n,O}$) can be expressed as

$$V^2_{n,O} = \sum_f \left(\frac{\sqrt{8KT\gamma g_{m1,2}\Delta f}}{C_{P,Q}} \times TF_{env}(f) \right)^2$$

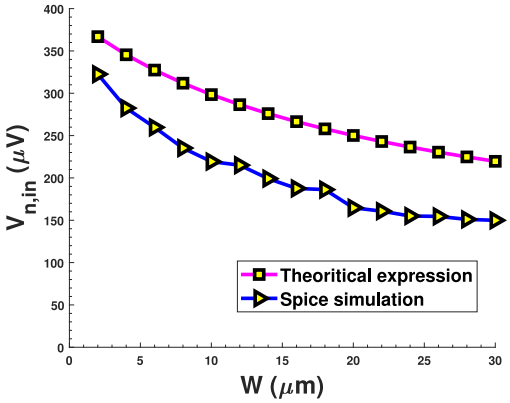


FIGURE 8. Variation of input-referred noise of strongARM latch for different widths of M_1 and M_2. Noise is calculated both from the theory (eq. 10) and from spice simulation following the method in [39].

$$= \frac{8KT\gamma g_{m1,2}}{C_{P,Q}^2} \times \int_0^\infty TF_{env}^2(f)df \tag{7}$$

Hence, the input-referred noise can be given by

$$V_{n,in}^2 = V_{n,in}^2 / \left(\frac{g_{m1,2}t_a}{C_{P,Q}}\right)^2 = \frac{8KT\gamma}{g_{m1,2}t_a^2} \times \int_0^\infty TF_{env}^2(f)df \tag{8}$$

The integral in eq. (8) can be numerically evaluated to be $t_a/2$ which gives the final input-referred noise expression as

$$V_{n,in}^2 = \frac{4KT\gamma}{g_{m1,2}t_a} \tag{9}$$

which exactly matches with the stochastic analysis result in [40]. Moreover, on replacing t_a with (1) and substituting the value of I_O one gets the expression for input-referred noise as

$$V_{n,in}^2 = M\frac{KT}{C_{P,Q}} \tag{10}$$

where $M = \gamma V_{TH3,4}/V_{ov1,2}$. Note that, the noise term has an usual KT/C-form with an additional factor-M. To validate this theory, input-referred noise of strongARM latch has been obtained in spice simulation following the method described in [39]. Fig. 8 compares the spice result with the theoretical expression plotted by extracting transistor parameters in 65 nm CMOS.

B. LOW NOISE AMPLIFIER

As mentioned in Section II, a low noise amplifier serves two important purposes: i) it provides a gain to the inbound signal and ii) offers much lower input-referred noise. The most commonly used broadband topology of a low-noise amplifier (LNA) is shown in Fig. 9 where R_B is a large resistor (realized by off-transistor in this case). The mid-band gain of this LNA can be given by

$$A_{LNA} = (g_{m1} + g_{m2})(r_{o1}||r_{o2}) \tag{11}$$

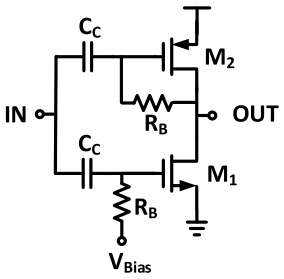


FIGURE 9. Circuit diagram of low noise amplifier with self-biased load.

where $g_{m1,2}$ is the transconductance of $M_{1,2}$ and $r_{o1,2}$ is its drain to source resistance. Hence the gain of the LNA is solely determined by the intrinsic gains of transistors M_1 and M_2. Also, the input-referred noise of this LNA can be expressed as

$$V_{n,in,LNA} = \sqrt{\frac{4KT\gamma}{g_{m1} + g_{m2}} \times B} \tag{12}$$

where B is the bandwidth of the LNA which depends on the bias current (I_{bias}) and effective load capacitance. Note that the bandwidth requirement of the LNA comes from the input data rate, i.e., the bandwidth of the LNA should be larger than or equal to the data rate to avoid any signal distortion causing inter-symbol interference (ISI). For the analysis in Fig. 10 a typical design setup in 65 nm CMOS is used where sizes of the transistors are kept constant (width of M_1 is 24 μm and that of M_2 is 48 μm) and an additional load capacitance (C_L) of $5fF$ (apart from the $5fF$ capacitance of the metal parasitics) has been used to account for the loading offered by the subsequent stage (i.e., an integrator or a strongARM latch). Fig. 10(a) shows the minimum I_{bias} required for the LNA as a function of its bandwidth. It is important to note that as the bandwidth requirement of the LNA goes down, operating region of the transistors moves from above-V_T to weak inversion and finally to depletion region. And hence, the power consumption goes down more-or-less linearly with reduction in target bandwidth. Fig. 10(b) shows the variation of the mid-band gain of the LNA with bandwidth, assuming the minimum bias current in the LNA for each target bandwidth. Note that for target bandwidths where transistors are in above-V_T region of operation, gain increases with reduction in bias current as g_m is proportional to $\sqrt{I_{bias}}$ and r_o is inversely proportional to I_{bias} in this region. When the transistors go to weak inversion, g_m becomes proportional to I_{bias} and hence, the gain remains almost constant. Finally, in the depletion region gain falls with reduction in current as r_o becomes comparable to R_B. On the other hand, the input-referred noise (in Fig. 10(c)) behaves exactly the opposite to the gain, for different target bandwidths, as expected from the noise expression in eq. (12). On comparing the noise performance of strongARM latch in Fig. 8 to that of the LNA in Fig. 10(c), it can be observed that the LNA has significantly lower input-referred noise. This, together with the gain plot in Fig. 10(b) substantiate the use

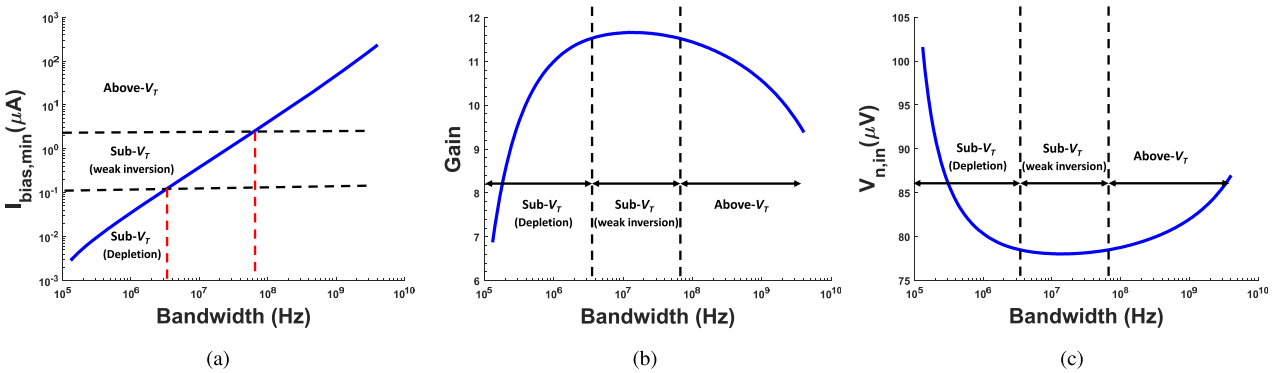


FIGURE 10. (a) Minimum bias current required for the LNA in Fig. 9 for different target bandwidths (b) gain of the LNA for different target bandwidths with minimum bias current (c) input-referred noise of the LNA for different target bandwidths with minimum bias current.

of the LNA before the sampler for achieving higher data rate in applications with high channel loss.

Note that one inherent drawback of using this single-ended LNA topology is the weak power supply rejection. The LNA used in this work shows a power supply gain of 15 dB. The power-supply rejection, however, can be improved by adopting some other suitable LNA topology.

C. INTEGRATING AMPLIFIER OR INTEGRATOR

An integrating amplifier can be used in the RX front-end to provide gain to the received signal before sampling with significantly lower power consumption than an LNA. Fig. 11(a) shows the circuit diagram of the integrator which utilizes pre-charging loads [33]. When *CLK* is low, the PMOS switches are on, which pre-charge the output nodes to V_{DD}. As *CLK* goes high, the output nodes start discharging and depending on the input voltage difference, a finite voltage difference is created between the output nodes which is then sampled by the sampler at the end of integration period. Assuming large output resistance, the ratio of the output and input voltage difference or the voltage gain of the integrator can be expressed as

$$A_{int} = \frac{g_{m1,2}T_{int}}{C_L} \tag{13}$$

where $g_{m1,2}$ is the transconductance of $M_{1,2}$, T_{int} is the period of integration which equals to half of the clock period and C_L is the equivalent load capacitor at the output nodes. Note that the integrator senses the input data only in the integration phase and hence, for clock frequency same as the data rate, the integrator integrates the input data for only half the bit-period. However, an half-rate topology [33] can be used where two parallel integrators work on complementary clock signals with clock frequency as half the data rate.

It is important to observe that as the integrator output is fed to the sampler realized by a strongARM latch, the common mode voltage of the output nodes at the end of integration phase should be high enough for proper operation of the strongARM latch. Reference [38] shows that $0.7V_{DD}$ is the optimum input common mode voltage for the strongARM latch in terms of speed and yield. However, for

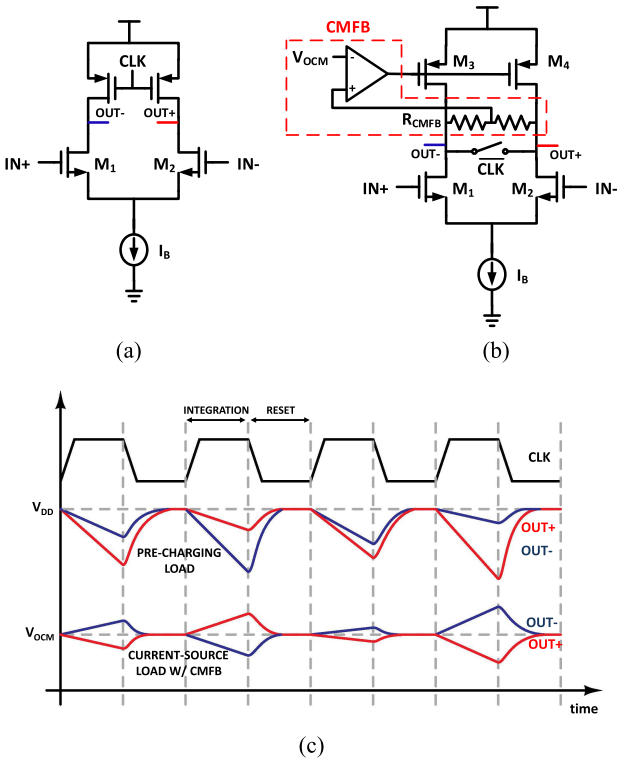


FIGURE 11. (a) Integrator based on pre-charging load [33], (b) modified integrator based on current-source load with common-mode feedback [35], (c) comparison of output waveform for both the integrators. Output common-mode voltage of the one with pre-charging loads keeps on decreasing, whereas the other one has a constant common-mode voltage.

65 nm CMOS, we found that the input common mode voltage can go down to $\sim 0.6V_{DD}$ without degrading the speed and yield significantly. With this observation, the maximum bias current ($I_{B,max}$) in the integrator for $V_{DD} = 1$V can be expressed as

$$I_{B,max} = \frac{(0.4V_{DD})(2C_L)}{T_{int}} = \frac{0.8C_L}{T_{int}} \tag{14}$$

Fig. 12 shows the variation of $I_{B,max}$ with clock frequency for $C_L = 4$ fF, which gives $I_{B,max} \approx 20\mu$A for a 1 GHz

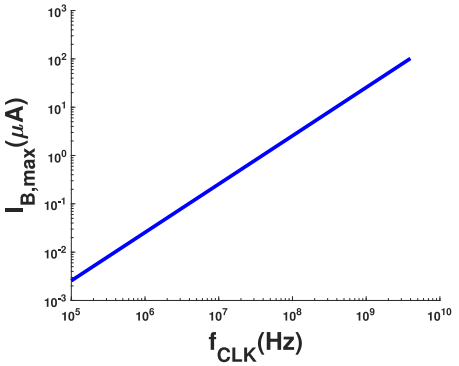


FIGURE 12. Variation of the maximum allowable current of the integrator in Fig. 11 with clock frequency.

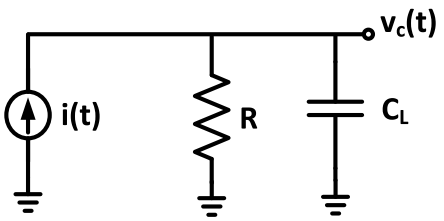


FIGURE 13. Equivalent circuit of the integrator (shown in Fig. 11 (a,b)) in the integration phase.

clock frequency. The common-mode droop problem associated with the integrator in Fig. 11(a) is handled in [41] by a separate common-mode boosting circuit using capacitive coupling, whereas [42] addresses the same by adding a common-mode current during the integration phase. In [35] the output common-mode voltage is kept constant by using current-source loads and a common-mode feedback (CMFB) circuit as shown in Fig. 11(b). The corresponding output waveform is shown in Fig. 11(c).

From the gain expression in eq. (13) it might seem that the gain of the integrator in Fig. 11(a) can go very large for lower clock frequency as $g_{m1,2} \propto \sqrt{I_{B,max}}$ and $T_{int} \propto 1/I_{B,max}$. But practically, the gain will be different from that given by eq. (13) due to the presence of finite output resistance of the integrator. In the following portion, we derive an accurate expression for the gain of the integrator considering the drain to source resistance of $M_{1,2}$ in the integration phase.

In the integration phase, the circuit in Fig. 11(a) can be simplified as shown in Fig. 13, where $i(t) = g_{m1,2}v_{in}$, R is the drain to source resistance of $M_{1,2}$ and C_L is the load capacitance at the output nodes. Now, from Kirchoff's current law, we can write

$$i(t) = \frac{v_c(t)}{R} + C_L\frac{dv_c(t)}{dt} \tag{15}$$

on solving this differential equation and applying the initial pre-charge condition $v_c(0) = 0$, we can write

$$v_c(t) = \frac{e^{t/RC_L}}{C_L}\int_0^t e^{\tau/RC_L} i(\tau)d\tau \tag{16}$$

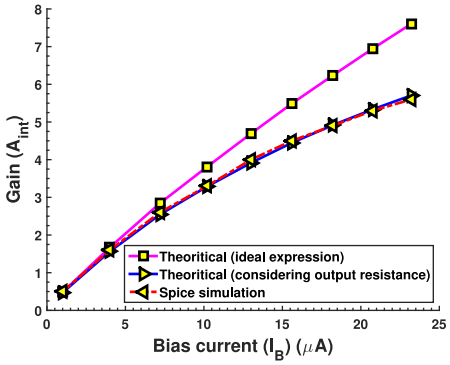


FIGURE 14. Variation of integrator gain with bias current for f_{CLK} = 1 GHz. Note that, the plot obtained from the modified expression in eq. (17) exactly matches with that obtained from spice simulation.

finally substituting $i(\tau)$ with $g_{m1,2}v_{in}$ we can express the gain as

$$A_{int} = \frac{v_c(T_{int})}{v_{in}} = g_{m1,2}R\left(1 - e^{-T_{int}/RC_L}\right) \tag{17}$$

Note that if $T_{int} << RC_L$, expression in eq. (17) matches to the ideal gain expression in eq. (13). Fig. 14 compares the integrator gain obtained from the ideal (eq. (13)) and modified (eq. (17)) expressions to that obtained from spice simulation, for a clock frequency (f_{CLK}) of 1 GHz. It can be seen, there is an excellent match between the modified theoretical expression and spice simulation. Note from Fig. 14 that, as the bias current I_B reduces for a fixed T_{int}, value of R increases (as $R \propto 1/I_B$) and hence the two gain expressions give same results for very low I_B. Now, for a particular f_{CLK}, as the gain increases with I_B, the maximum gain can be achieved with $I_B = I_{B,max}$ given by eq. (14). Also, considering the fact that $R = \frac{2}{\lambda I_B}$ (λ being the channel length modulation parameter) for $I_B = I_{B,max}$ eq. (17) becomes

$$A_{int,max} = g_{m1,2}R\left(1 - e^{-0.4\lambda}\right) \tag{18}$$

Hence, it can be concluded that the maximum gain of the integrator in Fig. 11(a) for a particular clock frequency (f_{CLK}), is mostly governed by the intrinsic gain of the transistors $M_{1,2}$ and it can not be made very high for lower clock frequencies. Fig. 15 shows the variation of the maximum gain ($A_{int,max}$) with clock frequency. Note that, the difference in gains of the integrators with pre-charging load (Fig. 11(a)) and current-source load (Fig. 11(b)) arises from the difference in their output resistances (R). For the same bias current, I_B, the output resistance of the latter one is half of the output resistance of the former assuming the same channel-length modulation parameter (λ) for both PMOS and NMOS devices. This results in a lower gain for the current-source load based integrator compared to the former for the same bias current. Also, as the output common-mode voltage of the current-source load based integrator is constant, the bias current doesn't impose any constraint over the maximum achievable gain. However, note from eq. (17) that the maximum achievable gain for the current-source based

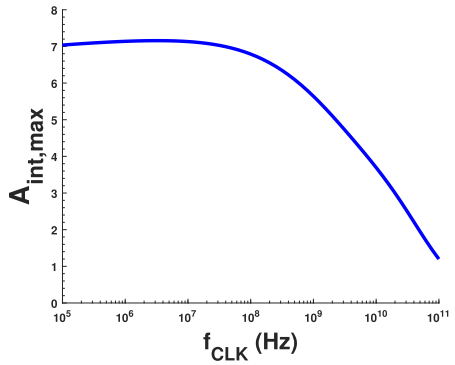


FIGURE 15. Variation of the maximum gain of the integrator with clock frequency. As the maximum gain is mainly governed by the intrinsic gain of the transistors (eq. (18)), it saturates for lower clock frequencies as the transistors enter into sub-threshold regime.

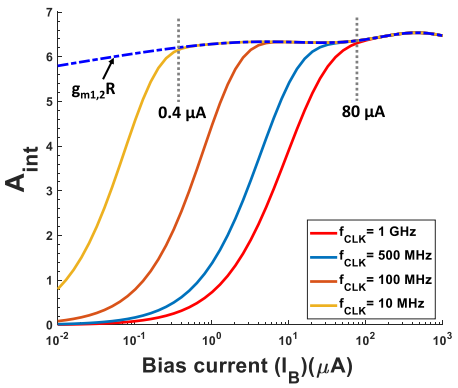


FIGURE 16. Variation of gain of the current-source load based integrator for different clock frequencies.

integrator for a fixed T_{int} (and hence fixed f_{CLK}) can not exceed $g_{m1,2}R$ which is half of the intrinsic gain of $M_{1,2}$. Fig. 16 shows the variation of the gain of the current-source load based integrator with bias current, I_B for different clock frequencies (f_{CLK}). As it can be seen, the gain increases with increase in I_B and finally converges with $g_{m1,2}R$. Also, the minimum I_B required to converge with $g_{m1,2}R$ decreases with decrease in f_{CLK}.

Coming to the noise performance of the integrator, note that the theory of input-referred noise described in Section III-A2 directly applies to the integrator in Fig. 11(a) with t_a being replaced by T_{int}. Hence, the input-referred noise of the integrator with pre-charging load can be given as

$$V_{n,in} = \sqrt{\frac{4KT\gamma}{g_{m1,2}T_{int}}} \tag{19}$$

However, for the current-source load based integrator, the PMOS current sources M_3 and M_4 will also contribute to the input-referred noise and it can be shown that the overall input-referred noise in this case can be expressed as

$$V_{n,in} = \sqrt{\frac{4KT\gamma}{g_{m1,2}T_{int}}\left(1 + \frac{g_{m3,4}}{g_{m1,2}}\right)} \tag{20}$$

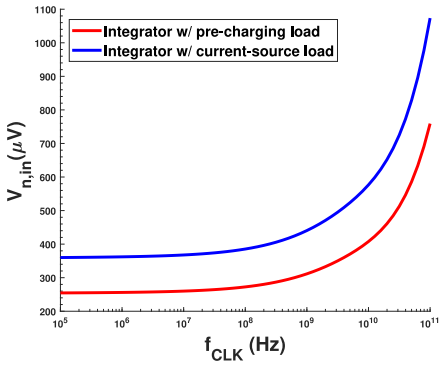


FIGURE 17. Variation of the input-referred noise of the integrator with clock frequency.

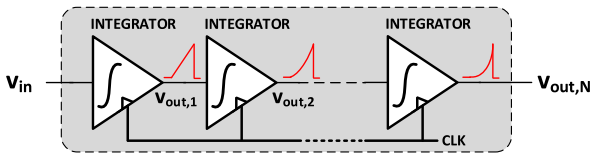


FIGURE 18. Cascading multiple integrators to improve the gain.

Fig. 17 shows the variation of $V_{n,in}$ with clock frequency for both type of integrators. Finally, it can be concluded that performance of the pre-charging load based integrator is superior to that of the current-source based integrator in terms of gain, noise performance and power consumption. However, applications where the data rate (and hence the clock frequency) varies widely making a stable output common-mode voltage of the integrator an absolute necessity, the current-source based integrator turns out to be more effective. In all other practical applications, the pre-charging load based integrator gives superior performance. In this work, the pre-charging load based integrator has been used to analyze the performance of all the RX topologies.

D. MULTI-INTEGRATOR CASCADE: CASCADING MULTIPLE INTEGRATORS

As already seen, a single integrator can typically provide a gain ranging from $4.5 - 7$ for all frequencies of operation. It will be interesting to see whether the gain can be further enhanced by cascading multiple integrators operating with the same clock signal as shown in Fig. 18. To understand the behavior of the cascaded integrators in Fig. 18, let us for the time being ignore the effect of the output resistance. Hence output of the first integrator and the gain can be given by

$$v_{out,1}(t) = \int_0^t K_i v_{in} dt = K_i v_{in} t \tag{21}$$

$$A_{int,1} = K_i T_{int} \tag{22}$$

where $K_i = g_{m1,2}/C_L$. Similarly, output of the second stage and the combined gain of 2 cascaded integrators can be expressed as

$$v_{out,2}(t) = \int_0^t K_i (K_i v_{in} t) dt = \frac{K_i^2 v_{in} t^2}{2} \tag{23}$$

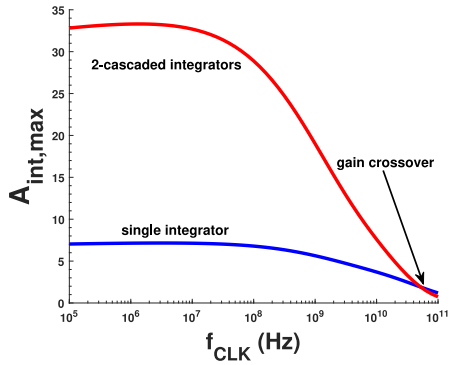


FIGURE 19. Gain improvement with 2 cascaded integrators over a single integrator.

$$A_{int,2} = \frac{K_i^2 T_{int}^2}{2} = A_{int,1} \times \frac{K_i T_{int}}{2} \tag{24}$$

Hence, from eq. (24) it can be observed that in order that gain of 2 cascaded integrators ($A_{int,2}$) be larger than that of a single integrator, gain of a single integrator ($= K_i T_{int}$) must be greater than 2. Proceeding in the same way it can be shown that the overall gain of N-cascaded integrators would be

$$A_{int,N} = \frac{K_i^N T_{int}^N}{N!} = A_{int,N-1} \times \frac{K_i T_{int}}{N} \tag{25}$$

This is an important result which shows that for a fixed clock frequency (or, equivalently fixed T_{int}) and with single integrator gain A, cascading $[A]$ (box of A) many integrators results in maximum overall gain and the gain starts falling on cascading integrators further. Now, considering the effect of the output resistance of the integrator, using eq. (16) the overall gain of 2 cascaded integrators can be expressed as

$$A_{int,2} = \left(g_{m1,2}R\right)^2 \left(1 - \left(1 + \frac{T_{int}}{RC_L}\right) e^{-T_{int}/RC_L}\right) \tag{26}$$

which again matches the expression in eq. (24) if $T_{int} << RC_L$. Similarly, for a 3-integer cascade the actual gain expression can be given as

$$A_{int,3} = \left(g_{m1,2}R\right)^3 \times \left(1 - \left(1 + \frac{T_{int}}{RC_L} + \frac{1}{2}\left(\frac{T_{int}}{RC_L}\right)^2\right) e^{-T_{int}/RC_L}\right) \tag{27}$$

In general, it can be mathematically proven that the overall gain of an N-integrator cascade can be expressed as

$$A_{int,N} = \left(g_{m1,2}R\right)^N \left(1 - T_N\left(\frac{T_{int}}{RC_L}\right) e^{-T_{int}/RC_L}\right) \tag{28}$$

where

$$T_N(x) = 1 + x + \frac{x^2}{2} + \cdots + \frac{x^{N-1}}{(N-1)!} \tag{29}$$

Fig. 19 shows the gain improvement of the front-end on cascading 2 integrators. Note the gain crossover at high-frequency which indicates that after a certain frequency,

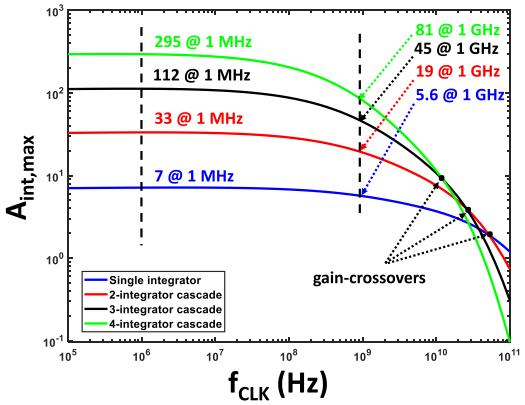


FIGURE 20. Comparison of the gain provided by an N-integrator cascade for $N = 1, 2, 3, 4$.

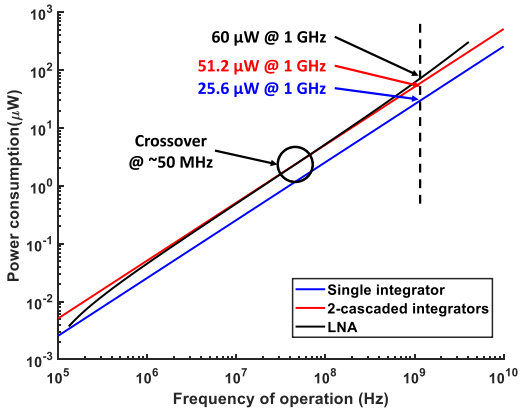


FIGURE 21. Comparison of power-consumption between LNA and integrator. The power numbers are obtained for a 1 V supply voltage. For the single and 2-cascaded integrators, the power numbers correspond to their maximum possible bias current (which also maximizes the gain) and for the LNA the power number corresponds to the minimum required bias current to achieve the specified bandwidth denoted by the frequency of operation.

single-integrator proves to be a better choice than 2-cascaded integrators considering both gain and power aspects. Fig. 20 compares the gains of N-integrator cascades for $N = 1, 2, 3, 4$ in log-scale. By cascading 4 integrators, a gain of as high as 295 can be achieved at lower operating frequencies. However, there is a significant difference in magnitudes of the gains obtained at lower frequency regions and at higher frequency regions. Also, as one increases the number of integrator stages, the gain-crossover frequency between subsequent multi-integrator cascades reduces as it is evident from Fig. 20. The power consumption of the single and 2-integrator topologies are compared with the LNA power consumption in Fig. 21. Although at higher operating frequencies, the 2-integrator cascade is a low power option than the LNA, however, for a frequency of operation < 50 MHz, LNA power consumption becomes smaller than the 2-integrator cascade. Nonetheless, the significantly larger gain provided by the 2-integrator cascade makes it a better option than the LNA for applications requiring large front-end gain.

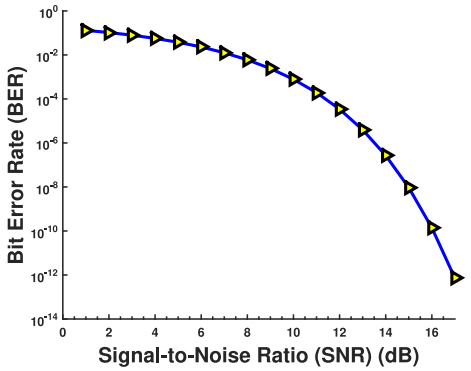


FIGURE 22. Variation of bit-error rate (BER) with signal-to-noise ratio (SNR) for NRZ communication.

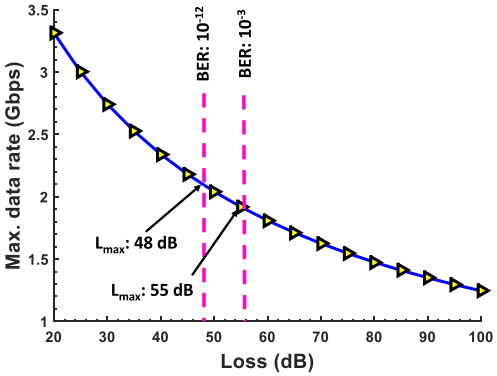


FIGURE 23. Variation of maximum data rate with channel loss for topology-1.

III. PERFORMANCE OF DIFFERENT TOPOLOGIES FOR LOSSY BROADBAND CHANNELS

Based on the detailed analyses of different signaling blocks in the previous section, we are now in a position to compare the performance of each topology in Fig. 3 for different channel loss. In the performance analysis of different topologies, a full rate RX topology has been assumed where the clock frequency is the same as the data rate. Moreover, signal inputs are assumed to be single ended for all the topologies. The input configuration for topology-I and III are similar to that in [20] where the input signal is ac-coupled to one of the input ports of the sampler (for topology-I) or the integrator (for topology-III), while the common-mode voltages of both the input ports are set using a voltage-DAC and resistor combination. For topology-II and topology-IV, the output of the LNA is coupled to the sampler and integrator respectively in a similar fashion. The methodology adopted to find the maximum achievable data rate of each topology as a function of the channel loss is delineated below.

For any particular topology, as the channel loss (L) increases, the input signal swing to the RX ($v_{RX}(L)$) reduces. Let $A_{FE}(f)$ be the gain of the RX front-end (this gain excludes the strongARM latch) which depends on the operating-frequency f (or, equivalently the data rate). Then, the input voltage of the sampler is given by, $v_{SAL}(f, L) = A_{FE}(f)v_{RX}(L)$. Note that for topology-I (the sampler-only topology), $A_{FE}(f) = 1$. Now, if g be the function which maps the input voltage of the strongARM latch (v_{SAL}) to its maximum operating frequency (Fig. 5(b)), then a data rate f is achievable by an topology *iff* $g(A_{FE}(f)v_{RX}(L)) \geq f$. Hence, the maximum achievable data rate (f_{max}) for an topology corresponding to a channel loss L for which the above-mentioned equality holds, i.e., $g(A_{FE}(f_{max})v_{RX}(L)) = f_{max}$. This gives the gain-constraint curve of the maximum achievable data rate as a function of channel loss L. Note that, in this methodology, noise of the front-end has not been considered. However, with reduction in the input signal swing of RX, the input signal-to-noise ratio (SNR) reduces which in turns degrade the bit-error rate (BER) of the final received data. It is important to understand the noise/BER constraint on the maximum achievable data rate. For a given channel loss, L, the input signal swing (v_{RX}) can be found simply by dividing the transmitted signal swing by L. Hence, for a given L and a target SNR (or target BER), there is a specific value of the total input-referred noise (say $v_{n,L}$) which meets the target SNR. Now, for almost all the RX topologies (except topology-1) discussed here, the input-referred noise is a function of the operating frequency (or bandwidth). Hence, one can find an operating frequency, f_n for which the RX input-referred noise will be exactly equal to $v_{n,L}$. Also, Fig. 10(c) and Fig. 17 indicate that at higher operating frequencies, the input-referred noise increases with frequency. Hence, f_n denotes the maximum operating frequency the RX can support for a given channel loss L while satisfying the target SNR/BER. This gives the BER-constraint curve for a RX topology as a function of channel loss, L. Now, the maximum achievable data rate for a RX topology can be obtained from the combination of the gain constraint curve and the BER constraint curve. Fig. 22 shows the BER vs SNR plot for NRZ communication. For wireline applications, a target BER of 10^{-12} is generally used and for mm-wave (or in general wireless) applications the preferred target BER is 10^{-3} considering the large loss of wireless channel. However, for wireline-like channels any target BER in this range can be chosen depending on the application and the value of channel loss. In the following performance analysis, while calculating the energy efficiency of different RX topologies, power consumed by the clock generation circuits and biasing circuits has not been included for simplicity and to focus on the Rx topology dependent power.

A. TOPOLOGY I: ONLY SAMPLER

Assuming a 1 V transmitted signal swing, the input signal swing of the RX (v_{RX}) can be computed as a function of the channel loss, L and maximum achievable data rate for that particular channel loss can be found following the methodology discussed earlier. Fig. 23 shows the corresponding plot. Note that, $A_{FE}(f) = 1$ for topology-I. Also, as the channel loss increases, the input SNR reduces which degrades the BER of the received signal. As the input-referred noise of topology-I is constant and not a function of frequency,

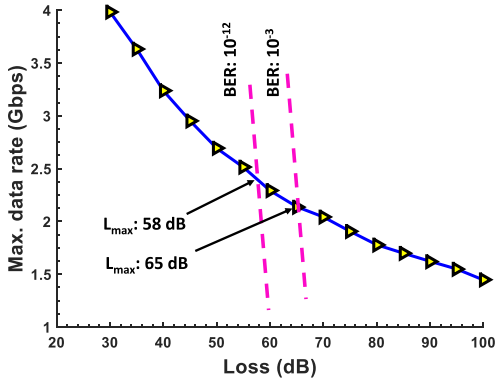


FIGURE 24. Variation of maximum data rate with channel loss for topology-II. Note that, deploying an LNA in the front-end enhances the data rate by providing a gain to the input signal and extends the maximum allowable channel loss (L_{max}) for a target BER by reducing the total input-referred noise.

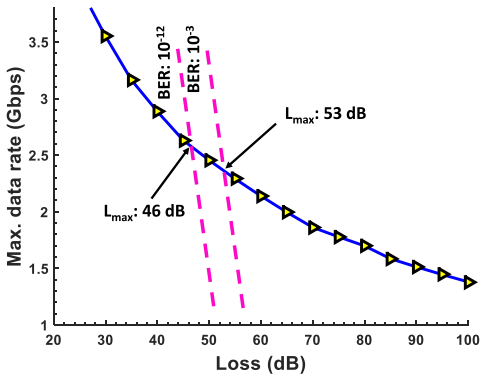


FIGURE 25. Variation of maximum data rate with channel loss for topology-III. Using integrator in the front-end improves the data rate as compared to topology-I, however, maximum allowable channel loss doesn't improve as input-referred noise of an integrator is comparable or larger to that of a SAL.

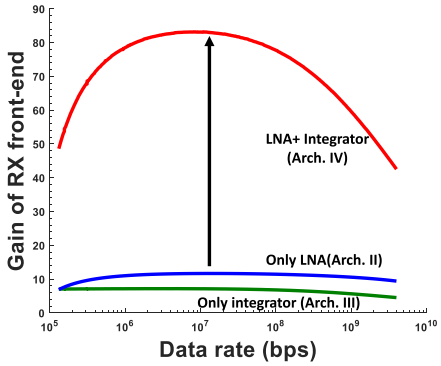


FIGURE 26. Gain improvement of RX front-end by cascading LNA and integrator in topology-IV.

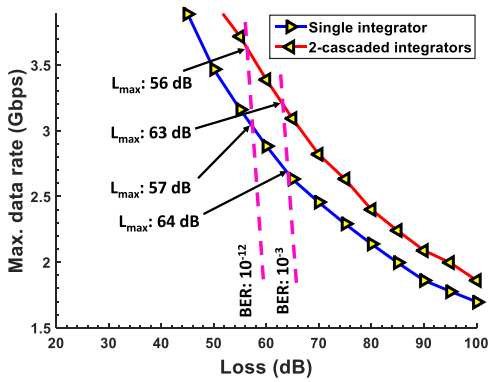


FIGURE 27. Variation of maximum data rate with channel loss for topology-IV with single and 2-cascaded integrators. Deploying an LNA followed by an integrator enhances the data rate significantly as well as improves the maximum allowable channel loss by simultaneously providing large gain and reducing the input-referred noise. Cascading two integrators provides even larger front-end gain and improves the data rate further.

the corresponding BER constraint curves are vertical. The channel loss at which both the constraint curves intersect denotes the maximum channel loss (L_{max}) the topology can support for a given BER. Considering a target BER of 10^{-12}, L_{max} for topology-I is 48 dB and for a BER of 10^{-3}, the maximum allowable channel loss is 55 dB. Also, as power consumption of the strongARM latch is proportional to the clock frequency (and hence to the data rate), energy efficiency of topology-I is constant and independent of the data rate. For the design in this work the energy efficiency is found out to be 0.022 pJ/bit.

B. TOPOLOGY II: LNA + SAMPLER

Fig. 24 shows the performance of topology-II for different channel loss. As expected, introduction of the LNA improves the maximum data rate for each channel loss and also shifts the BER constraint curve towards right by offering lower input-referred noise. The input-referred noise of the RX in this case can be given as

$$V_{n,in,RX} = \sqrt{V_{n,in,LNA}^2 + \frac{V_{n,in,samp}^2}{A_{LNA}^2}} \tag{30}$$

From eq. (30) it can be seen that the RX input-referred noise is mostly dominated by the LNA and hence is quite low comparative to that of topology-I leading to a 10 dB improvement in maximum allowable channel loss (Fig. 24). Also, the $V_{n,in,RX}$ is a function of data rate and hence, the BER constraint curves in Fig. 24 are not exactly vertical as in Fig. 23. From Fig. 10(c) it can be understood that at higher bandwidths of operation, for a small reduction in the input-referred noise of the LNA, the corresponding reduction in bandwidth is drastic. This leads to a large negative slope of the BER constraint curve. Which implies that if the channel loss for the particular application is greater than L_{max}, the RX will work in the noise-limited regime and the maximum allowable data rate will fall drastically with increase in channel loss while satisfying the BER constraint. Note that the minimum bias current required for the LNA varies linearly with data rate (Fig. 10(a)) rendering the energy efficiency of topology-II to be constant which is having a value of 0.082 pJ/bit in this design.

C. TOPOLOGY III: INTEGRATOR + SAMPLER

Fig. 25 shows the performance of topology-III for different channel loss. Given that both the LNA in topology-II

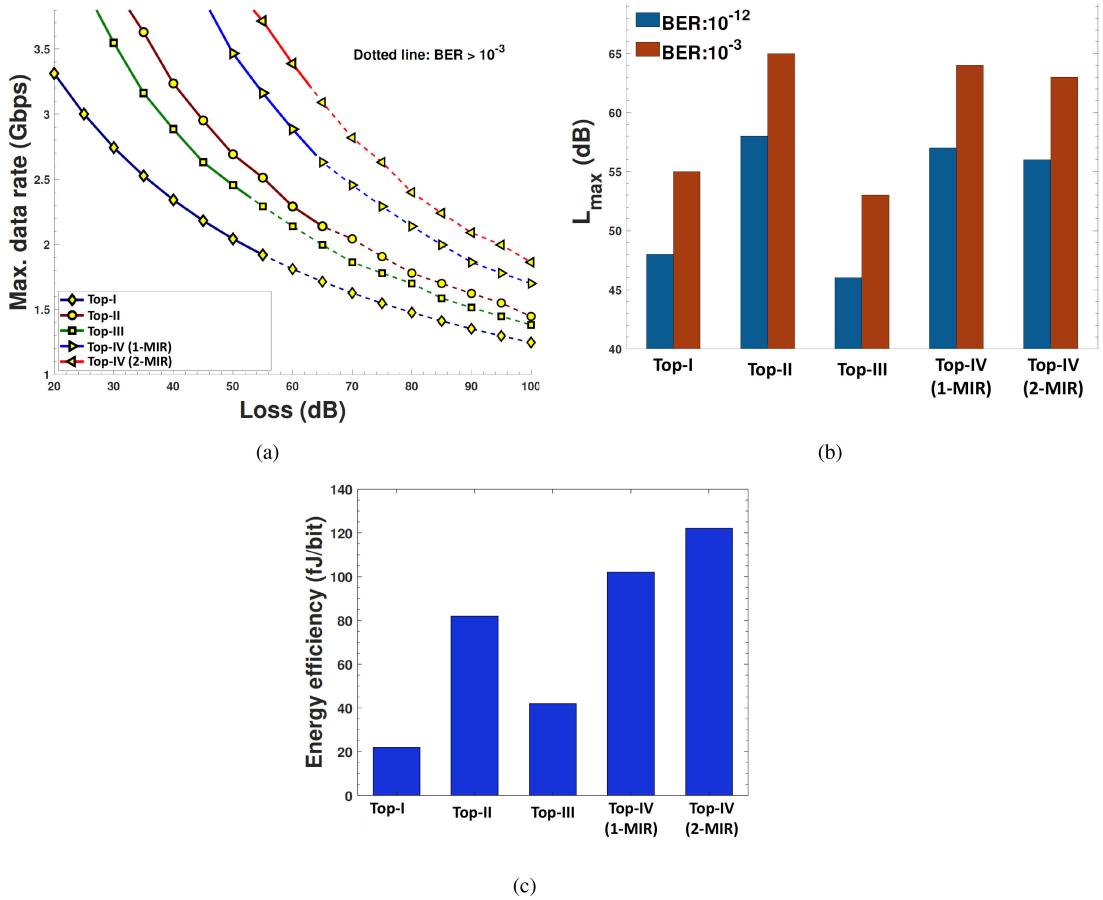


FIGURE 28. Performance comparison of different RX topologies in terms of (a) maximum achievable data rate for different channel loss, (b) maximum allowable channel loss for a target BER and (c) optimum energy efficiency.

and integrator in topology-III are driving the same sampler (i.e., same C_L), performance of the integrator is subordinate to that of the LNA both in terms of gain and input-referred noise. Hence, a deterioration in maximum allowable data rate and maximum achievable channel loss can be observed as compared to topology-II. However, energy efficiency of this topology ($\approx$ 0.042 pJ/bit) is superior than that of topology-II due to lower power consumption of the integrator. It also shows a significant improvement in the maximum data rate compared to that of topology-I due to the additional gain provided by the integrator. Hence, topology-III can be suitably used to achieve high data rate with low power consumption for applications with relatively lower channel loss.

D. TOPOLOGY IV: LNA + INTEGRATOR(S) + SAMPLER (MIR)

To improve the maximum achievable data rate further for topology-II, an integrator can be introduced between the LNA and sampler, which provides gain to the signal with lower power consumption. Fig. 26 shows the improvement in gain of the RX front-end by cascading an LNA and integrator. Using both LNA and integrator in the RX front-end ensures both lower RX input-referred noise($V_{n,in,RX}$) as well as higher front-end gain. Note that, an alternative way to improve the gain would have been to cascade multiple LNAs. However, the LNA+integrator combination provides comparable gain to that of LNA+LNA combination with a much lower power consumption. To increase the front-end gain further, multiple integrators can be cascaded as discussed in Section II-D resulting in a *multi-integrating receiver* (*MIR*). Fig. 27 shows the variation of maximum achievable data rate with channel loss for topology-*IV* with both single and 2-cascaded integrators. It can be seen from Fig. 27 that the BER constraint curve remains the same for both single and 2-cascaded integrators. This is due to the fact that $V_{n,in,RX}$ is governed by the input-referred noise of the LNA and first integrator as the large gain of the LNA and integrator combination makes the noise contribution of the next stages insignificant. Energy efficiency of topology-*IV* is 0.102 pJ/bit with a single integrator and 0.122 pJ/bit for 2-cascaded integrators.

IV. COMPARISON OF DIFFERENT TOPOLOGIES

Fig. 28 compares the performance of different RX topologies. It is obvious from the previous discussions that for any given channel loss, topology-IV with 2-cascaded integrators (i.e., *MIR*) gives the highest maximum achievable data rate (Fig. 28(a)). With increase in channel loss, the maximum

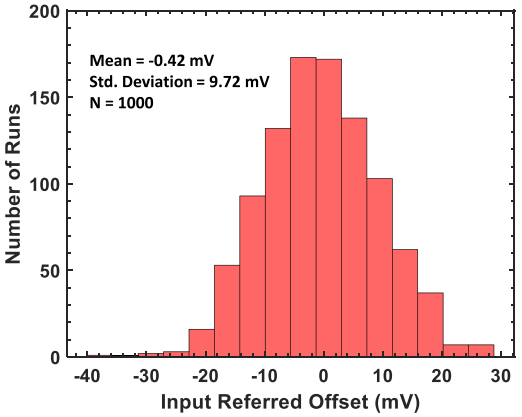


FIGURE 29. Monte-Carlo simulation for the input-referred offset of the integrator.

achievable data rate decreases with a gradual degradation in the BER performance for all the topologies. In Fig. 28(a), the dotted portion of the curves represents a BER $> 10^{-3}$. Fig. 28(b) shows the maximum sustainable channel loss for different RX topologies for two standard BERs. Up to these channel loss values (i.e., L_{max}), the data rate is mainly governed by the timing behavior of different signaling blocks. However, once the channel loss exceeds L_{max}, the maximum data rate is limited by the noise-performance of the signaling blocks. Hence, for any specific application, the designer can readily identify the region of operation and can optimize the chosen RX topology accordingly. It can be seen that deploying LNA in the RX front-end extends the maximum achievable channel loss for topologies II and IV compared to the others. If the application demands high data rate even with a very large channel loss, one must deploy an LNA in the RX front-end. If one wants to increase the data rate further, one may increase the number of integrators used in the MIR front-end, however, with additional power consumption. Note that, all these figures show the ideal performance of different topologies. In real scenario, the clocking scheme apart from the signaling blocks may also limit the maximum data rate and increase the energy-efficiency. However, those additional constrains have not been considered in this work as the main focus was to identify the most suitable topology given different channel loss profile and data rate requirements. Our previous work on interference-robust HBC [20] deploys topology-III which achieves a data rate of 30 Mbps for a channel loss of 60 dB and target BER of 10^{-3}. This observation can be corroborated from Fig. 25 which shows that, for topology-III once the channel loss exceeds L_{max} ($= 53$ dB), the maximum achievable data rate decreases drastically while satisfying the target BER.

While comparing different RX topologies, the input-referred offset of the signaling blocks has been ignored. However, both the integrator and the strongARM latch practically contributes to input offset of different topologies due to mismatch between devices. Fig. 29 shows the Monte-Carlo simulation for the statistical input-referred offset of the integrator for the input device sizes chosen to be $w = 4\mu m$ while operating at a clock frequency of 1 GHz. The standard deviation of the input offset is 9.72 mV. Similarly, following the methodology mentioned in [39], the standard deviation of the input-referred offset of the strongARM latch has been found to be 10.52 mV assuming the statistical offset to follow a Gaussian distribution. Given this data, the input-referred offset of different topologies can be compared and the MIR can be proved to have the lowest input offset ($\sim$ 1 mV). Note that, this input offset can be greatly reduced by means of different offset cancellation techniques for integrators and strongARM latches mentioned in [5], [20], [40], [43], [44].

V. CONCLUSION

Some emerging applications are utilizing wireline-like wireless channels, which is leading to *lossy broad-band channels*, that are atypical of traditional wireline communication. The transceivers for such channels tend to be noise-limited instead of being ISI-limited, calling for a new class for transceivers. The work theoretically analyzes performance of different signaling blocks that can be employed in the RX for broad-band communication through lossy wireline-like channels. A new approach to theoretically estimate the input-referred noise of the strongARM latch has been described and compared with simulation results. An accurate closed-form expression of the gain of the current-integrating amplifier has been developed. The work also proposes the use of multi-integrator cascade as a low-power gain element and shows how employing the same in the RX improves the gain of the front-end with low power consumption. Finally, based on the analysis of the signaling blocks, performance of different topologies have been analyzed and compared. Although this work assumes an ideal lossy-channel with large enough bandwidth, once the designer chooses a particular RX topology form the ones analyzed here, they can add or modify functionalities to meet the specific requirements of the channel under consideration. The in-depth analysis presented in this work sets a foundation for the choice of appropriate receiver topology and should serve as a great place to start a design for designers working on emerging applications of lossy broad-band channels such as proximity communication, human body communication, among others.

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