20.11 A crystal-less BodyID with an asynchronous clockless leakage-powered wake-up receiver and over-the-channel clock recovery

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Energy-constraint wireless transceivers with wake-up receivers (WuRX) traditionally rely on an always-running clock (Fig. 1) for sampling incoming data and digital correlation, necessitating local oscillator calibration through a reference, such as crystal oscillator. This consumes unnecessary power during idle periods and adds significant size and cost to the system. Removing the always-running clock can reduce system power consumption to leakage levels during idle, requiring innovative approaches to implement the wake-up functionality while maintaining low latency. The absence of the external clock reference can enhance energy efficiency and system integration but requires innovation in clock synchronization methods. Recent advances in the solid-state community targeting ultra-low-power (ULP) wearables have achieved notable energy efficiency and latency [1-19]. However, limitations remain in having an always-running clock and ULP clock generation unit needing external reference, creating a research need for ULP yet low-latency solutions. [1] demonstrates a ULP WuRX with 17nW, albeit with a higher latency of 2ms due to the ULP clocks operating at 4kHz. [2] presents a ULP WuRX with 200us latency but at the cost of 220uW power consumption, restricting its impact on battery-less nodes. [3] showcases a battery-less wearable node with a combined peak power of only 13.96uW, but it relies on a power-hungry external crystal for clocking, negating the energy efficiency gains. While [4-6] offer ULP crystal-less designs, they either depend on external reference voltages for calibration or utilize a forwarded clock through power or amplitude shift keying (ASK) signals, which limit their applicability across different use cases.

Addressing these challenges, [7] highlights a promising approach, demonstrating over-the-air clock recovery without needing an additional clock reference despite not being ULP. [8] utilized the body-channel to achieve 102us latency with 45uW power. However, the wideband body-channel (0.1-30MHz) promises significantly more. In this paper, we introduce a ULP always-on and instantly responsive BodyID SoC featuring an asynchronous, clock-less WuRX that consumes only leakage power when listening and utilizes over-the-channel clock recovery that is both crystal-less and reference-less. While this approach is realized through the wideband human body communication channel, it is also applicable to other communication systems that rely on on-off-keying (OOK) modulation.

The full system architecture of the fabricated IC is illustrated in Fig. 2. The IC consists of six primary blocks: 1) a ULP and low-latency asynchronous WuRX, 2) a ULP clock recovery unit, 3) a digital data demodulation unit that leverages a counter and comparator to demodulate data, 4) a digital Finite State Machine (FSM), 5) an OOK data modulation unit, and 6) a transmitter tri-state driver. The WuRX, despite being clockless, can pass the input data stream through multiple delay stages, with each stage automatically tuned to a delay equal to half the carrier-clock-period. This design converts the incoming serial bit pattern to multiple-parallel delay-adjusted bit streams on which a combinational circuit can operate without a clock, allowing the asynchronous WuRX to be triggered only by the correct bit pattern. To enable ULP listening, instead of oversampling or Nyquist designs, a clockless asynchronous design of the WuRX ensures that only leakage power is consumed while maintaining the wake-up capability. This reduces the listening power consumption to just 191.6nW, >234x lower than similar latency prior work [8]. The intermittently syncing clock recovery unit operates by synchronizing to the intermittent OOK data, where the carrier frequency is present during a bit '1' and maintaining the frequency during bit '0' (Fig. 2).

Fig. 3 illustrates always-listening ULP asynchronous clockless WuRX. The data input (DIN) flows through nine cascaded delay cells, each tuned to a half carrier-clock-period delay and the wake-up sequence matching happens at the carrier-clock domain to achieve low latency. While [9] originally introduced this delay cell for clockless WuRX, it was limited by needing external delay tuning. This work enhances the design by incorporating an auto-tuning capability. Specifically, a phase detector (PD) is implemented to adjust the delays of each cell through current starving by comparing the DIN with the delay chain third-stage output and controlling Vtune. Within each cell, the input is processed by a reset-set flip-flop, which automatically resets after a half-clock period by a self-generated reset pulse to allow sufficient Vcap rise time to VDD. After the 1st delay stage, the reset pulse becomes the input to ripple-carry DIN to subsequent delay stages. When the individual delay matches the half-clock period, all the Q's represent an integer multiple of a half-clock-period delayed copy of DIN. After the delay auto-tuning and serial to parallel conversion, a combinational circuit detects the correct bit sequence by comparing the outputs (Q1,3,5,7,9) with a 5-bit Barker code: 11101. The level-0 in the code sequence requires a mechanism to prevent unintended delay tuning when the input is level-0 and Q3 is level-1. To address this, the combinational circuit generates a no-tune signal to stop the PD when the input is level-0, but all outputs are level-1. A false-triggering protection circuit is developed to enhance reliability further by delaying the no-tune signal by a clock period. The enable signal is only triggered when the correct bit sequence and the delayed no-tune signal are detected together. This approach effectively prevents spurious spikes and misalignments of outputs from falsely triggering the enable signal, which could otherwise occur during startup or with incorrect DIN sequences. True negatives are reduced by utilizing a wake-up sequence with repeated barker codes. In the presence of DIN, the WuRX consumes 425.5nW, which is 105x lower than similar latency system [8]. The minimum time required for the delay to lock onto the input carrier frequency from startup is <80us, 20% lower than the previous body channel WuRX [8]. Compared to BLE WuRx [2], a 2.5x latency reduction is achieved.

Fig. 4 presents the ULP clock recovery (CR) unit. Oversampling CR techniques suffer from increased complexity and power consumption despite being commonly employed for high accuracy and low jitter. To enhance energy efficiency, this design implements a baud rate CR approach. The CR core is a 71-stage digitally-synthesized current-starved ring oscillator (ROSC) with a closed-loop and open-loop mode. In the closed-loop mode, the output of ROSC feeds back to its input, whereas in the open-loop mode, the data input (DIN) is directly fed into the ROSC. A PD adjusts the oscillation frequency by varying the propagation delay of the ROSC current-starved inverter, through Vtune. To achieve a fast start-up and fast lock onto the carrier frequency, the PD is enabled at start-up, and the ROSC operates in open-loop mode for 10 clock cycles, followed by 1000 cycles in closed-loop mode. This process accelerates the frequency locking time to <80us. After the start-up phase, the ROSC syncs to the carrier clock frequency whenever DIN is present by switching to open-loop mode with the PD enabled. When DIN is absent, the ROSC maintains the open-loop oscillation frequency by switching back to closed-loop mode and disabling the PD to effectively hold the Vtune. A fast data presence detector is implemented to identify positive and negative phase differences between DIN and the clock output, allowing instant switching between the two modes. No tuning is required if no phase difference is detected between DIN and the clock. To prevent the Vtune leakage from affecting the clock frequency during extended periods without DIN, the Vtune capacitor is sized up such that frequency deviation in the baseband clock remains within 3% after 200ms of DIN absence, as shown through the measured result in Fig. 4.

Fig. 5 shows the oscilloscope-captured waveform of the clockless WuRX and the over-the-channel CR unit. The IC is externally powered, and an FPGA (CMOD A7) provides the test waveform into the IC at 1 MHz. For the WuRX, the measured Q1 and Q7 signals are displayed, demonstrating frequency locking onto the DIN frequency in <80us. Additionally, the data is propagated sequentially from Q1 to Q7 and Q9, with the enable signal being sent out only when the correct bit pattern is detected. For the CR unit, the measured start-up waveform shows that the frequency converges to the 1MHz DIN carrier frequency within 80us. The intermittent synchronization capability is also illustrated, with the clock frequency holding input frequency during the absence of DIN and locking to 1MHz upon the presence of DIN. Moreover, by performing demodulation in the digital domain, an adjustable hysteresis mechanism enables a clock frequency deviation tolerance of up to 3.3%, enabling prolonged DIN absence.

In contrast with conventional RF WuRXs, which prioritize sensitivity enhancement, this paper focuses on innovations in the time domain for asynchronous, clockless WuRX, simultaneously achieving low latency and ULP along with intermittently syncing clock-recovery suitable for wideband body channels. Comparison with state-of-the-art (SOTA) is shown in Fig. 6. The proposed design achieves a listening power of 191.6nW, representing >5x reduction compared to prior SOTA, while maintaining a start-up latency of <80us and requiring just 34pJ of start-up energy, marking a significant improvement over SOTA. The crystal-less operation is realized by intermittently syncing with the incoming data, achieving a clock start-up latency of <80us, a 20% improvement over existing designs. Fig. 7 presents the die micrograph and key specifications of the 65nm TSMC CMOS IC, which has 0.077mm² total active area.

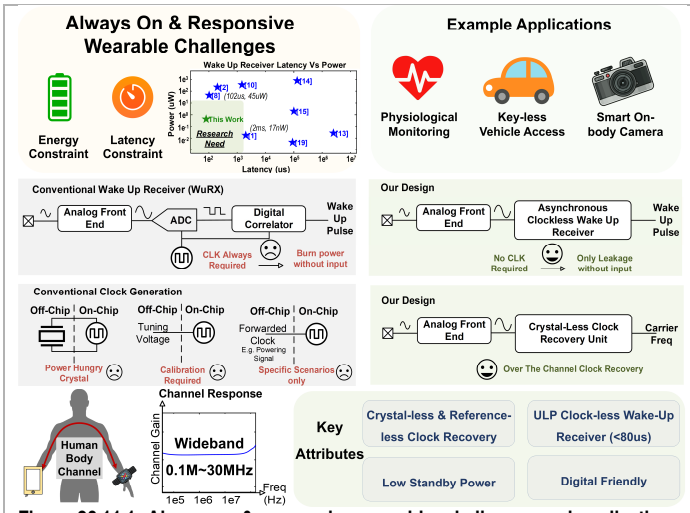


Figure 20.11.1: Always on & responsive wearable: challenges and applications; conventional vs implemented wake-up receiver & clock generation; key attributes of the IC

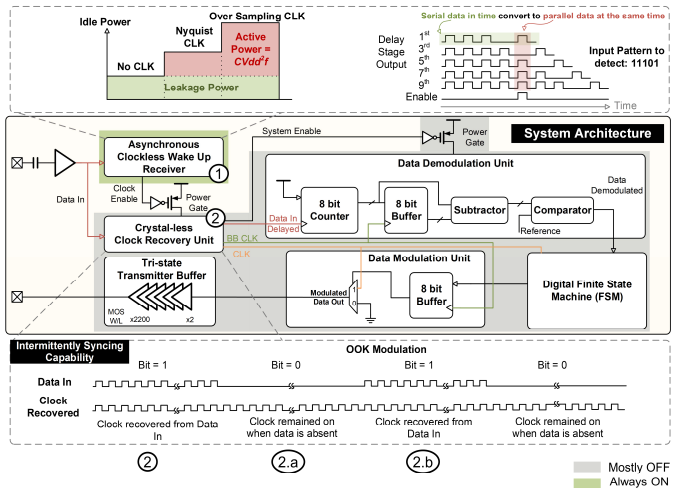


Figure 20.11.2: Full system architecture and working principle

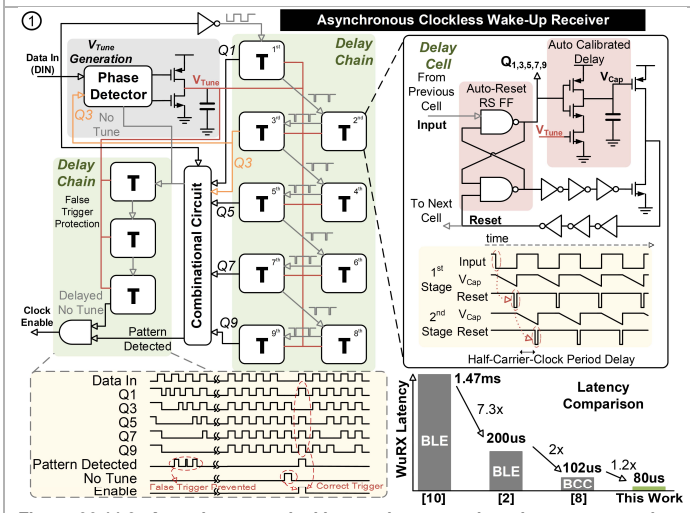


Figure 20.11.3: Asynchronous clockless wake-up receiver; latency comparison with state-of-the-art wake-up receivers.

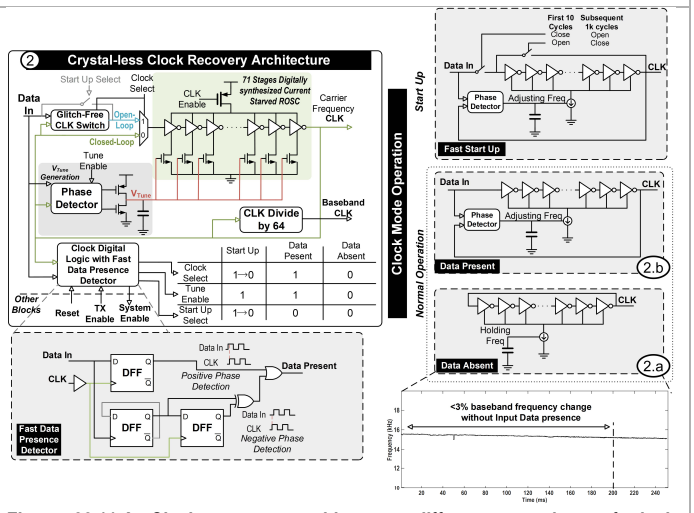


Figure 20.11.4: Clock recovery architecture; different operations of clock recovery architecture; measurement result of clock holding frequency without input data presence.

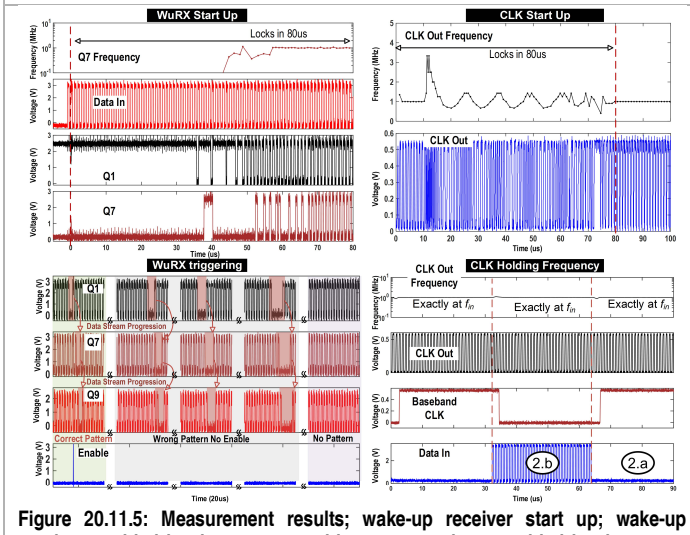
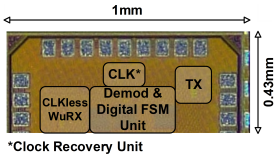


Figure 20.11.5: Measurement results; wake-up receiver start up; wake-up receiver enabled by the correct enable pattern and not enabled by the wrong pattern; clock start up; clock holding frequency and intermittent synchronization with the incoming data.

	This Work	ISSCC'20 [7]	ISSCC'24 [4]	JSSC'21 [10]	ISSCC'19 [2]	ISSCC'24 [11]	JSSC'16 [12]	JSSC'15 [8]
Crystal-less	*Yes*	Yes	Yes	NA		No	Yes	Yes
Over-the-channel clock recovery through Data			No	NA		No		
Forwarded Clock	*No*	No	Yes	No				
Clock-less WuRX	*Yes*	No	NA	No			NA	No
Listening[$] power	*191.6nW*	2.7mW	NA			1.11uW	NA	
Clock Operational power	*351.7nW*	NA	2.193uW	NA			22.5mW	NA
WuRX Operational power	*425.5nW*	NA		4.4uW (Wi-Fi) 352uW (BLE)	220uW	NA		45uW
Total Operational power	*3.93uW[#]*	2.7mW	17uW			44uW	22.5mW	45uW
WuRX start-up latency	*<80us*	<750us	NA	1s (Wi-Fi) 1.47ms (BLE)	200us ~ 1.47ms	NA		<102us
Clock start-up latency	*<80us*	<100us	NA				<600us	NA
WuRX start-up energy	*34pJ*	2.025uJ	NA	4.4uJ / 517nJ	44nJ~323.4 nJ	NA		4.59nJ
Area (mm^2)	*0.077*	1.33	0.95	0.6	2.4	0.66	1.63	1
Technology	*65nm*	40nm	65nm	65nm	65nm	40nm	65nm	0.18um
Operation Frequency	*1MHz**	2.4GHz	2.4GHz	2.4GHz	2.4GHz	433MHz	0.2~9MHz	80MHz

* Broadband HBC Frequency Range: 0.1MHz ~ 30MHz, # with TX Power

Figure 20.11.6: Comparison table with the state-of-the-art wake-up receiver and clock generation SoCs.



Specifications	
Process	TSMC 65nm
VDD	0.46V (Clkless WuRX) 0.47V (Clk Recovery Unit) 0.5V (Demod & Digital FSM Unit) 0.52V (TX)
Die Area	0.6mm^2
Active Area	0.077mm^2
Idle Power	265.3nW
Carrier Frequency	1MHz
Baseband Frequency	15.625KHz
Modulation Scheme	On-Off-Keying
Communication Channel	Human Body & Conductive Structure
CLKless WuRX	
Functionality	Clock-less Pattern Recognition
Operational Power	425.5nW
Leakage Power	161nW
Clock Recovery Unit	
Operational Power	351.708nW
Transmitter	
Operational Power	3.1564uW

Figure 20.11.7: IC micrograph and specification.

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