A 65nm 21.9pJ/Sa Pixel to PWM Conversion SoC with Time-domain Body Communication for ULP Body-Worn Video Sensor Nodes with Distributed Real-Time Inference

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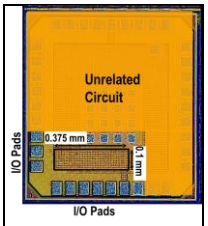
With the growing presence of body-worn cameras, head-mounted devices, and smart glasses in the era of Internet of Bodies (IoB) and Internet of Things (IoT), the demand for low-power, smaller form-factor nodes for video sensing, computing, and communication with an ability for long term usage and easy integration on the body have been steadily increasing. As shown in Figure 1, conventional architectures employ front-end ADCs to convert all the sensed analog samples to digital bits (high data volume) and then compress it using DSP blocks before communication. However, such implementations consume high conversion energy [1] and generate huge data volumes that need significant energy for communicating over wireless modalities, like Wi-Fi (which consumes 50-400mW for HD video at 30fps), Bluetooth cannot yet transfer HD video), etc. Recent non-IC based video sensing solutions [2] uses pulse-width modulated backscatter system, where the analog sampled values are converted to pulse widths before modulation, using COTS components and backscatter communication, which cannot support higher bandwidth. Although it eliminates the need for front-end ADC, the solution has bigger form factor and can function with only smaller frame sizes (112 x 112 at 13 fps), while consuming significantly higher power (2.36 mW), which makes it unsuitable for high-speed video transmission around the human body. In recent years, Human Body Communication (HBC) has emerged as a promising low-power alternative for wireless communication, providing easy integration with the body and keeping the data secured close to the body. These sensor nodes are also required to get real time inference from the data received from the sensors for proper data analysis. This inferencing workload can be transferred to an On-Body processing hub which can be of higher power and larger form factor, hence, transferring the high-power processing from the sensors to the hub, enabling distributed processing of the signal. We present the first monolithic solution **ATC-VSN** (Analog Voltage to Time Converter Video Sensor Node) for ultra-low power energy harvester friendly VSNs, to achieve a low-power sensing and communication solution for transmitting video around the body. It exploits the time-domain data representation to eliminate the need for front-end ADC and utilizes the low power, wideband and secure HBC communication modality to transmit the pulse-width modulated analog signal through the human body to the On-Body processing hub where the real time inferencing can be realized exhibiting > 21.9 pJ/Sa energy efficiency, which is orders of magnitude improvement over state of the art techniques [2]. For body worn cameras, a design space is explored where a direct ATC image sensor output followed by ultra-low power (ULP) HBC channel using time domain samples can enable order of magnitude reduction of power consumption in body worn VSNs, making ATC-based VSNs an energy-efficient replacement for ADC less implementations.

ATC-VSN presents the first on-chip validation of Analog to Time Conversion and communication using pulse-width modulated analog values for ULP VSNs. Figure 2 shows the overall system architecture of the ATC chip, implemented in a 65nm CMOS process. To mimic the operation of analog camera(sensing), the gray scale image pixel values are read column/row wise and serially converted into analog voltage samples (within a voltage dynamic range), before feeding it to the IC using Arbitrary Waveform Generator (AWG). The input waveform is sampled using a high frequency clock generated using an on-chip Ring Oscillator (RO). Care is taken to maintain at least a 4X oversampling for accurate reconstruction of the input in post processing. The RO is designed using a 7-stage single-ended current starved inverters, where the frequency can be controlled using the supply voltage or the bias of the pull-up or pull-down path of the current-starved inverters. The sampled input voltage is stored on a capacitor (=1pF), which is discharged using a constant current source, which can be either controlled by a 5-bit Scan Control or by the reference current (I_{ref}). During high-speed operation, the discharge current (I_{dis}) is used to tune the pulse width and achieve a larger dynamic range to represent the analog voltage values of pixels. The voltage across the discharging capacitor is compared with a reference voltage V_{Th}, which is generated using a 5bit DAC, providing another knob to control the mapping of the analog voltages to pulse width. Hence, the resulting pulse-width of PWM signal depends on the sampled voltage across the capacitor, the discharge current and threshold voltage (V_{Th}). Figure 2 (bottom) shows the circuit diagram and resulting waveforms.



Die micrograph.

To transmit the generated PWM waveform, the HBC driver couples the binary (digital-like) PWM signal to the human body for communication. Since the human body has a flat-frequency response in the Electro-Quasi-Static EQS region (~ up to 10's of MHz) of operation [3], the time-domain characteristics (pulse-widths) of the waveform remain intact during transmission and only the amplitude of the signal gets attenuated due to the channel loss.

Figure 3 (top) presents the timing waveforms for an input sinusoid at 5MSps, depicting the variations in the pulse-widths for different voltage levels. The IC generates pulse-width modulated waveform corresponding to the analog voltage values (fed using AWG), which is coupled to the human body for communication using HBC driver. The PWM signal are captured using an oscilloscope and further processed in MATLAB. The pulse-widths of received PWM signal are measured and re-scaled back to voltage levels of the input. For performance evaluation, we have used standard image processing metrics, the Peak-Signal-to-Noise-Ratio (PSNR) and Structural Similarity Index (SSIM). Different sets of images are used for validating the functionality of the system. Figure 3 (bottom left) shows the dependency of generated PWM signal for various input data rates, illustrating the dynamic operating range of the input and output signals. Figure 3 (bottom right) shows that high frequency operation reduces the dynamic range of pulse-widths as well as it reduces the operable input voltage range. However, by proper calibration of the discharge current I_{dis} and the comparator threshold V_{th}, the input range can be further extended for operating effectively at higher frequencies.

The entire ATC-VSN node occupies an area of 375 µm × 100 µm. Figure 4 (top left) shows the power consumption for different input data rates at varying supplies. The IC consumes 0.64µW- 110µW for sample rate varying from 0.1- 5 MSps, which is > 100X lower than other reported works in the literature. Figure 4 (top middle) presents the shmoo plot which depicts the operability of the IC for various supplies and data rates. Figure 4 (top right) shows the optimal VDD to be supplied for efficient functioning of the IC for various data rates. ATC-VSN exhibits a 21.9 pJ/Sample energy efficiency while operating at 5MSps and 0.75V core VDD supply. Figure 4 (bottom) evaluates the performance of the IC for different sets of images using PSNR and SSIM metrics. Checkerboard images exhibit better reconstruction qualities due to higher dynamic range at the input. We chose > 0.85 SSIM , user perception metric, as the acceptable image quality for our work, which is considered a standard for several image processing applications. Figure 5 (top) shows the input and reconstructed images and test-chip specifications. Reconstructed test images exhibits >22 dB PSNR and > 0.93 SSIM values. Figure 5(bottom) shows the off-chip offline pre and post processing done in MATLAB, demonstrating the entire test flow.

Figure 6, shows the measurement setup and compares the test chip performance with state-of-the-art communication ICs exhibiting the lowest energy efficiency of 21pJ/Sa and highest dynamic range of 300mV at 5MSps video communication compared to the implementation in [2] due to maximally linear ATC, and ultra-low power flat-band EQS-HBC Communication link.

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References:

[1] B. Murmann, " ADC Performance Survey" [Online] [2] S. Naderiparizi [MobiSys 2018] [3] D. Das, [Scientific Reports 2019] [4] S. Hanson, [JSSC 2010], [5] H. Cho, [ISSCC 2015], [6] J. Jang, [JSSC 2018]. [7] B. Chatterjee, [ESSCIRC, 2022].

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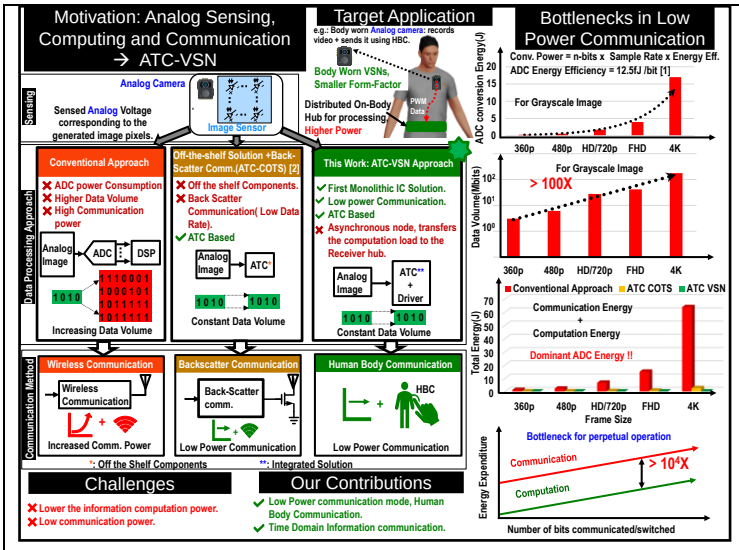


Fig 1. (Top left) Motivation for ATC-VSN. (Middle) Target application for Body worn VSNs (Top right) Bottlenecks in Low power communication: ADC and data communication energy. (Bottom) Challenges and Our contributions.

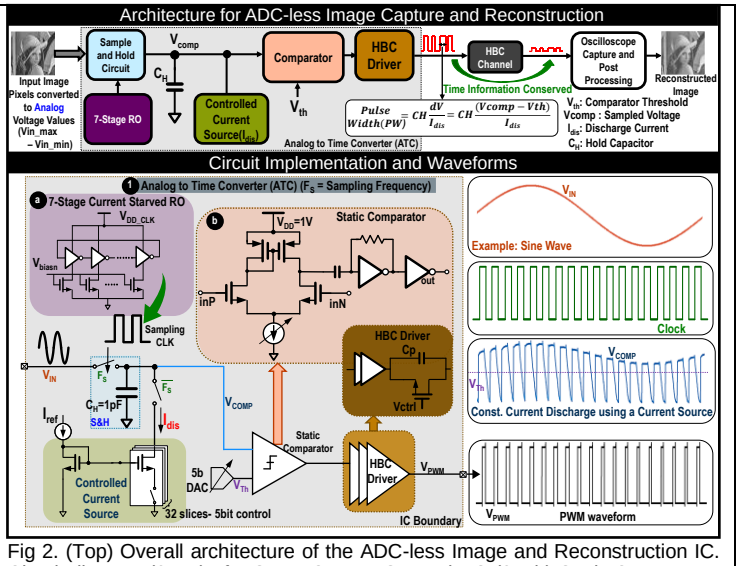


Fig 2. (Top) Overall architecture of the ADC-less Image and Reconstruction IC. Circuit diagram (2.1.a) of 7-Stage Current Starved RO (2.1.b) Static Comparator (Bottom) The detailed circuit diagram of the IC along with the waveforms at various nodes.

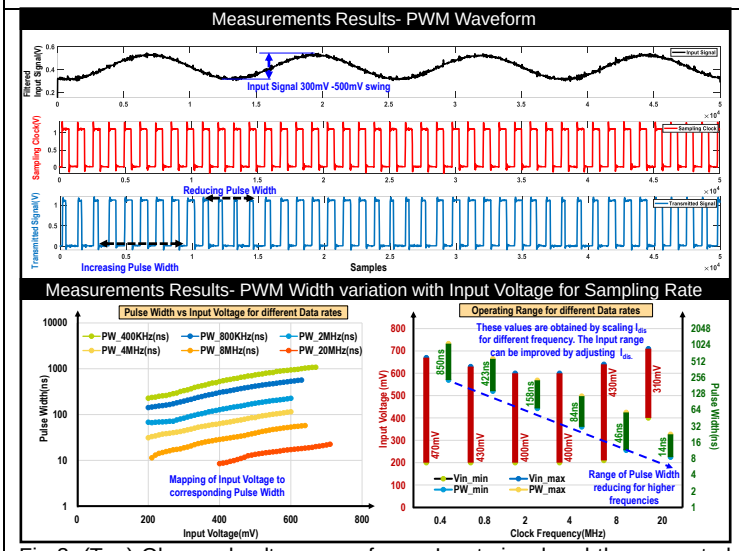


Fig 3. (Top) Observed voltage waveforms: Input signal and the generated PWM signal. (Bottom) Shows the relation between the Input voltage and the Pulse width along with many-to-many mapping of Input Voltage to Pulse width for various Clock rates.

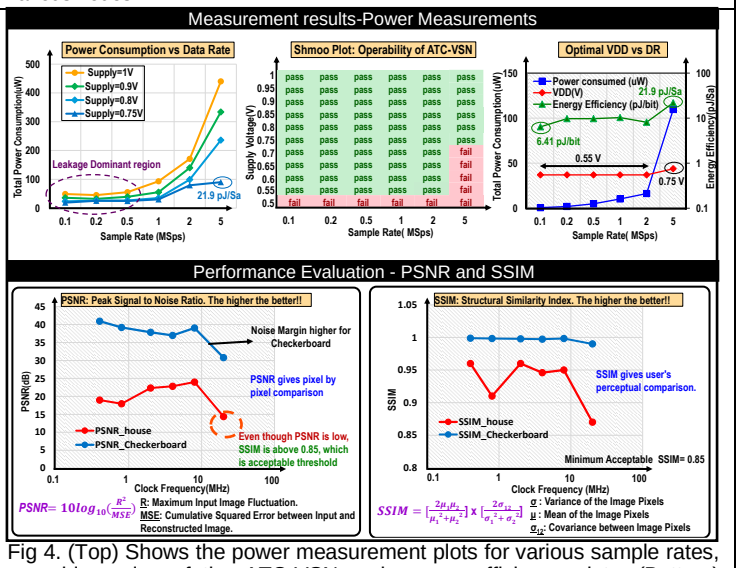
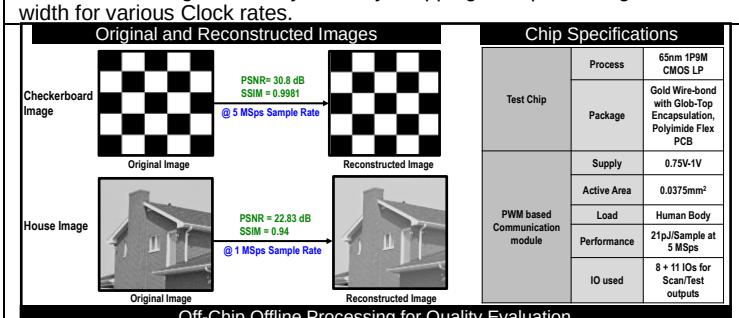


Fig 4. (Top) Shows the power measurement plots for various sample rates, operable region of the ATC-VSN and energy efficiency plots. (Bottom) Shows the PSNR and SSIM plots for various clock rates for House and Checkerboard Image - Setup shown in Figure 5.



Chip Specifications		
Test Chip	Process	65nm 1P9M CMOS LP
	Package	Gold Wire-bond with Glob-Top Encapsulation, Polyimide Flex PCB
PWM based Communication module	Supply	0.75V-1V
	Active Area	0.0375mm²
	Load	Human Body
	Performance	21pJ/Sample at 5 MSps
	IO used	8 + 11 IOs for Scan/Test outputs

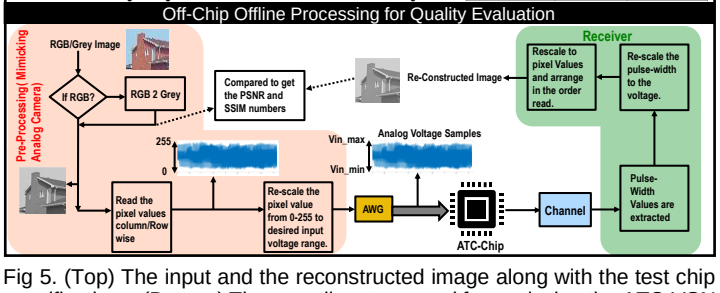
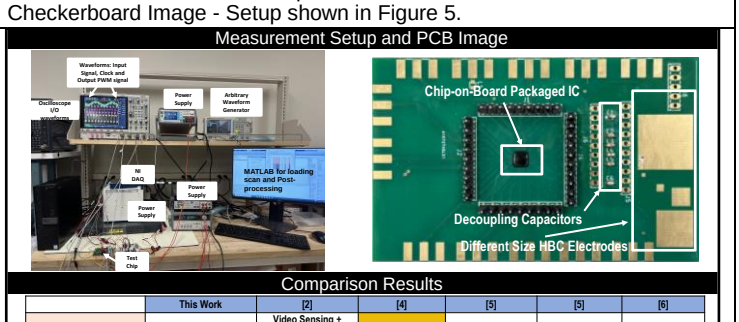


Fig 5. (Top) The input and the reconstructed image along with the test chip specifications. (Bottom) The overall system used for analyzing the ATC-VSN non-idealities.



Comparison Results	This Work	[2]	[4]	[5]	[5]	[6]
Target Application	ATC + Communication	Video Sensing + Communication	Sensing Only	Communication	Communication	Communication
Sensing	Yes	Yes	Yes			
Implementation Style/ Communication Mode	Analog to Time Conversion	Analog to Time Conversion	Analog to Time Conversion	Coherent BPSK	OOK	BPSK
Sample/Data Rate	100K- 5MSps	1 MSps		80 Mbps	100 Kbps	80 Mbps
IC Solution	Yes	No	Yes	Yes	Yes	Yes
Power Supply	0.75-1	3.7	0.5	1.2	0.8	1.1
Communication Medium	HBC	Backscatter		BCC	BCC	BCC
Power Consumption	109.5 uW (5 MSps)	15.66 mW (1 MSps)		6.32 mW (80Mbps)	43 mW (100Kbps)	1.76 mW (80 Mbps)
Energy Efficiency	21.9 pJ/Sa	15.66 nJ/Sa	140nJ/frame or 8pJ/Sa	79pJ/bit	430nJ/bit	22pJ/bit
Dynamic Range	300-470mV	100mV				
Area	0.375 x 0.1 mm²	3.5 x 3.5 x 3.5 cm³	1.28 x 0.85 mm²	1.8 x 3.2 mm²	1.8 x 3.2 mm²	2 x 4 mm²(Only TX)
Technology	65nm CMOS	COTS Components	130µm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
	Processing + Communication		Sensing	Communication		

Fig 6. (Top) Test PCB with provisions for electrodes to perform HBC testing and overall, the measurement setup. (Bottom) Comparison results with other state-of-the-art ICs.