# A Low Phase Noise 30 GHz Oscillator Topology for Resonant-Fin-Transistors Based High-Q On-chip Resonators in 14 nm Technology

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*Abstract*—**This work presents an ultra low phase noise 30 GHz oscillator topology in 14 nm technology for an active mode Micro-electro-mechanical systems (MEMS) based resonator that utilizes resonant-fin transistors (RFT). A novel oscillator architecture has been presented for the active mode RFT, which can be modelled as a voltage controlled current source with 270° phase shift between its output current and input voltage. The proposed oscillator has been designed in 14 nm GF technology and simulation results show that it achieves phase noise less than -144 dBc/Hz at 1 MHz offset for 30 GHz carrier frequency for active mode RFT with quality factor of 10,000, while consuming 5.5 mW power from 0.8 V supply.**

*Keywords*—**Oscillator, active-mode, RFT, MEMS, phase noise, 14 nm**

## I. INTRODUCTION

High quality factor (Q) on-chip resonators are highly sought for ultra low phase noise oscillators in high performance wireless transceivers. With the advent of 5G technologies, demand of low phase noise, low power, phase locked loop (PLL) free radio frequency (RF) synthesizers have risen to support the huge number of channels around mmWave frequencies. For example, at 30 GHz carrier frequency, continuous channel bandwidth of about 800 MHz to 1 GHz are possible in 5G technologies and there could exist multiple such channels. Traditionally, for RF carrier synthesis, piezoelectric quartz crystals, with reasonable frequency stability having $Q > 10^5$ are used in oscillators. However, due to its bulky size, integration of quartz crystals in standard IC technology is very difficult. Moreover, these quartz crystals are also limited to MHz frequencies ($< 500MHz$), which makes PLL essential for >10 GHz frequency generation, which in turn increases the power consumption while significantly increasing system complexity. The other choice for mmWave oscillators is using on-chip LC tanks. However, problem with LC oscillators is that it occupy huge area. Moreover, its frequency stability is limited due to the limited Q ($< 30$) of the on-chip LC

tank. Injection locking technique or a PLL can be used to improve the performance of an LC oscillator but at the cost of increased power and area. For low power and area efficient RF carrier generation, PLL-free direct resonator based systems seem more viable, which require more versatile devices with monolithic IC integration capabilities. Moreover, transceiver arrays in multiple-input-multiple-output fashion for 5G applications also need individual RF carrier generators, where a fixed frequency carrier is required from each transceiver and tuning range of oscillator need not to be very wide.

Micro-electro-mechanical systems (MEMS) based resonators are the potential candidates for satisfying the low phase noise, low tuning range and low power GHz oscillator demands. In last two decades, a lot of research activities has emerged for developing high frequency monolithic MEMS and acoustic resonators, which can be directly used for RF carrier generation. Recently, researchers have shown resonant Fin transistor (RFT), which can be used as a high-Q active mode resonator for >10 GHz frequencies [1], [2], [3], [4], [5]. In this work, we present 1) a low phase noise oscillator topology at 30 GHz for on-chip, high-Q active mode RFT resonator, 2) its design and implementation in 14-nm GlobalFoundries process and 3) simulation results to validate the proposed topology.

The paper is organised as follows. Section II gives the brief background of the active mode RFT-MEMS technology and its electrical equivalent, which is used for circuit simulations. Section III presents the proposed circuit topology followed by section IV, which presents the implementation details with simulation results. Finally, section V concludes the paper.

## II. RESONANT FIN TRANSISTOR

Monolithic integration of MEMS resonators with CMOS circuits is quite challenging. Integration strategies like MEMS-First CMOS Integration, MEMS-Last CMOS Integration [6] or CMOS back-end-of-line (BEOL) MEMS Integration require
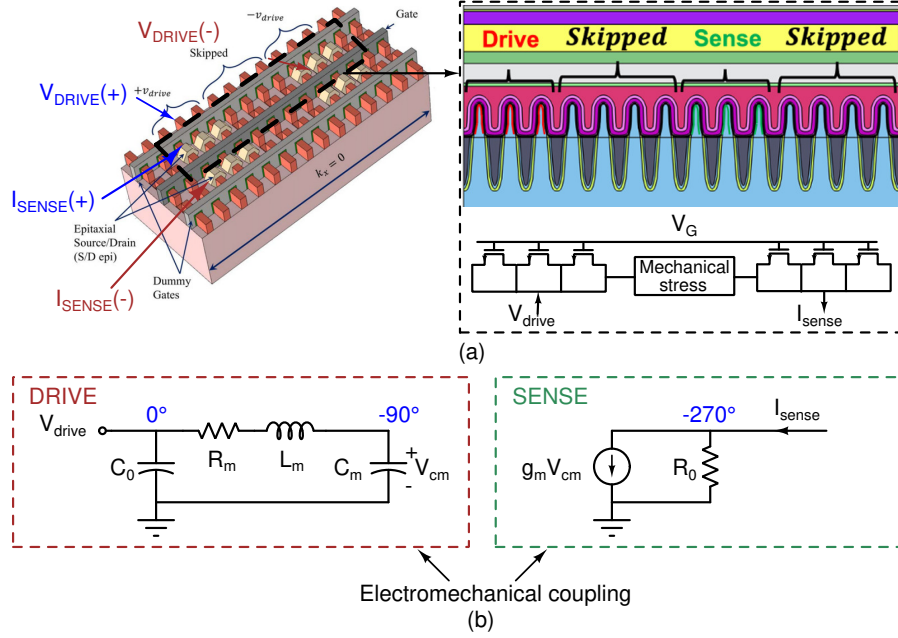
Fig. 1. (a) Depiction of active mode resonant fin FET [2] and (b) its single ended electrical equivalent [1]

very complicated and extensive processing [7]. Creating a free moving surface in MEMS structures for determining the resonance frequency of the resonator and setting the boundary condition is very cumbersome and affects the yield. Moreover, the process involved to fabricate the free surface is highly prone to environmental conditions, which affects the quality of the resonators. The idea of Acoustic Bragg Reflectors (ABR) enables the creation of a truly solid-state MEMS resonator, in which mechanical vibrations can be confined into continuously solid domains without the need for any free surfaces or air gaps [8]. As shown in Fig. 1(a), a Resonant Fin Transistor (RFT) was demonstrated in [2] using the ABR concept. RFT was fabricated in GlobalFoundries's 14nm FinFET technology, leveraging the vertical 3D geometry of FinFETs to efficiently confine, drive, and sense acoustic vibrations in the solid (unreleased) CMOS stack with no post-processing or custom packaging. RFT uses active FET sensing to harness the high-quality, high-yield MOSFETs available in CMOS technologies.

Fig. 1(b) depicts electrical equivalent of RFT in active FET sensing mode, which will be referred as active mode of RFT now onwards [1]. In Fig. 1(c), $R_m$, $L_m$ and $C_m$ are the motional resistance, inductance and capacitance, respectively and $C_0$ is the static capacitance at the driving port of the RFT. As shown in Fig. 1(c), $g_m$ is the equivalent transconduction showing relation between sensed drain current ($I_{OUT}$) and voltage ($V_{cm}$) across the motional capacitance ($C_m$) due to the electromechanical coupling. Quality factor of the resonator is defined as $Q = \frac{\omega L_m}{R_m}$. $R_0$ is the output resistance at the sensing FET. As shown in the Fig. 1(c), $V_{cm}$ is -90° phase shifted with

respect to the input drive voltage ($V_{drive}$) and $I_{sense}$ is further phase shifted by -180° resulting into an overall 270° phase shift between $I_{sense}$ and $V_{drive}$. It makes RFT realization as a voltage controlled current source (VCCS), where the phase shift between output current and input voltage is -270°. Now the question arises that how this VCCS with 270° phase shift realization of active mode RFT be utilized to build an oscillator and what is the fundamental limit of the achievable phase noise of the oscillator. These questions are answered in the following section.

### III. PROPOSED OSCILLATOR TOPOLOGY FOR ACTIVE MODE RFT AND PHASE NOISE ANALYSIS

As discussed in the previous section, RFT in active mode can be realized as VCCS with 270° phase shift between exciting voltage (input) and sensed current (output). In this section, a topology for utilizing this RFT realization to make a mmWave oscillator is proposed, which is followed the discussion of its phase noise performance as compared to the conventional LC oscillators.

### A. Proposed oscillator topology for Active Mode RFT

Fig. 2 depicts the block diagram of an oscillator for active mode RFT. As shown in the figure, the oscillator uses a current to voltage (I-V) conversion stage to convert the out put current of RFT into a voltage quantity. I-V stage is followed by a phase shifter block to provide -90° phase shift such that overall phase shift in the loop becomes 360°, which is one of the Barkhausen criterion for oscillation. Moreover, as shown in Fig. 2, for meeting the gain criteria of oscillation (|loop-gain| ≥ 1) near 30 GHz, a gain stage is also needed in the loop. Since, gain is
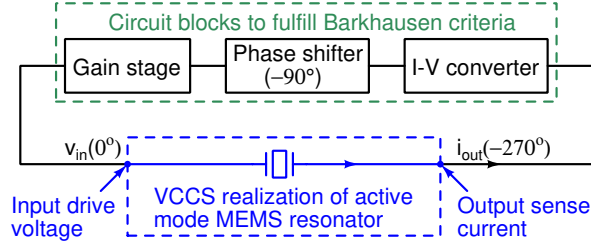
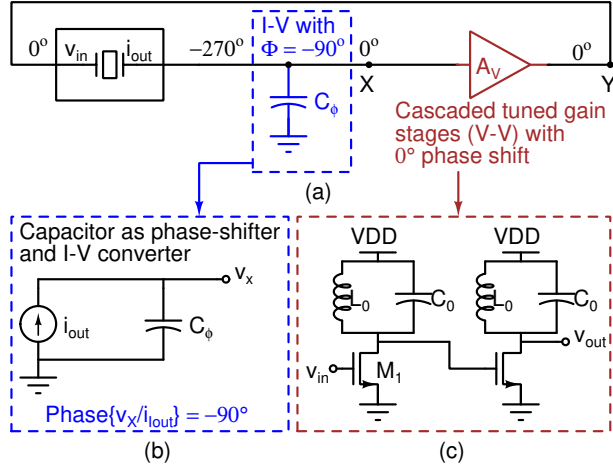Fig. 2. Block diagram of the proposed oscillator with RFT realized as VCCS with 270° phase shift



Fig. 3. (a) Proposed oscillator topology, (b) a capacitor as -90 ° phase shifter and I-V converter and (c) cascaded tuned gain stages

only needed around 30 GHz, a tuned gain stage will be more suitable for the design. The placement of I-V stage, phase-shifter and gain stage can be in any order depending on the way these blocks are realized.

Fig. 3(a) shows the block diagram of the proposed oscillator topology with the help of half circuit model of RFT. As shown in the figure, we propose a capacitor ($C_\phi$) as an I-V converter as well as phase shifter unit (Fig. 3(b)), which can provide -90° phase shift between output voltage and input current. Moreover, for providing sufficient gain near 30 GHz without adding any extra phase shift, cascade of tuned common-source amplifier stages (Fig. 3(c)) are used in the proposed topology.

Fig. 4(a) shows the complete schematic of the proposed active mode oscillator, where $C_B$ is the coupling capacitor between $C_\phi$ and sense output of the active mode RFT. In the figure, $V_{BIAS}$ and $R_B$ are the bias voltage and resistance, respectively, which are used to bias the first stage ($M_1$) of the tuned amplifier. Second stage ($M_2$) of the amplifier is directly coupled to the first stage. The inductor value of $L_0$ in the tuned loads has been chosen such that the static capacitance ($C_0$) of RFT can be utilized in the load tank of the second gain stage. Same values of tank components are used in the first stage of the amplifier. As shown in [4], due to the resonance

of $C_0$ with $L_0$, the overall Q-factor of inductor compensated resonator will not get affected if the Q factor of RFT is $> 2K$. Therefore, the advantage of high-Q factor will still be there. It is important that phase shift from $C_\phi$ should be -90° at the desired frequency of operation ($f_0 = 30$ GHz). In Fig. 4(a), for $R_B >> R_0$, net resistance at node A will be $R_B || R_0 \approx R_0$ and phase shift from $C_\phi$ will be $\phi_{C_\phi} = -tan^{-1}(\omega_0 R_0 C_\phi)$. For $\phi_{C_\phi} = $-90° , $R_0 >> \frac{1}{\omega_0 C_\phi}$. Therefore, value of $|\omega_0 C_\phi|$ should be sufficiently large for achieving -90° phase shift. At the same time $C_\phi$ should be small enough as compared to $C_B$ in order to avoid any signal attenuation due to capacitive division. Since oscillation frequency is very high (30 GHz), a reasonable value of $C_\phi$ can be used. In fact, input capacitance of the first stage ($M_1$) of tuned amplifier can also be utilized as $C_\phi$.

*B. Phase noise performance of the proposed topology*

Phase noise (PN) in dBc/Hz of an oscillator at an offset ($\Delta\omega$) can be defined by Eq. (1).

$$PN = 10log\frac{P_{noise}}{BW \times P_{carrier}} \quad (1)$$

where, $\frac{P_{noise}}{BW}$ is the noise power density at $\Delta\omega$, in a bandwidth $BW$ and $P_{carrier}$ is the carrier power. For an ideal scenario, the minimum achievable phase noise can be calculated by considering loop gain of 1 and noise power ($S_0$) contribution from active-mode resonator only and assuming no noise from gain stages. There are three major noise sources in the active-mode resonator - 1) thermal noise ($S_{th_{R_m}} = 4KTR_m$) due to $R_m$, 2) thermal noise ($S_{th_{sense}} = 4KT\gamma g_m R_0^2$) of sense transistor and 3) flicker noise ($S_{1/f} = \frac{k_{i/f,n}}{f_0 WLC_{ox}} g_m^2 R_0^2$) of FinFET at the sense output which affects its $g_m$. Phase noise can be calculated by considering noise shaping as defined by Leesons heuristic model for the oscillator noise spectrum, which shows the relationship between the phase noise power spectral density ($S_\phi(\Delta\omega)$) at an offset of $\Delta\omega$ from $\omega_0$ and the known parameters of the oscillator such as carrier power levels, noise of the active devices and tank characteristics [9]. Eq. (2) shows the Leeson's equation, where Q is the quality factor of the resonant tank and $S_0$ is the effective noise power generated by the oscillator circuit [9].

$$S_\phi(\Delta\omega) = \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 S_0 \quad (2)$$

For ideal case described above, $S_0$ can be given as follows.

$$S_0 = 4KTR_m + 4KT\gamma g_m R_0^2 + \frac{k_{i/f,n}}{f_0 WLC_{ox}} g_m^2 R_0^2 \quad (3)$$

Using equations (2) and (3), $P_{noise}$ can be calculated as follows.

$$P_{noise} = S_0 \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \frac{V^2}{Hz} \quad (4)$$

For $R_m$ = 332 Ω, Q = 10,000, $\omega_0$ = 30 GHz, $\Delta\omega$ = 1 MHz, $R_0$ = 2 kΩ, $\gamma$ = 3 (for short channel device), noise contributions from sense transistor can be ignored as compared to $R_m$ and $S_0 \approx S_{th_{R_m}}$. Therefore, for ideal scenario, $10logP_{noise} \approx$
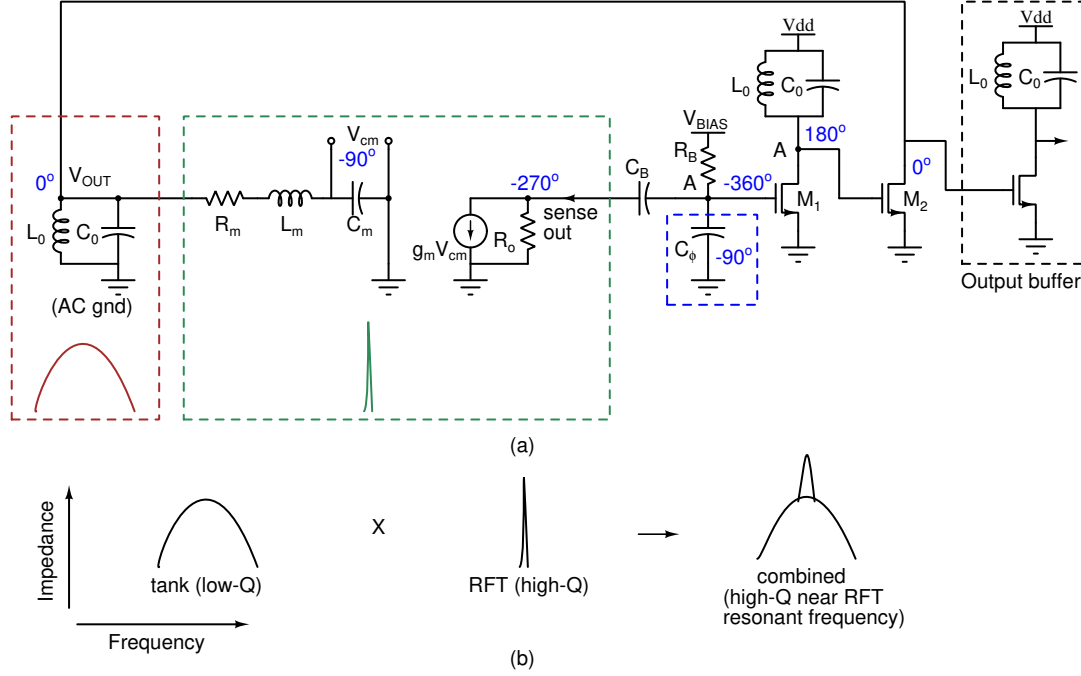
Fig. 4. (a) Schematic of the proposed oscillator circuit and (b) intuitive depiction for phase noise improvement due to overall high-Q factor in the loop

-169 dB/Hz. In Eq. 1, $P_{carrier} = V^2_{OSC-AMP}/2$, where $V_{OSC-AMP}$ is the oscillation amplitude. Considering maximum amplitude equal to $\frac{1}{2}$ V, $P_{carrier}$ = -6 dB. Therefore, for ideal scenario minimum achievable PN = -163 dBc/Hz. This significantly low PN is mainly due to the high Q factor of the resonator. Even if the noise contributions from other parts of the circuits are considered, with the proposed topology, a significant improvement in PN can be guaranteed over the traditional LC oscillators.

Fig. 4(b) presents an intuitive explanation that how does the phase noise improvement occur in the proposed topology as compared to a typical LC oscillator. As shown in Fig. 4(b), the high-Q RFT and low-Q tank ($L_0 C_0$) are cascaded in the topology and their resonances are also aligned in the same directions. The overall Q of the oscillator at the resonance frequency is governed by high-Q of the RFT, which maximize the noise filtering at the resonant frequency and considerably improves the phase noise of the oscillator ($PN \propto \frac{1}{Q^2}$).

## IV. IMPLEMENTATION AND SIMULATION RESULTS

The proposed circuit shown in Fig. 4(a) has been implemented in 14 nm GF technology. In the design shown in Fig. 4(a), transistor $M_1$ is designed in such a way that its input capacitance has been utilized as $C_\phi$. Fig. 5 shows the layout of the circuit, which occupies $42\mu$m $\times$ $100\mu$m. Active mode RFT has been modelled with its electrical equivalent shown in Fig. 1(c) for the simulations, for which following parameters have been used at 30 GHz : $Q = 10\ K$, $R_m = 332\ \Omega$, $L_m = 17.59\ \mu H$, $C_m = 1.6\ aF$ and $C_0 = 16\ fF$ and $g_m = 1\ \mu S$, $R_0 = 2\ K\Omega$ [2], [1], [4]. For the design, foundry
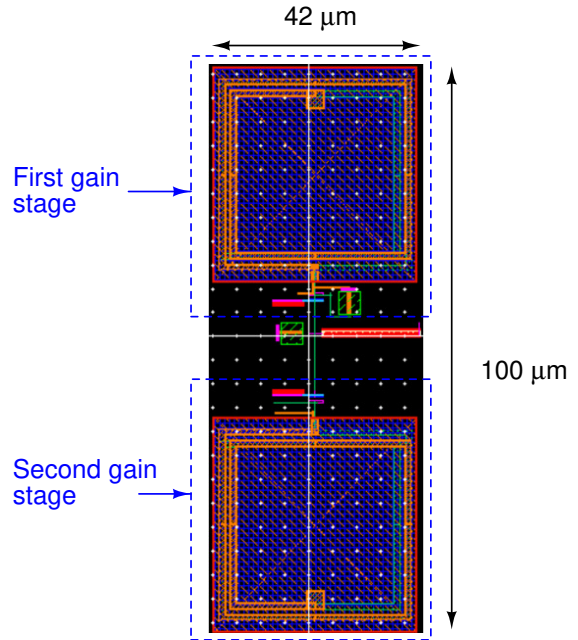


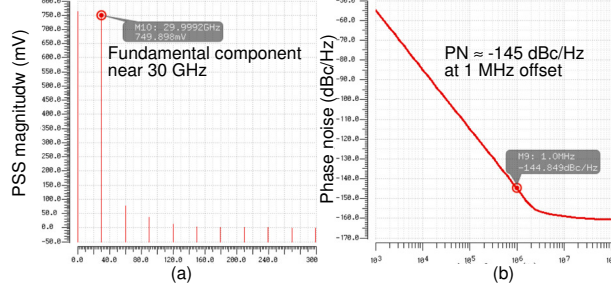Fig. 5. Layout of the proposed oscillator

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Fig. 6. Simulation results showing oscillator (a) spectrum near 30 GHz and (b) its phase noise
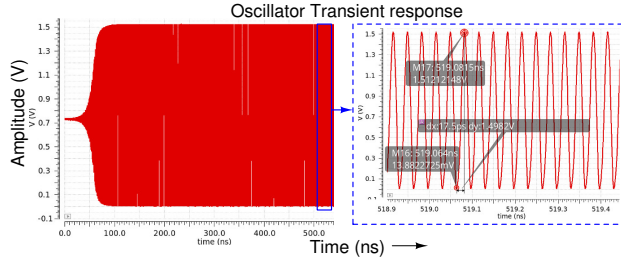


Fig. 7. Simulation results showing transient response of the proposed oscillator (Q=10K)



Fig. 8. Simulation results showing (a) phase noise across process corners (Q=10K) and (b) phase noise for oscillator with Q=1K

inductor was taken as $L_0$ =650 pH, which is valid for 30 GHz. For the gain stage transistor size, post layout extraction showed that its $C_{in}$ was about 5 fF, therefore $C_{in}$ has been utilized as $C_\phi$. With $C_\phi \approx 5$ fF, the condition $R_0 >> \frac{1}{\omega_0 C_\phi}$ gets satisfied for -90° phase shift from $C_\phi$, while providing I-V conversion as discussed in section III-B. Coupling capacitance ($C_B$) of 20 fF was used in the design. For this a MIM capacitor from the foundry PDK was used. Since, at 30 GHz the extracted design will have parasitic capacitances, inductances and resistances, the design was optimized through simulation iterations. The proposed oscillator design consumes about 5.5 mW power from 800 mV supply.

Fig. 6(a) and Fig. 6(b) show the oscillator spectrum near 30 GHz and its phase noise, respectively. As shown in Fig. 6(b), the simulated phase noise at 1 MHz offset for 30 GHz carrier frequency is $< -144$ dBc/Hz for Q = 10K. Fig. 7 shows the transient response of the oscillator. As shown in the figure, oscillator start-up time is about 80 ns. Fig. 8(a) shows the phase noise simulation results across the transistor process corners for Q=10,000. As sown in the figure, phase noise remains <-143 dBc/Hz at 1 MHz offset. Fig. 8(b) shows the phase noise result for active mode resonator with Q=1K, which is about 17 dB worse than the Q=10K case.

As discussed in section III-C and shown in Fig. 4(b), phase noise improvement in the proposed topology is primarily obtained due to the cascade of two resonant tanks, which results in an overall high Q value in the oscillator's feedback loop. However, any variation in $L_0 C_0$ values may cause misalignment of resonant frequencies of tuned gain stage and
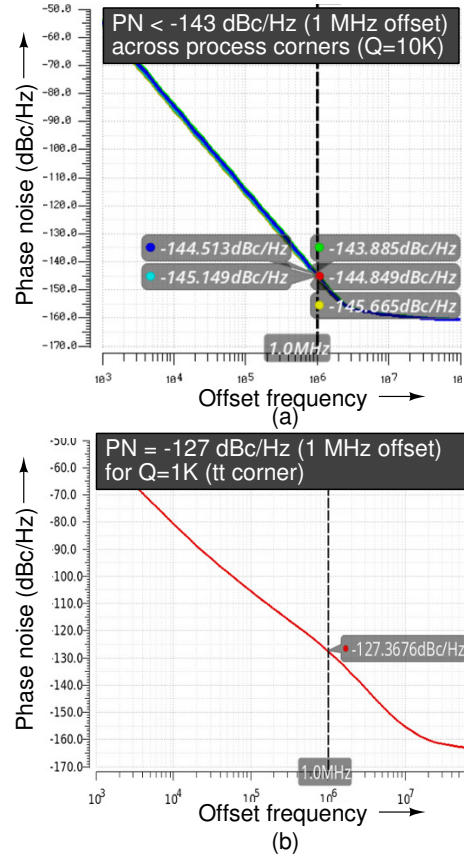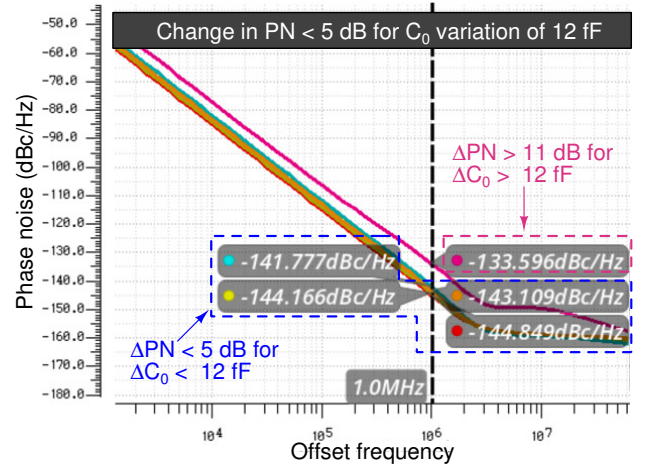


Fig. 9. Phase noise variation due to variation in $C_0$ resulting in change in $L_0 C_0$ tank's resonant frequency with respect to RFT's resonant frequency

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON

| Parameters | [10] | [11] | [12] | [13] | This work |
|---|---|---|---|---|---|
| Measured/ Simulated | Measured | Measured | Measured | Measured | Simulated |
| Technology | 65 nm CMOS | 65 nm CMOS | 28 nm CMOS | 135 nm BiCMOS | 14 nm CMOS |
| Frequency | 29.92 GHz | 28 GHz | 25.56 GHz | 15 GHz | 30 GHz |
| Type | LC | LC | LC | LC | MEMS [2] |
| Oscillator Phase Noise | -112.3 dBc/Hz | $> -110$ dBc/Hz | -102.4 dBc/Hz | -124 dBc/Hz | $-127$ dBc/Hz (Q=1K) $-144$ dBc/Hz (Q=10K) |
| (offset) | (1 MHz) | (1 MHz) | (1 MHz) | (1 MHz) | (1 MHz) |
| Power | 4 mW | 17.5 mW | 5.5 mW | 72 mW | 5.5 mW |
| Supply | 0.48 V | 0.65 V | 0.9 V | 3 V | 0.8 V |

active mode RFT (Fig. 4) resulting into overall Q degradation, which will cause phase noise degradation. However, since the resonant peaks are aligned in same direction, therefore for slight resonant frequency variations, noise peaking in the oscillator's feedback loop will still happen near active-mode resonator's frequency ($f_0$) and oscillations will build up with good quality. Fig. 9 shows this effect, where phase noise variation with respect to the change in $C_0$ values over a range of 12 fF are plotted for Q=10K case. As shown in Fig. 9, the degradation in phase noise ($\Delta PN$) is $< 5$ dB for a variation of 12 fF value in $C_0$. Table I shows the performance summary and the comparison with other mm-Wave oscillators. As compared to the other works, the proposed circuit with active mode of RFT provides more than 20 dB improvement in phase noise, while consuming sufficiently low power.

## V. CONCLUSION

In this work, we proposed a low phase noise oscillator topology for an active mode resonant fin transistor (RFT) with a very high quality factor (10,000) in MEMS technology. RFT uses active FET sensing to harness the high-quality, high-yield MOSFETs available in CMOS technologies and can provide fully monolithic solution for mmWave signals. This research presented the potential of utilizing fully monolithic active mode RFT based resonators for realizing low phase noise oscillators beyond conventional LC oscillators. The proposed topology has been validated by the design and simulation of a 30 GHz oscillator in GlobalFoundries's 14 nm FinFET technology. For an active mode RFT with Q-factor of 10,000, simulation results showed that the proposed oscillator consumes about 5.5 mW of the power from 0.8 V supply and exhibits phase noise less than -144 dBc/Hz at 1 MHz offset for 30 GHz carrier, which is $> 20$ dB better than that for the existing LC oscillators.

## ACKNOWLEDGEMENT

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