16.6 A 65nm 63.3μW 15Mbps Transceiver with Switched-Capacitor Adiabatic Signaling and Combinatorial-Pulse-Position Modulation for Body-Worn Video-Sensing AR Nodes

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Recent advances in audio-visual augmented reality (AR) and virtual reality (VR) demands 1) high speed (>10Mbps) data transfer among wearable devices around the human body with 2) low transceiver (TRX) power consumption for longer lifetime, especially as communication energy/b is often orders of magnitude higher than computation energy/switching. While WiFi can transmit compressed video (HD 30fps, compressed @6-12Mbps), it consumes 50-to-400mW power. Bluetooth, on the other hand, is not designed for video transfer. New mm-Wave links can support the required bandwidth but do not support ultra-low-power (<1mW). In recent years, Human-Body Communication (HBC) [1-6] has emerged as a promising low-power alternative to traditional wireless communication. However, previous implementations of HBC transmitters (Tx) suffer from a large plate-to-plate capacitance (C_P, between signal electrode and local ground of the transmitter) which results in a power consumption of $\alpha C_P V^2 f$ (Fig. 16.6.1) in voltage-mode (VM) HBC. The recently proposed Resonant HBC [6] tries to overcome this problem by resonating C_P with a parallel inductor (L). However, the operating frequency is usually < a few 10's of MHz for low-power Electro-Quasistatic (EQS) operation, resulting in a large/bulky inductor. Moreover, the resonant LC_P circuit has a large settling time ($\approx 5Q^2RC_P$, where R is the effective series resistance of the inductor) for EQS frequencies which will limit the maximum symbol rate to <1MSps for a 21MHz carrier (the IEEE 802.15.6 standard for HBC), making resonant HBC infeasible for >10Mb/s applications.

Realizing that the primary source of power consumption (C_P) for VM capacitive HBC is similar to digital computing circuits (as opposed to wireless radio communication with a 50Ω resistive load), we present, for the first time: 1) Adiabatic communication which breaks the $\alpha C_P V^2 f$ limit for power consumption, and 2) Combinatorial Pulse-Position Modulation (CPPM), which reduces α (activity factor) by reducing the number of transitions/b, effectively increasing information/energy. Adiabatic switching (AS) approximates a slow, linear ramp using n-step charging and discharging, reducing the power consumption by ≈40% (144.4μW to 85.7μW @2.5MSps) w.r.t. CMOS switching with OOK (1b/symbol), which is further reduced to 51.9μW (~3.5pJ/b) with CPPM (6b/symbol). The energy efficiency including clocking power is ≈4.2pJ/b (improvement of >2.5× over the state-of-the-art) without the need for bulky inductors [6] or magnetic coils [4]. The test chip with adiabatic EQS HBC+CPPM is implemented in 65nm CMOS (Fig. 16.6.2, top), featuring 1) a 4.2pJ/b digital-friendly Tx with on-chip clock, programmable digital modulation (OOK, CPPM, RZ/NRZ) and AS driver, 2) a 4pJ/b integrating receiver (Rx) with fully digital Clock Data Recovery (CDR) and a demodulator.

Inspired by NASA's previous designs for Satellite Communication [7], we minimize energy/information by adopting CPPM in the custom ASIC and choosing only those codes that represent high number of combinations with low number of transitions. Figure 16.6.2 describes the CPPM encoding for reducing the number of transitions per bit. 8 cycles of a 20MHz carrier are considered as a symbol (resulting in 2.5MSps symbol rate), with each cycle being considered as a slot where information may be present. Slot 1 in each symbol is always filled, which is used to detect the start of the symbol. Any, none or multiple of the remaining 7 slots can be filled, based on the CPPM encoding. The number of filled slots (N) will result in a number of combinations (${}^7C_N$) which can be used to encode multiple b/symbol. For example, 3 filled slots out of 7 results in 35 combinations which can encode 5b/symbol. CPPM can utilize either NRZ (filled slot = digital 1, empty slot = digital 0) or RZ signaling (NRZ signal multiplied with the 20MHz clock). For RZ, the number of transitions per symbol (and thereby power) increases linearly with increasing N, while b/symbol first increases and then decreases due to the nature of ${}^7C_N$. Hence, the pJ/b for RZ increases sub-linearly for N=0 to 3 and super-linearly for N=4 to 7. For NRZ, the number of transitions follow the nature of ${}^7C_N$ and hence the pJ/b stays relatively constant with N. Hence, to increase the amount of information while keeping pJ/b low, we chose to operate with N=0 to 3. To further maximize b/symbol, we utilize multiple combinations of N. For example, N=0 (${}^7C_N$=1) and N=1 (${}^7C_N$=7) together produce 8 combinations which can be utilized to encode 3b (called CPPM-3b), while N=0 and N=1 separately could encode only 0 and 2 bits, respectively. Using this approach, N=0 (${}^7C_N$=1), N=1 (${}^7C_N$=7), N=2 (${}^7C_N$=21) and N=3 (${}^7C_N$=35) together produce 64 combinations which is utilized to encode 6b (called CPPM-6b). The average number of transitions/b for CPPM-3b, CPPM-4b, CPPM-5b, and CPPM-6b are 1, 0.875, 0.75 and 0.82, respectively for NRZ, and 1.25, 1.22, 1.125 and 1.135, respectively for RZ, as compared to the average of 4 transitions/b for OOK and 2 transitions/b for 16-PSK (@ 2.5MSps, 20MHz carrier). By reducing the number of carrier cycles per symbol, and by removing the sync (slot 1), the number of transitions/b can approach the theoretical minimum for broadband (BB) systems (1 transitions/b for BB RZ and 0.5 transitions/b for BB NRZ) at the cost of higher bandwidth, which is acceptable for body channel communication, unlike wireless. On the other hand, the increased number of carrier cycles per symbol will require more registers for deserialization/serialization and less frequent synchronization.

Figure 16.6.3 shows the circuit-level implementation details of the Tx, Rx and clocking sub-systems. The Tx consists of a fully digital modulator and a driver with AS, implemented using 4-step charging/discharging enabled by a switched capacitor circuit. An n-step charging/discharging (n>>4) will better approximate a linear ramp for adiabatic energy benefits, but an n-step AS will require 4n carrier phases to generate the control signals for AS (for charging and discharging both to happen within the phase when modulator output=1), thereby increasing the clocking power and complexity. The Tx clocking is implemented with an 8.3μW, 40MHz crystal oscillator, and then dividing it by 2, which provides 2-phase injection to an 8-stage, 3.1μW, 20MHz differential ring oscillator (DRO) for reduced phase asymmetry. The DRO generates the 16 phases for 4-step AS. The CPPM Rx needs to detect each slot for NRZ CPPM, and each half-slot for RZ CPPM, and hence uses a clock of 20MHz for NRZ and 40MHz for RZ. Thus, the frequency of the DRO needs to be adjusted for the Rx (based on RZ/NRZ modes), and hence the Tx, Rx and clocking systems all run on separate supplies (0.75V for Tx, 1V for Rx, adjustable supply for clocking).

Figure 16.6.4 shows the power consumption and pJ/b of the Tx for different symbol rates, modulation and drivers. AS with CPPM-6b (NRZ) achieves 2.8× lower power and 16.5× lower pJ/b w.r.t. a CMOS driver with OOK at 2.5MSps. CPPM-6b achieves 7.6pJ/b in RZ mode and 3.5pJ/b in NRZ mode (without clocking), and the measured energy-efficiency numbers for various CPPM modes correspond closely with the theoretical number of transitions/b as shown in Fig. 16.6.2. The measured stepwise charging/discharging waveforms are band limited, as shown in Fig. 16.6.4, due to the finite switch resistances. Figure 16.6.5 exhibits the BER, pJ/b and the sensitivity for the Rx for various modes. The BER for CPPM modes is higher than OOK at a particular timing offset (similarly the sensitivity of CPPM modes is worse than OOK) because CPPM needs to detect each slot (cycle of carrier) correctly, while OOK only needs to detect each symbol (8× of the carrier cycle) and hence has less strict timing requirements. Similarly, CPPM in RZ mode performs slightly worse than CPPM in NRZ mode because the Rx works at 40MHz for CPPM in RZ mode, and at 20MHz for CPPM in NRZ mode. The sensitivity of the OOK modes is found to be ≈-65dBm, (≈-52dBM for CPPM) @2.5MSps, 10^{-3} BER. There is no significant degradation due to AS w.r.t. CMOS switching, as the human body works as a band-limited channel, and smoothens the high frequency components in both the output of the CMOS driver and the adiabatic driver.

Figure 16.6.6 compares the test-chip performance with state-of-the-art wearable HBC TRX, exhibiting the best energy efficiency at the Tx (>2.5× improvement vs. [4], with 3× higher data rates), due to adiabatic switching and CPPM (shown for the first time in VM capacitive communication), while demonstrating equivalent pJ/b at the Rx. Figure 16.6.7 shows the chip micrograph with the power breakdown of different subsystems.

Acknowledgment:
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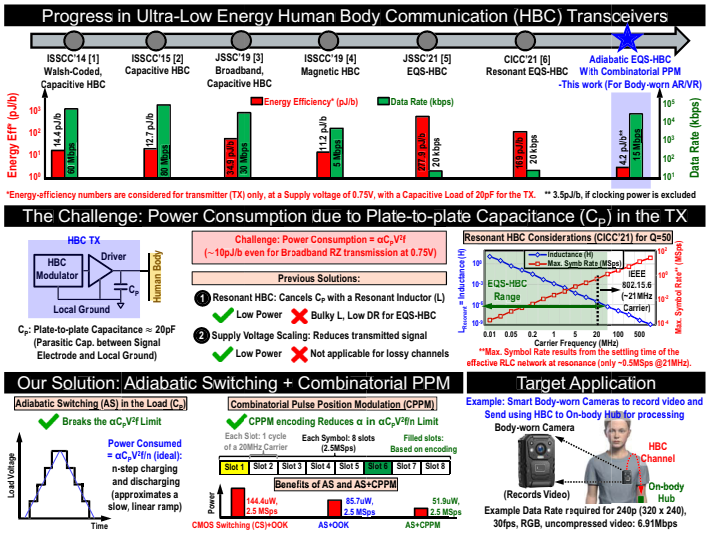


Figure 16.6.1: The challenge in high-speed low-power Electro-Quasistatic (EQS) Human Body Communication (HBC), and the implemented solution with Adiabatic Switching (AS) and Combinatorial Pulse Position Modulation (CPPM).

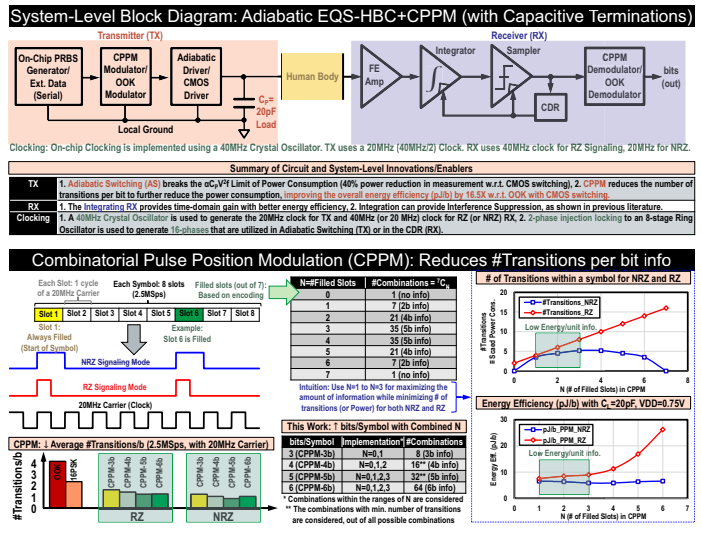


Figure 16.6.2: System-level block Diagram of the adiabatic EQS-HBC IC, with implementation details of CPPM for maximizing b/symbol (combination of N = 0,1,2,3) and minimizing transitions/b info.

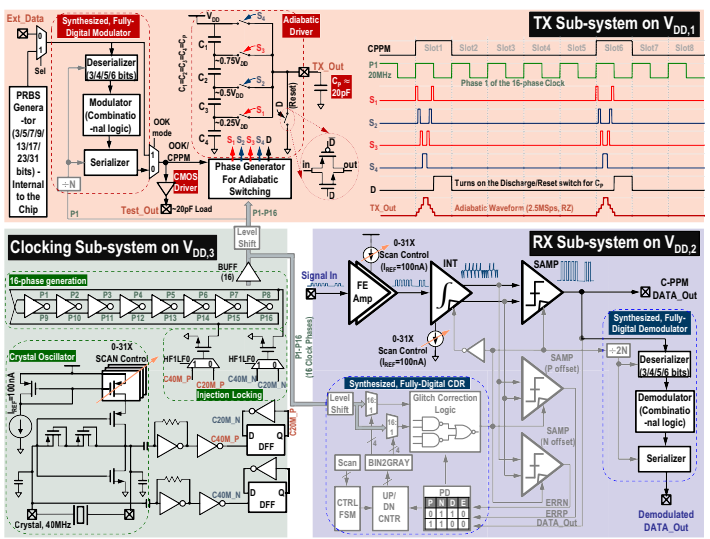


Figure 16.6.3: Circuit implementation and timing diagram of the Tx (with a fully digital modulator and a digital-friendly, switched capacitor-based adiabatic driver), clocking, and Tx sub-systems.

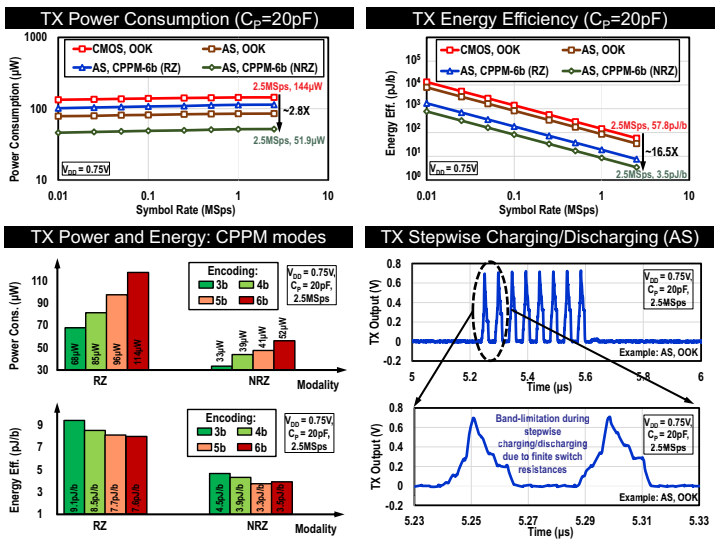


Figure 16.6.4: Tx power consumption and energy efficiency of various modes (CMOS/AS, OOK/CPPM, RZ/NRZ, CPPM 3b/4b/5b/6b) without clocking power, with time-domain adiabatic charging/ discharging waveforms.

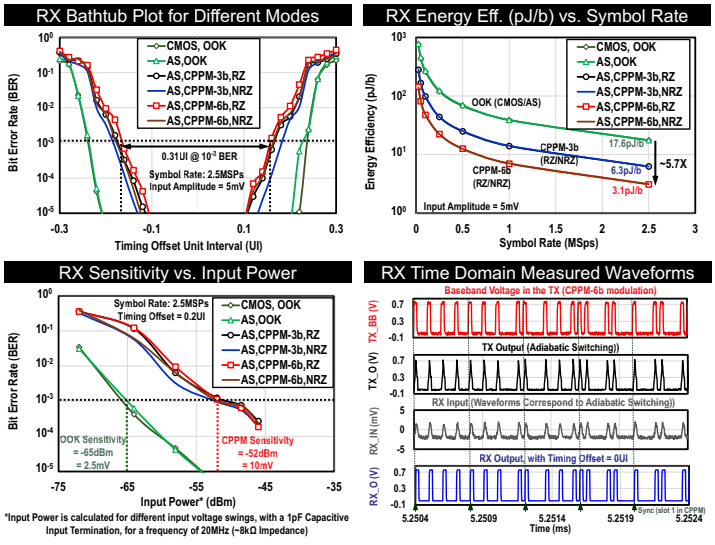
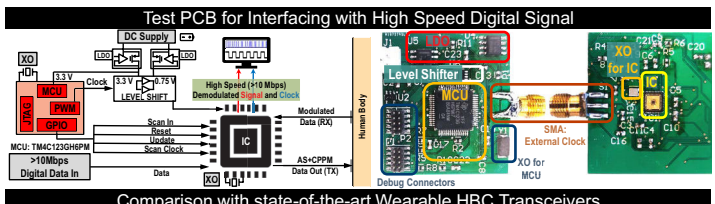


Figure 16.6.5: Rx bathtub plot (BER vs timing offset), energy efficiency and sensitivity of various modes (CMOS/AS, OOK/CPPM, RZ/NRZ), along with time-domain measured waveforms at Tx and Rx.

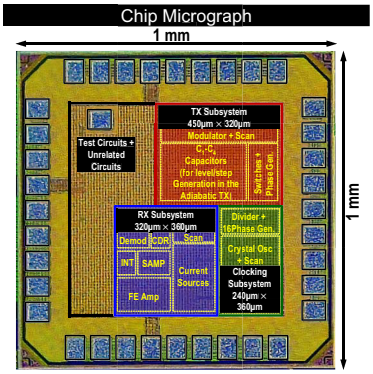


Comparison with state-of-the-art Wearable HBC Transceivers

	This Work	N. Modak CICC'21 [6]	S. Maity JSSC'21 [5]	J. Park ISSCC'19 [4]	S. Maity JSSC'19 [3]	H. Cho ISSCC'15 [2]	J. Lee ISSCC'14 [1]
Technique	Adiabatic Switching + CPPM (3-6 bits)	Resonant, EQS	Capacitive, EQS	Magnetic	Capacitive-Broadband	Capacitive	Capacitive
CMOS Process	65nm	65nm	65nm	65nm	65nm	65nm	65nm
Carrier Freq.	20MHz	0.5-2 MHz	0.05-1MHz	40 MHz	-	140-180 MHz	40-80 MHz
Modulation	OOK and CPPM	OOK	OOK	OOK	NRZ	Coherent BPSK	Walsh Coding
Supply Voltage (V_{DD})	0.75 V	0.5 V	0.5 V	0.6 V	1 V	1.2 V	1.1 V
Data Rate (DR)	7.5Mbps-15Mbps	1-20 kbps	1-20 kbps	5 Mbps	30 Mbps	80 Mbps	60 Mbps
TX Power With 20pF Load (C_P)	63.3μW (NRZ, CPPM-6b) with Clocking	1.5 μW	2.47 μW	35.8 μW	1.86 mW	2.6 mW	1.85 mW
RX Power	60.6μW (NRZ, CPPM-6b) with Clocking + CDR	72 nW (with Clocking + CDR)	1.4 uW	24uW	98 uW	6.3 mW	9.02 mW
TX Energy Eff. (pJ/b) @ C_P=20pF, V_{DD}=0.75V	≈4.2 (NRZ, CPPM-6b) with Clocking	169	277.9	11.2	34.9	12.7	14.4
RX Energy Eff. (pJ/b)	≈4 (NRZ, CPPM-6b) with Clocking + CDR	3.6	140	4.8	3.27 (without clock)	79	150
RX Sensitivity	-65dBm (OOK), -52dBm (CPPM) @10-3 BER	-60 dBm @10-5 BER	-64dBm @10-3 BER	-56 dBm @10-3 BER	-64dBm @10-3 BER	-58 dBm @<10-3 BER	-58 dBm @<10-5 BER

Figure 16.6.6: Comparison with state-of-the-art wearable HBX TRX, showing the improved energy efficiency of AS+CPPM (>2.5× improvement over previous literature in Tx pJ/b), along with test PCB photo.

Chip Micrograph



Technology Specs and Design Summary

Test Chip	Process	65nm 1P9M CMOS LP
	Package	Gold Wire-bond with QFN Packaging, FR4 PCB
AS+ CPPM TX	Supply	0.6V-0.8V (0.75V nominal)
	Active Area	0.144mm² (including Scan for programming)
	Load	20pF Load Cap
	Performance	4.2pJ/b with AS+CPPM(6b), 15Mbps
	IO used	5 (Additional 10 IOs for Scan/tests)
ULP CPPM RX	Supply	0.75V
	Active Area	0.1152mm² (including Scan)
	i/p Termination	Capacitive (20pF)
	Performance	4pJ/b with AS+CPPM(6b), 15Mbps
	IO used	7 (Additional 5 IOs for test outputs)
Clocking	Active Area	0.0864mm² (including Scan)
	IO used	4 (Additional 2 IOs for test outputs)

Power Consumption Summary for CPPM-6b with RZ Signaling

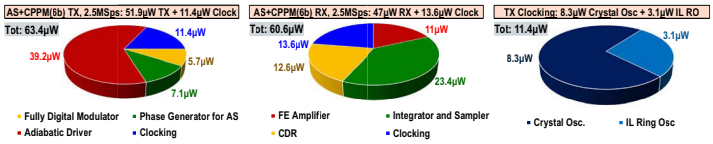


Figure 16.6.7: Chip micrograph, technology specs/design summary of the SoC and power breakdown.

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