1.3–1.55-μm CMOS/InP Optoelectronic Receiver Using a Self-Aligned Wafer Level Integration Technology

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***Abstract*—A heterogeneous 10-Gb/s 1.3- to 1.55-μm optoelectronic receiver is designed and fabricated using a complementary metal–oxide–semiconductor transimpedance amplifier and an InGaAs–InP PIN (p-type, intrinsic, n-type diode) photodiode. The receiver is heterogeneously integrated based on a batch fabrication process which promises low fabrication cost. The receiver measures a transimpedance gain of higher than 50 dB $\cdot\Omega$ over a bandwidth of 6 GHz and demonstrates an open eye diagram with a 1.55-μm 10-Gb/s light source.**

***Index Terms*—Advanced electronic packaging, complementary metal–oxide–semiconductor (CMOS) analog integrated circuits, optoelectronic receiver, PIN photodiode, transimpedance amplifier.**

I. Introduction

LOW-COST wideband optical communication systems are an essential part of the expanding communication market due to their high data rate, extremely high channel capacity, and insensitivity to electrical interference. The receiver systems often use a high-gain transimpedance amplifier in conjunction with a photodiode to transform the optical signal into electrical signal. They are traditionally built using either hybrid or monolithic approaches based on high-speed bipolar or InP high electron mobility transistor technologies.

In hybrid receivers, a photodiode is fabricated on a separate die from the amplifier. The two components are either packaged separately or together using an optical package. A loss in sensitivity of hybrid optoelectronic receivers due to small area of the PIN photodiodes is a consequence of extra parasitic capacitances of the hybrid implementation. In monolithic optoelectronic receivers, the transistors of the amplifier and photodiode are built on a common substrate using either shared heterostructure (same heterostructure for transistor and PIN diode) or stacked heterostructure (PIN structure is grown on top of the transistor heterostructure). The advantages of using monolithic optical receivers are their smaller size and higher data rate for a given optical power sensitivity, when compared with their hybrid counterparts. The drawbacks of using monolithic optical receivers are the high cost associated with integrating photodiode and transistor technology and tradeoffs between the speed of the transistor and the sensitivity of the photodiode when utilizing a common heterostructure approach [1], [2].

Integrated photodetectors based on silicon complementary metal–oxide–semiconductor (CMOS) technology have been recently reported in the literature for the visible spectrum [3]–[5]. The work presented in [3] is at low data rates (3 Gb/s) while [4] and [5] present high-data-rate application (10–15 Gb/s) using the silicon-on-insulator process for the visible spectrum. An apparent performance degradation reported in [5] is due to bondwire inductance as well as bond pad and other parasitic capacitances. None of these reported technologies are appropriate for long-haul communication systems as the wavelength is not compatible with optimum spectrum for optical fibers (near infrared wavelengths of $1.3 \sim 1.55$ μm). Due to low absorption of Si around near infrared, current long-haul 10- and 40-Gb/s systems are only realized in InP technology [6].

The obvious solution to achieve high sensitivity Si-based optoelectronic systems for long-haul communications is to heterogeneously integrate InP or GaAs photodiodes with Si circuitry. Along this path, fluidic self-assembly of microstructures on Si substrate has been demonstrated by Smith *et al.* [7]. In this technique, GaAs light-emitting diode microstructures with trapezoidal shapes suspended in a fluid are self-assembled onto trapezoidal holes etched in Si substrate through fluidic transportation. The technique has not been applied to integration of Si devices/circuits and InP photodiodes for optoelectronic receiver applications.

In this work, we have demonstrated for the first time a heterogeneous 10-Gb/s Si-based optoelectronic receiver at near infrared spectrum. Fig. 1 shows the circuit schematic and the integration concept. A 0.13-μm RF CMOS technology is used to design a two-stage cascode transimpedance amplifier circuit with a gain of 51 dB $\cdot\Omega$ over a bandwidth of 6.4 GHz, although any commercial transimpedance amplifier can also be used. The cascode configuration eliminates the bandwidth degradation due to the Miller effect. This bandwidth degradation is significant in deep submicron CMOS circuits, where the gate-drain capacitance can be as high as gate-source capacitance.

The shunt–shunt feedback (R_1 and L_2) lowers the input impedance of the amplifier such that most of the photocurrent couples to the amplifier instead of the parasitic capacitance of the PIN diode. In order to increase the bandwidth, a small series inductor L_1 is inserted between the transistor's gate terminal and PIN diode. This inductor generates a third-order

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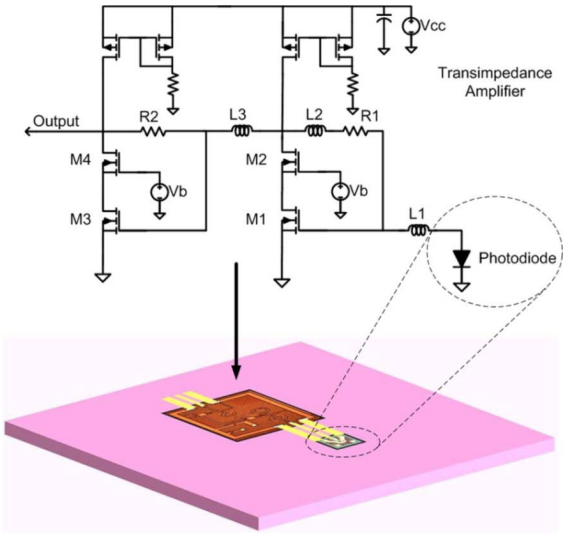

Fig. 1. Schematic and concept of a heterogeneous optical receiver using a CMOS transimpedance amplifier and an InP PIN photodiode.

low-pass filter with the parasitic capacitance of the PIN diode and the input capacitance of the amplifier. Inductor L_3 is used to separate output capacitance of TIA from the capacitance of the next stage. These inductors also cause peaking in the gain response. P-channel metal–oxide–semiconductor current mirrors are used to feed both amplifying stages.

By tightly integrating the wideband CMOS transimpedance amplifier with a commercial InGaAs–InP PIN photodiode, we have substantially reduced parasitic capacitances and inductances between the two chips. As a result, a CMOS-based 10-Gb/s optical receiver operating at 1.55-μm wavelength is made possible.

II. Technology

In [8], we have reported a self-aligned wafer-level integration technology (SAWLIT) suitable for a microwave integrated circuit. The technology is applied to integrate a 10-GHz CMOS receiver chip with embedded passive components and a 10-GHz filter. In this work, we have utilized the process to tightly integrate two disparate chips, namely the designed RF CMOS amplifier and a commercial 1310- to 1550-nm InGaAs–InP PIN photodiode from Microsemi. Heterogeneous integration of the two chips using SAWLIT offers several advantages over current integration and packaging schemes. In fact, the requirement of good performance and low cost at high operating frequencies cannot be achieved either by monolithic or hybrid approaches. It is the synergistic development of technologies that will enable excellent performance while constraining costs and achieving multifuntionality and agility. Therefore, the impact of the proposed technology on the high-speed optoelectronic receivers is to achieve monolithic performance using hybrid heterogeneous integration by tightly integrating various optimized chips and components.

SAWLIT provides many advantages over current integration schemes. Some of these advantages are listed below and are explained in more detail in [9] and [10].

1) Single substrate solution: The entire system, including CMOS transimpedance amplifier and InP PIN photodiode, can be integrated into a single Si substrate.
2) Batch fabrication: Due to self-aligned placing of the chips inside the carrier substrate, the integration process can be done in a batch fabrication.
3) Minimum parasitic inductance and electromagnetic interference: Parasitic inductance and associated delays due to wirebond as well as electromagnetic interference are eliminated due to tight integration.
4) Heterogeneous integration: This approach allows various optimized chip and component technologies to be combined to obtain improved overall performance.
5) Embedded passives including antennas and transmission lines can be added on carrier substrate. Their performance (loss, bandwidth, quality factor, and self-resonance frequency) can be independently optimized.
6) Low-loss coplanar waveguide (CPW) transmission lines essential for high-frequency design can be utilized on high resistivity Si carrier substrate.
7) Time to market for integrated systems can be minimized. This is achieved through modifying only passive components (frequency tuning, matching) on carrier substrate, while keeping the active design intact.
8) Low cost of the integrated system due to batch fabrication process.

The integration technology is briefly described in this section. The details of the integration technology are provided elsewhere [8], [9]. First, the Si carrier substrate is etched using a deep reactive ion etcher with holes slightly larger ($\sim$20 μm) than the size of the two chips. Then the chips are inserted in the holes and are self-positioned while the gap between the chips and Si substrate is filled with polydimethylsilicone. After applying a planarization layer (SU-8) and opening vias, chip-to-substrate interconnects are printed using photolithographic defined metallization with very narrow width (25 μm). This is essential for 10-Gb/s operation of heterogeneous optoelectronic receivers as extra parasitic capacitances at the input of the transimpedance amplifier or the output of PIN diode can severely limit the bandwidth of the system.

Using the proposed heterogeneous integration technology, the designed CMOS transimpedance amplifier and a commercial 1310- to 1550-nm InGaAs–InP PIN photodiode are integrated on a high resistivity silicon carrier substrate. The size of the PIN diode chip is 450 μm $\times$ 450 μm with pad size of 75 μm $\times$ 75 μm. The PIN photodiode in Fig. 1 is modeled with a parallel junction capacitance, a current source, a small series resistance, and a shunt pad capacitance. The junction capacitance value of the diode is 200 fF at a bias voltage of 5 V. In order to improve the output matching of the transimpedance amplifier, an embedded series inductor (1 nH) is added to the output of the amplifier on the carrier substrate. Fig. 2 illustrates the integration of the optical receiver. Ideally, if a photodiode with much smaller pad size is available (less than 25 μm $\times$ 25 μm which results in $\sim$1/10 of pad capacitance), it can be integrated using SAWLIT but not wirebond. This will be the true distinction of the proposed technique.

III. Characterization

Agilent 8722 network analyzer with on-wafer probe measurement is used to measure the S-parameters of the heterogeneous optoelectronic receiver. Transimpedance gain is found from measured S-parameters. Fig. 3(a) shows simulated and measured transimpedance gain of the system. The measured

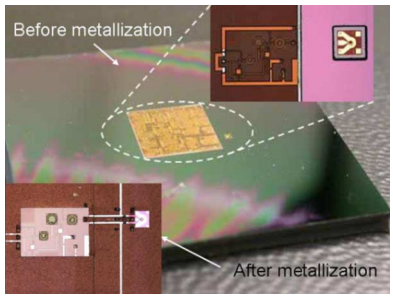

Fig. 2. Integration of the optical receiver using SAWLIT. The 3-μm Au interconnect metallization is printed to connect the two chips.

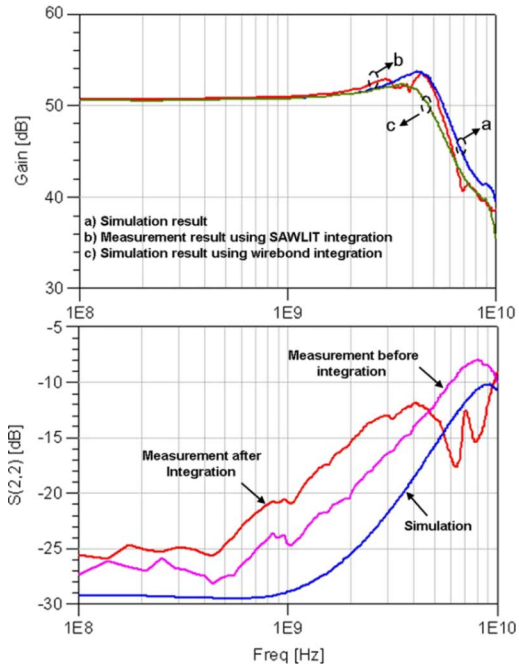

Fig. 3. (Top) Simulated and measured transimpedance gain of the optoelectronic receiver. (Bottom) Simulated and measured output matching of the amplifier.

transimpedance bandwidth ($=$ 6 GHz) is slightly degraded compared to the simulation results due to the parasitic capacitance of the SAWLIT approach and limited accuracy of transistor models. Also shown in Fig. 3(a) is simulated transimpedance gain of the receiver when a 1-mm wirebond is used to attach the PIN diode to the amplifier. Bondwire inductance and parasitic capacitances of the bond pads degrade the bandwidth of the circuit to 5 GHz. Fig. 3(b) shows the simulated and measured output reflection coefficient S_{22}. A 1-nH embedded inductor integrated to the output of the transimpedance amplifier improves the output matching to better than 10 dB over the bandwidth of the receiver. The overall power dissipation of the chip using a 2-V power supply is 45 mW.

An eye-diagram measurement is performed using a 10-Gb/s 1.55-μm modulated laser source and a Tektronix OTS 9010 pseudorandom pattern generator gated with a word length of $2^{31} - 1$. A CPW RF probe is used to feed the output signal of the optoelectronic system to an HP 54120B sampling oscilloscope. A -10-dBm optical signal is applied through a fiber optic to the optoelectronic system. Fig. 4 shows the measured

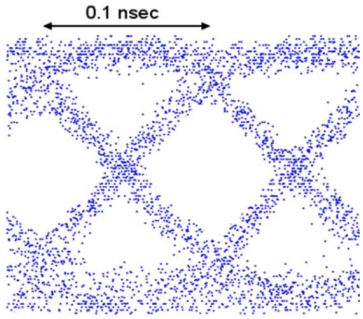

Fig. 4. Eye-diagram measurement of the optoelectronic receiver using a -10-dBm power gated with a $2^{31} - 1$ pseudorandom pattern with 1.55-μm light source at 10 Gb/s.

results indicating open eye characteristics at 10-Gb/s input data rate. The receiver shows an open eye with source power of -12 to $+6.9$ dBm.

IV. Conclusion

Heterogeneous integration of a high-gain (51 dB $\cdot\,\Omega$) CMOS transimpedance amplifier implemented in 0.13-μm CMOS process with an InGaAs–InP photodiode is demonstrated using an SAWLIT. The integration process is suitable for low-cost high-performance heterogeneous systems as batch integration is made possible. The heterogeneously integrated optoelectronic receiver achieves a 10-Gb/s performance at near infrared wavelengths (1.3–1.55 μm).

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