Self-Aligned Wafer-Level Integration Technology With High-Density Interconnects and Embedded Passives

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***Abstract*—This paper presents a polymer-based wafer-level integration technology suitable for integrating RF and mixed-signal circuits and systems. In this technology, disparate dies can be integrated together using a batch fabrication process. Very high density die-to-die interconnects with widths currently as small as 25 μm are implemented. To demonstrate the capabilities of this technology, a 10-GHz receiver front-end implemented in 0.18-μm CMOS technology is integrated with a high-resistivity Si substrate and embedded passives. By adjusting the input matching of the receiver using the embedded passives fabricated on the high-resistivity Si substrate, the input matching and conversion gain of the front-end receiver are improved.**

***Index Terms*—Heterogeneous integration, packaging, system-on-chip (SOC), system-on-package (SIP), wafer-scale integration.**

I. Introduction

ADVANCED electronic packaging is a multidisciplinary research and development area that contains various technologies such as electronic circuit design and fabrication, thermal analysis and design, material characterization, and electronic and mechanical testing. The worldwide electronic packaging market is expected to grow at an annual rate of 7.9% and reach nearly $20 billion by 2007 [1]. One of the most critical levels of electronic packaging is the packaging and interconnecting of integrated circuit (ICs) and semiconductor devices [2]. There are two main IC packaging concepts, namely system on chip (SOC), where the complete system is integrated into a single chip and system in a package (SIP) or system on a package (SOP) where the integration is done using the IC package.

In SOC technology, all the necessary electronic components for a "system" are placed on a single integrated circuit (IC), known as a microchip. For example, a SOC for a wireless communication device might include a receiver radio frequency (RF) front-end, an intermediate frequency (IF) variable gain stage, an analog-to-digital converter (ADC), and a micro-controller with embedded memory, all on a single microchip. If the integration of all the components is realized, SOC offers the most compact, light-weight system that can be mass produced. While SOC might be a good approach for systems with homogeneous technology requirement, it does not provide a cost-effective solution for most complete end-product systems. The high costs are due to the need to integrate active but disparate devices such as SiGe bipolar, CMOS, and optoelectronic components in one chip using several mask steps [3]. Among SOC challenges are the long design times due to integration complexities, high test and fabrication costs, mixed-signal processing complexities, and intellectual property issues.

Unlike SOC that is implemented on a single chip, SIP contains several chips integrated to form a complete system on a ceramic or laminate substrate. An SIP is a multichip module (MCM) that contains all the components of a complete system. In general, SIPs are based on four mainstream technology categories: modules, stacked-die, MCM, and 3-D packaging. Modules are fully functional subsystems with a substrate, one or multiple dies, chip-level interconnects (wire-bond or flip-chip), integrated or surface-mounted passive and active components, and a protective casing [4]. Stacked-die packages are two or more vertically stacked dies that have been packaged with chip-level interconnects (wire-bond or flip-chip) on a laminate, ceramic, flex, or lead frame substrate [5]. MCMs are chip packages that contain several dies mounted close together on a substrate. The short interconnects among the chips improve the performance and significantly reduce the noise that is picked up by tracks connecting individual chip packages. MCMs are classified by substrate: MCM-C (with ceramic), MCM-D (deposited), MCM-S (with Si) and MCM-L (with laminated circuit board). Three-dimensional packaging technology includes stacked dies, stacked packages, and other solutions where the components are mounted in several layers above each other. SIP provides more integration flexibility, faster time to market, and lower product research and development cost than SOC [6].

Similar to SIP concept, SOP offers the system solution in a package. However, SOP has a much broader concept than SIP. While in SIP, interconnect lines are used to connect the active and passive chips together, in SOP, dissimilar chips are connected through a network of interconnects and embedded passive components. The SOP package substrate is a functional unit with optimized electrical, mechanical, and thermal properties [7]–[16]. Fig. 1 demonstrates the SOP concept for a wireless

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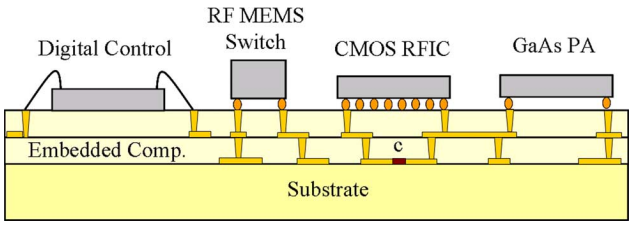

Fig. 1. SOP concept for a wireless system.

system comprising digital control and IF signal processing circuitry, RF MEMS switches, advanced CMOS or SiGe RFICs, GaAs power amplifiers, and embedded RF passive components.

In the IC packaging concepts discussed above, it is necessary to interconnect chips to their associated package. The main chip-to-package interconnect techniques available today are wire bond, flip chip and tape automated bonding (TAB). In wire bonding, a fine metal (typically Au or Al) is bonded between each of the I/O pads on the chip and its associated pin on the package, one at a time, using solid-phase welding. The process involves applying pressure and ultrasonic energy (ultrasonic wire bonding) and in some cases, additional heat (thermosonic wire bonding). The main advantages of wire bonding are high yield, high reliability, high interconnect density (pad size of 30 to 35 μm), and high flexibility of interconnect between the chip and package. The disadvantages of the wire bonding are high dynamic power dissipation, electromagnetic interference (EMI), high I/O inductance, and additional signal delay due to long chip-to-package interconnects.

In flip-chip technology, the integrated circuit chip is attached to a carrier substrate with its active surface facing toward the substrate. Interconnection between I/O pads on the chip and pads on the substrate is achieved using solder bumps. Flip-chip interconnects provide the shortest possible chip-to-package interconnection distance compared to other standard chip-to-package interconnect technologies such as wire bonding or TAB. However, the package system performance is not much improved, as it is highly dependant on the interconnection layout design and the various materials used for underfill, substrate metallization, substrate solder mask, and chip passivation. Additionally, there are other disadvantages with flip-chip including solder migration, difficulty in removing heat, die inspection using X-ray, and stress-related reliability issues such as die cracking, underfill cracking, solder fatigue cracking, and fillet cracking [2], [17].

TAB is a high-density interconnection technology based on bonding a die to a flexible polymer tape containing copper leads. The die is bonded to the metal lead through bumps using thermocompression bonding. The interconnection is formed by either solid state interdiffusion of Au plated leads and Au bumps or by diffusion in eutectic Sn-plated leads and Au bumps. One of the advantages of this bonding technology is the ability to test prior to assembly using probe pads patterned on the tape. Other advantages include small weight and ability to handle high I/O counts. The main disadvantages of TAB are long parallel interconnection with high interwire capacitance and large series inductance, difficulties with system testability, and coplanarity of the beam leads with the chip and substrate [18].

Herein, a new integration technology based on the SOP concept is presented, where the packaging material is a planar substrate such as Si wafer. Embedded passives and interconnecting lines between chip and package are implemented by using standard microfabrication techniques including photolithography, etching, and lift-off. Therefore, there is no need for wire-bond, flip-chip, or TAB. In the following section, this technology and its advantages and disadvantages are discussed. Section III presents the design and characterization of interconnect electrical performance at high frequencies. In Section IV a simple implementation and characterization of the developed integration technology for a 10-GHz CMOS receiver is presented. A summary and conclusion based on the developed technology is presented in Section V.

II. Self-Aligned Wafer-Level Integration Technology (SAWLIT)

The wireless communication market continues to expand and has become larger than the personal computer industry. Demand for low-cost technology with higher levels of integration has lead to innovations in many application areas including integration and packaging. Packaging of RF microsystems is essential to realizing a wireless communication module. RF packages include disparate components including power amplifiers, transmit/receive/control modules, lumped and distributed filters, couplers, RF switches, impedance matching, and antennas. Some of these components, such as high-Q RF inductors, capacitors, filters, and antennas are best fabricated on the package rather than the active chip which is typically a low resistivity silicon substrate. In standard silicon technologies, the Q factor of integrated spiral inductors is limited to 5–30 due to the inherent losses of silicon substrate. Using low-loss dielectric materials or unconventional 3-D fabrications, the quality factor can be enhanced to values higher than 100 [19], [20]. While the Q of these passive components can be improved, their size still remains large compared to active devices. Integrated lumped spiral inductors as well as I/O pads on a typical RF integrated circuit occupy more than 60% of the chip area resulting in additional chip cost [21], [22]. Antennas are another example that cannot be integrated on silicon due to their large size and limited bandwidth on Si substrate [7], [23].

A technology to tightly integrate heterogeneous chips and passive components has been introduced by General Electric [24], [25]. GE high-density interconnect (HDI) technology originally was developed for digital applications. In this technology, a thick common carrier substrate is partially etched with cavities to embed disparate active chips and passive components. The chips are placed inside the etched cavities using a die-attach material. A 25-μm-thick polyimide such as Kapton film is laminated over the top of the substrate in order to form the first dielectric and passivation layer. Via holes are made directly on the chip pads using laser drilling. The interconnection metallization and via contacts are formed using sputtering and electroplating processes. Fig. 2 shows the GE HDI technology concept.

Wafer-scale integration has also been discussed in a number of other papers [26]–[31]. These technologies have, however, suffered from low yield [3], [18], [32], [33]. The SAWLIT with

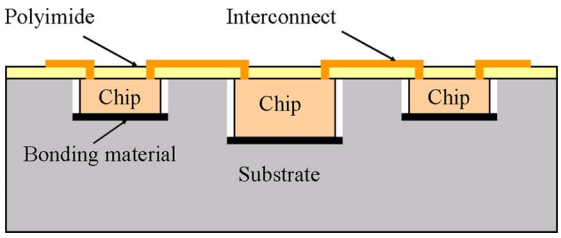

Fig. 2. GE HDI concept.

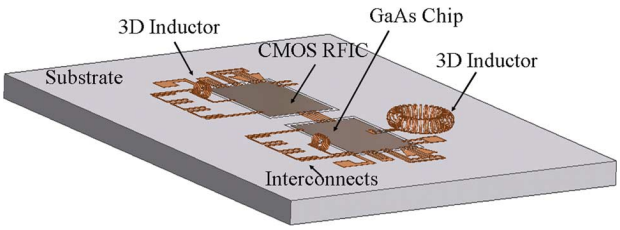

Fig. 3. SAWLIT concept for a wireless transceiver system.

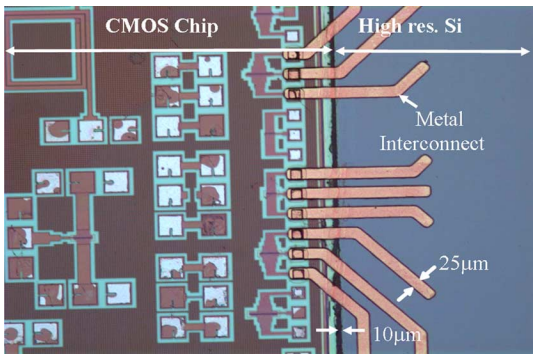

Fig. 4. CMOS chip integrated inside a high-resistivity Si. Interconnects as narrow as 25 μm are used.

embedded passives introduced here is based on the SOP approach [34], [35]. In SAWLIT, as shown in Fig. 3, various heterogeneous chips are placed in a carrier substrate with a seamless transition between each chip and the substrate. By utilizing photolithographic-defined chip-to-package interconnects, very high density interconnect metallization can be achieved.

SAWLIT allows for integration of chips fabricated using different technologies on one substrate. In this heterogeneous integration scheme, instead of using wire bonds or flip-chip bumps to make chip to package connection, lithographically defined interconnects with very narrow ($\sim$25 μm) footprints as shown in Fig. 4 are utilized.

I/O pads on the chip with current dimensions of 25 μm $\times$ 25 μm occupy slightly smaller area than the pads for flip-chip or wire bond (state-of the-art 35 μm $\times$ 35 μm). By further optimization of SAWLIT, compared to current standard technologies, not only higher interconnect density can be achieved, but also the size of the active chip is reduced as the area allocated to I/O pads shrinks.

Bulky passive components such as inductors and capacitors used in RF and mixed-signal circuits can be removed from the active chips and placed on the carrier substrate. Since the chip-to-package interconnect width is only 25 μm, there is no additional penalty in terms of excess dc power dissipation or extra loss associated with the off-chip passive components. In fact, by using a low-loss carrier substrate such as high-resistivity Si or quartz, the quality factor of the inductors or transmission lines can be improved, resulting in better performance of RF modules. At the same time, since the bulky inductors and capacitors are relocated from the active chip to the carrier substrate, the size of active RF or mixed-signal chips are significantly reduced.

The dynamic power consumption of digital, RF, and mixed-signal systems is directly proportional to the total I/O and wiring capacitance. In digital and mixed-signal systems, typically line drivers and buffers are used to drive long and wide capacitive interconnects at high data rates from one chip to another. These line drivers not only occupy a large chip area but are also power hungry. In RF systems, matching to 50 Ω is often used to drive I/O and off-chip components. This results in significant increase of the power consumption of RF circuits. In SAWLIT, high-density narrow interconnects can significantly reduce I/O pad and interconnect wire capacitances. Once the I/O and interconnect capacitances are reduced, there will be no need for large-area and power-hungry buffers in digital and mixed-signal systems. High-impedance connections instead of 50-Ω connections can be used in RF systems. Therefore, the total dc power consumption in systems integrated using SAWLIT is significantly lowered, at no additional penalty. Interconnects in SAWLIT are also characterized by small series inductance and reduced EMI when compared to standard interconnect techniques, and provides an excellent packaging solution for RF, microwave, and even millimeter-wave circuits.

Since the passive components are embedded on the carrier substrate, same active chip can be used with different passive components to achieve different system functions. It is also possible to modify the embedded passives in order to improve the system performance. These unique capabilities allow the system designer to modify the system without changing the expensive active chip, thus decreasing the time to market and saving cost on system development and revisions. It is also noted that the system integration can be done in a batch fabrication manner, as many of the same systems can be integrated and interconnected at the same time. This will further reduce the system cost. The other advantage of SAWLIT is the possibility of visual inspection of chip-to-package contacts in determining the yield of the integration process (see Fig. 6), which is not possible using flip-chip technology [2].

Like most SIP and SOP approaches, SAWLIT suffers from the problem of unidentified known good die. As the size of the chips and pad areas are reduced, screening for good ICs using on-wafer probing becomes more challenging. Therefore, the yield of the integration process is eventually determined by the yield of individual chips rather than by the integration process itself. In order to improve the yield of the system integration, one should characterize individual chips prior to the assembly. For such preintegration tests, new automatic on-wafer probing techniques need to be developed.

The following describes the step by step SAWLIT integration process. While the carrier substrate in SAWLIT can be any machinable and planar substrate, high-resistivity silicon wafer is chosen as the carrier substrate for its mechanical and thermal

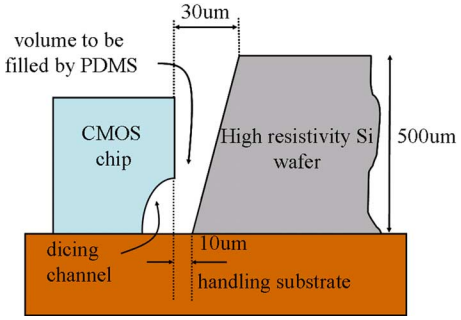

Fig. 5. Etch profile and dimensions of the hole etched inside the carrier substrate. DRIE process is optimized to achieve a 2° angle for the trenches, which results in a 20-μm lateral etch for a 500-μm-thick silicon wafer (30-μm gap on the top instead of 10 μm).

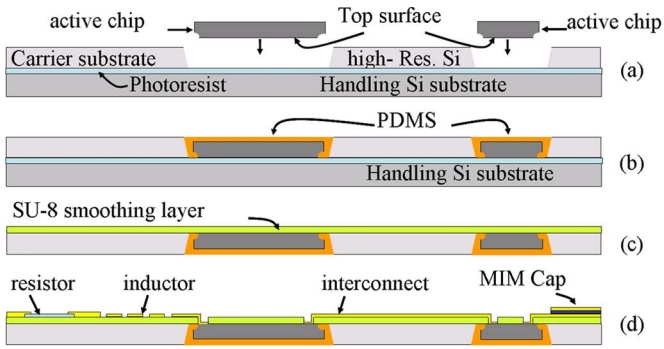

Fig. 6. Step-by-step SAWLIT fabrication process. (a) Carrier substrate and disparate chips are placed on the handle substrate upside down. (b) PDMS is applied and polymerized to fill the gaps. (c) Handle substrate is detached and Su-8 is deposited on the top surface for planarization. (d) Standard microfabrication process is used to add high-density chip-to-package interconnects and embedded passives.

match to Si chips as well as its low-loss characteristics for high-frequency applications. First, using a deep reactive ion etcher (DRIE), holes are etched all the way inside the high resistivity Si wafer. The dimensions of the holes and their etch profile are important design parameters to obtain optimum chip-to-package integration. Fig. 5 shows the desired interface between the chip and the carrier substrate. The size of the holes etched inside the carrier wafer is about 10 μm larger on each side of the diced disparate chips. This extra gap is necessary in order to allow poly di-methyl-silicone (PDMS) used in the following step to fill the cavity that is made by dicing saw during chip dicing process. The etch profile of the carrier substrate allows easy loading of PDMS inside the gap, without generating any air pocket. The 10-μm gap will result in a few micrometer misalignments between the chips. A minimum trace width of 25 μm and a separation of 25 μm between the interconnect lines assures that the small misalignment will not cause a short circuit or an open circuit in this self-aligned process. The etched high-resistivity Si wafer is then attached to a handling substrate, typically a Si wafer coated with photoresist. Next, active chips are placed upside down inside the DRIE holes as shown in Fig. 6(a). PDMS is dispensed and polymerized at room temperature to fill the $\sim$ 10-μm gaps between the chips and carrier substrate as illustrated in Fig. 6(b).

PDMS is chosen because of its low dielectric constant, low loss, and low viscosity. However, PDMS is only rated up to a temperature of 200 °C. Additionally, PDMS, like many other polymers, is not a good thermal conductor. Therefore, for applications where heat exchange is important or operating temperature is expected to be in excess of 200 °C, PDMS should not be used. Such applications include high-power amplifiers or microprocessors, where device junction temperature may be in excess of 150 °C and heat removal is critical. For such applications, gap filler thermal interface materials such as TP-2100 and TP-2101 with high thermal conductivity should be utilized [36]. After PDMS (or thermal interface materials) polymerization, the carrier substrate and the chips are detached from the sticky surface. This is accomplished by simply exposing the wafers to acetone in order to strip the photoresist and detach the carrier substrate and the chip from the handle substrate. 6 μm of SU-8 (a photo-curable polymer) is then spun for planarization, resulting in a seamless transition between the high-resistivity Si substrate and the chips as shown in Fig. 6(c). Finally, standard microfabrication steps including photolithography, etching, and lift-off are used to add chip-to-package interconnect lines and embedded passive components such as transmission lines, inductors, capacitors, and resistors [see Fig. 6(d)].

The chip placement in the SAWLIT process is done in a self-aligned manner. The etch profile of the carrier wafer and tight gap that exists between the chip and carrier wafer forces the chip to sit at the desired location with the possibility of only a few micrometers of misalignment. The misalignment sets a minimum interconnect width (25 μm) and metal to metal gap (25 μm) to obtain 100% yield. Most chip manufacturers use a dicing saw to dice their chips. The process results in chip dimensions that may vary by 25 μm from batch to batch. However, within one fabrication batch, the chip dimensions are rather accurate (within 5 μm). Because of the current dicing accuracy within different batches, chip self-alignment can only be achieved if the chips from the same batch are used or if the tolerances in SAWLIT on the pitch size and pad size are increased beyond 50 μm. On the other hand, to achieve higher interconnect density in SAWLIT, more accurate dicing machines are needed. Alternatively, it is possible to use DRIE or laser ablation instead of a dicing saw to dice the active chips that are to be integrated in the substrate. For dicing using DRIE, adjusting the etch rate and etch profile results in accurate chip dimensions [37], [38], and thus micrometer accuracy in the chip placement process can be achieved. This technique is more costly, but is expected to allow very high interconnect density and can help SAWLIT to achieve contact pitch size and interconnect spacing as small as 5 μm.

III. Design and Characterization of High-Density Interconnects

To characterize the signal loss due to transition over PDMS as well as vias through the planarization layer, various transmission lines on a Si chip embedded inside a high-resistivity silicon substrate are designed and fabricated. For comparison, the same lines on the same high-ρ silicon substrate are also fabricated. The coplanar waveguide (CPW) structures over the transition area are designed using Ansoft HFSS electromagnetic simulator. The optimum signal path width of W =78 μm and

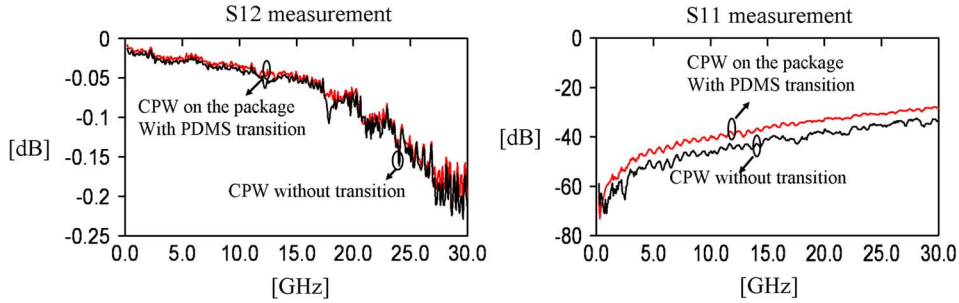

Fig. 7. Transmission coefficient (S_{12}) (left) and reflection coefficient (S_{11}) measurements (right).

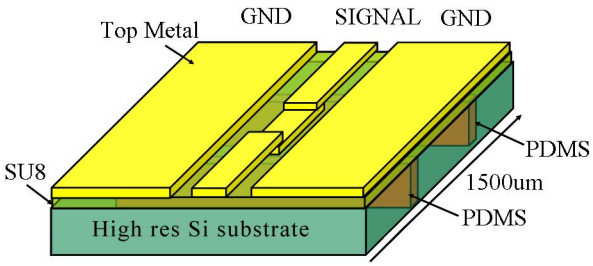

Fig. 8. CPW structures over the transition area with vias.

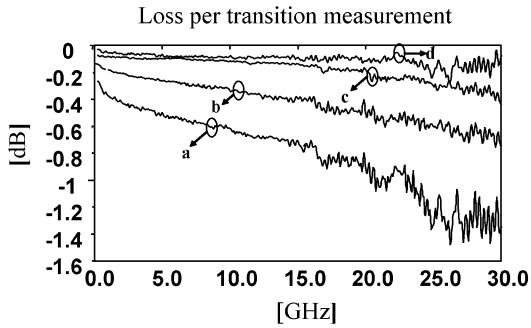

Fig. 9. Loss measurement for a CPW line over PDMS. (a) loss due to the line running over the PDMS. (b) and (c) illustrate the loss due to top and bottom metal layers, respectively. (d) Loss of the via and the transition area over the PDMS.

signal-to-ground gap of G =25 μm for low-loss 50-Ω CPW lines are utilized.

The S-parameters of the 1500-μm CPW lines are measured using an 8510XF network analyzer. Fig. 7 shows the measured transmission and reflection coefficients of the CPW line on the package structure (with a pair of PDMS voids) as well as CPW line on the high-resistivity Si. There is practically no difference between the insertion losses of these two structures up to 30 GHz. Moreover, the difference in reflection coefficients (S_{11}) of the CPW on the package with PDMS voids and CPW without transition is insignificant. The reason for the slight difference is the difference between dielectric constant of PDMS and silicon substrate. The results indicate that the transition gap between the carrier substrate and Si chip filled with PDMS has no significant loss or mismatch effect.

In order to characterize the via transitions across the SU8 planarization layer, CPW lines with vias connecting the top interconnect metal to the bottom metal on the chip surface are designed and fabricated as schematically shown in Fig. 8. Additional calibrating test structures to remove the effect of loss due to top and bottom metals are also fabricated and tested. The loss of each structure is calculated from measured S-parameters using the following equation:

$$\begin{aligned} \text{Loss} &= 1 - |S_{11}|^2 - |S_{21}|^2 \\ \text{Loss(dB)} &= 10.\text{Log}(1 - \text{Loss}). \end{aligned} \tag{1}$$

Fig. 9 shows the measured loss components for CPW structures measured in this experiment. Curve (a) in Fig. 9 is due to the line running over the PDMS, while curves (b) and (c) illustrate the loss due to top and bottom metal layers, respectively.

Curve (d) in Fig. 9 shows the loss of the via and the transition area over the PDMS. As the figure indicates, the loss per transition in this technology is less than 0.1 dB up to 30 GHz.

IV. Implementing a 10-GHz CMOS Receiver in SAWLIT

Using SAWLIT, a CMOS 10-GHz receiver front-end chip is designed and integrated with embedded passives on a high-resistivity Silicon carrier substrate. Although the RF receiver chip was initially designed to operate stand-alone, the integration concept is used to show how embedded passives that are added at a later stage can improve the overall performance. Effective use of SAWLIT can move most of the passive components from the receiver chip to the carrier substrate. Only small inductors or capacitors that need to be very close to the active device (such as a 370-pH inductor in an LC tank of a 10-GHz oscillator used here) remain on the chip. The receiver circuit with a schematic shown in Fig. 10 is implemented in 0.18-μm technology (IBM 7RF). The circuit consists of a cascode low-noise amplifier (LNA) with inductive degeneration, a single balanced mixer with an IF buffer, and a complementary cross-coupled *LC* voltage-controlled oscillator (VCO). Cadence simulation of the optimized LNA/mixer combination shows a conversion gain of 24 dB at the RF frequency of 10 GHz and IF frequency of 50 MHz. The 10-GHz LC VCO reported elsewhere [21] achieves a low phase noise of -125 dBc/Hz at 1-MHz offset from the center frequency. The receiver circuit area is only 1.2×1.25 mm^2. The chip that contains the receiver also holds other circuits and test structure with an overall chip size of 2.5×3.5 mm^2.

The RF receiver is first characterized using on-chip probing. The reflection coefficient of the input to the LNA (S_{11}) is measured with an Agilent 8722 network analyzer, and is -9.6 dB at 10.3 GHz. An Agilent E4448A spectrum analyzer is used to measure the gain and the 1-dB compression point of the front-

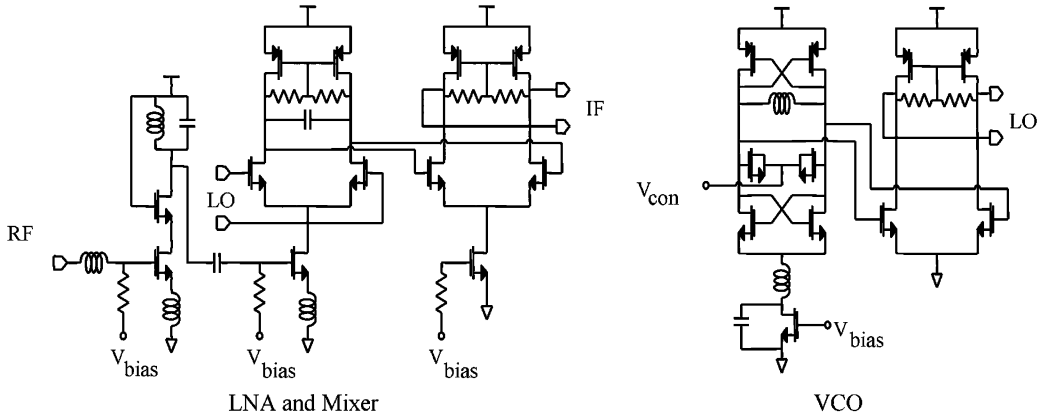

Fig. 10. Schematic of 10-GHz receiver front-end implemented in 0.18-μm CMOS (IBM 7RF) technology.

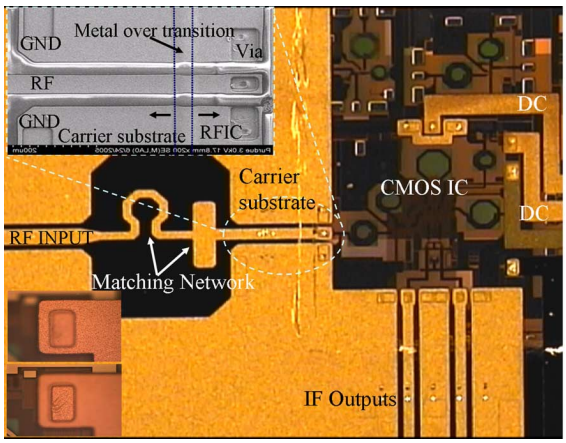

Fig. 11. Integration of a 10-GHz CMOS receiver using SAWLIT. SEM shows the transition area, and the picture on the bottom left illustrates one of the via pads after gold electroplating.

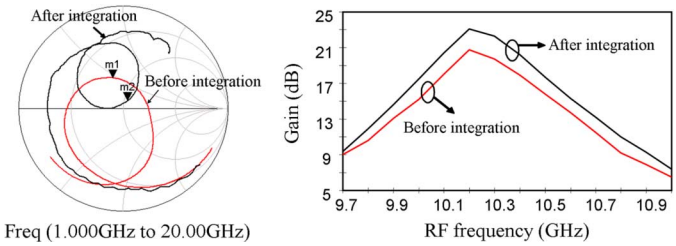

Fig. 12. Input matching (left) and conversion gain (right) of the receiver front-end before and after integration.

end. For the LO frequency of 10.25 GHz, the conversion gain is 21 dB, and the 3-dB bandwidth is about 300 MHz. The noise figure of the receiver is also measured based on output noise power measurement technique [39]. A double sideband noise figure of 8.2 dB at an RF frequency of 10.4 GHz and an IF frequency of 150 MHz is measured.

In order to improve the input matching and overall conversion gain of the receiver front-end, a combination of a series inductor and a shunt capacitor is added to the input of the LNA. Fig. 11 shows the proposed schematic design and fabricated system. An aluminum layer fabricated below the SU-8 works as the bottom plate of metal–insulator–metal capacitor, while the top plate of the capacitor is implemented using the interconnect metal. Also shown in the figure is an scanning electron micrograph (SEM) of the transition area over the PDMS gap. The metal coverage over the PDMS is very smooth due to the SU-8 planarizing layer used in this technology. Via pads of the CMOS chip electroplated with gold are also shown in the figure. Excellent step coverage from top to bottom of the vias was achieved in SAWLIT as illustrated in Fig. 11.

Fig. 12 shows the input matching of the receiver measured by one-port S-parameter measurement and conversion gain of the receiver front-end measured using a spectrum analyzer before and after integration. By adding the embedded passives, namely a series inductor (0.6 nH) and a shunt capacitor (0.28 pF), the input matching at 10.3 GHz improves from -9.6 to -26 dB. The conversion gain at 10.3-GHz input RF frequency improves from 21 to 23 dB. The improvement in the conversion gain is rather small mainly because the return loss before adding LC matching network is low (-9.6 dB) meaning a small portion of the RF signal is reflected. Nevertheless, the technology can prove to be very useful if the initial design of the RFIC is not satisfactory, or if the input, output, and interstage matching networks are embedded on the carrier substrate.

V. Conclusion

A new self-aligned wafer-level integration technology (SAWLIT) concept is presented. SAWLIT promises a cost-effective and batch-fabricated heterogeneous integration technology with high interconnect density, small die size, reduced dynamic power consumption, embedded and improved passive components, and overall better performance. By placing the passive components on the carrier substrate, SAWLIT allows the designer to modify the passive components of the design without changing the active chips. The development cost and time to market are also reduced. The technology allows for an easy inspection of the chip-to-package contacts. Furthermore, accurate chip dicing techniques (or dicing using DRIE) are needed to take advantage of self-aligned chip placement in SAWLIT. Similar to SIP and SOP integration, the drawback of SAWLIT is the problem of not knowing the good die. Unless on-chip probing techniques to identify the good dies are utilized, SAWLIT application will be limited to simple systems integrated with high-yield components. Nevertheless, SAWLIT has the potential to improve the performance and

reduce the cost of future digital, RF, and mixed-signal systems. A technological validation of SAWLIT is needed to prove the concept introduced in this paper. In this paper, a 10-GHz CMOS receiver is integrated with embedded passives on a high-resistivity Si substrate. The embedded passives were used to improve the performance of the receiver. The input matching is improved from -9.6 to -26 dB, while the convergence gain of the receiver improved from 21 to 23 dB.

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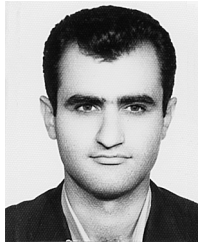

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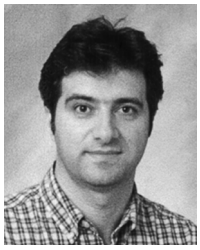

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