Multiwafer Vertical Interconnects for Three-Dimensional Integrated Circuits

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***Abstract*—Low-loss multiwafer vertical interconnects appropriate for a microstrip-based circuit architecture are proposed. These transitions have been designed, fabricated, and measured for 100-μm-thick silicon and GaAs substrates separately. Experimental results show excellent performance up to 20 GHz, with extremely low insertion loss (better than 0.12 and 0.38 dB for the two different silicon designs and 0.2 dB for the GaAs transition), and very good return loss (reflection of better than 12.9 and 17.3 dB for the two silicon designs, respectively, and 13.6 dB for the GaAs design). Using a high-performance transition allows for a more power-efficient interconnect, while it enables denser packaging by stacking the substrates on top of each other, as today's technologies demand.**

***Index Terms*—Integrated circuit packaging, microstrip line, vertical interconnects.**

I. Introduction

IN TODAY'S technology, integrating a system is a major challenge in terms of having the most compact and efficient packaging. Microstrip lines are one of the best suited architectures for monolithic microwave integrated circuits (MMICs) and, hence, are widely used due to their large bandwidth, high power handling, excellent miniaturization, and small volume. At the same time, the microstrip architecture has been the most difficult one to utilize in multiwafer arrangements due to the extending ground planes and the parasitic inductances and capacitances associated with changes in the ground metallization.

High-density circuit architectures require multiwafer transitions that can be used to tightly integrate circuit components on multiple wafers, integrated using wafer-to-wafer bonding methods. Developing a multiwafer circuit using a low-loss vertical interconnect architecture results in less dissipated power per unit area and, hence, increases power-handling capability and reduces volume and cost. To design an optimal transition, not only the line impedances should be matched (to maximize the coupling and minimize the reflection), but also the fields on the two interconnecting lines should make a transition in a way that reduces unwanted junction parasitics. Even at frequencies as low as L-band, matching the impedances alone is not adequate and the fields along the transition have to maintain their continuity as well. In a high-density circuit, good performance requires low loss combined with reduced parasitic radiation and proximity coupling between the various sections of the electromagnetic structure.

Previous research has demonstrated the development of efficient vertical transitions that transfer the wave (signal) from the backside of a wafer to the front side of the same wafer [1]–[3]. In addition, uniplanar transitions have been demonstrated that transition of the RF signal from one type of an interconnect to another [4]. Some examples of previous research include a coplanar waveguide (CPW)-to-microstrip transition on a single wafer [1], a CPW-to-CPW transition on a single wafer [2], a microstrip-to-coplanar stripline (CPS) transition, a slotline transition [3], and a CPS-to-CPW transition [4]. In all previous research, multiwafer transitions have thus far been designed and demonstrated in a finite-ground CPW circuit environment. Specifically, a CPW-to-CPW vertical transition was demonstrated on a silicon wafer, which transfers the signal from the front side of the bottom wafer to the backside of the top wafer, operated at frequencies as high as W-band [5]. As oppose to a CPW line, in a microstrip configuration, the ground and signal lines are separated by the thickness of the wafer. Hence, in order to make the transition of the microstrip line vertically from a lower wafer to the top wafer in a stacked configuration, both the signal and ground metallization have to go through vertically and, thus, multiple vias are needed.

The study presented in this paper describes for the first time the development and successful demonstration of a new three-dimensional (3-D) microstrip-to-microstrip interconnect that can transfer RF signals vertically through stacks of wafers. These transitions have been successfully demonstrated with two 100-μm GaAs wafers using deep reactive ion etching (DRIE) to form cylindrical vias [6] and are extended herein to multiwafer structures using two 100-μm Si wafers and wet etching to form conical vias. Fig. 1 illustrates the primary idea of the proposed transitions. In the 3-D view, the wire-framed boxes represent the substrates, while in the side view, the substrates are recognized as solid boxes. Also for the clarity of this figure, only the metal layers are depicted in the top view.

II. Design and Modeling

In order to implement the idea of the vertical interconnect, both signal and ground conductors have to make a transition

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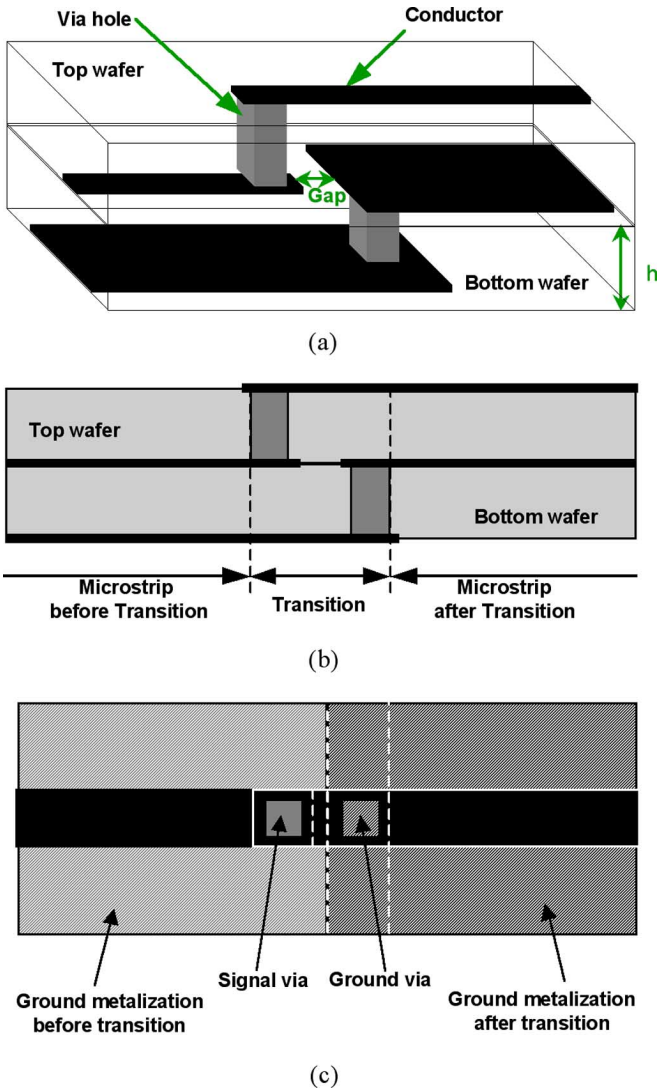

Fig. 1. Preliminary idea of vertical interconnects between two wafers (a) 3-D view. (b) Side view. (c) Top view. (Color version available online at: http://www.ieeexplore.ieee.org.)

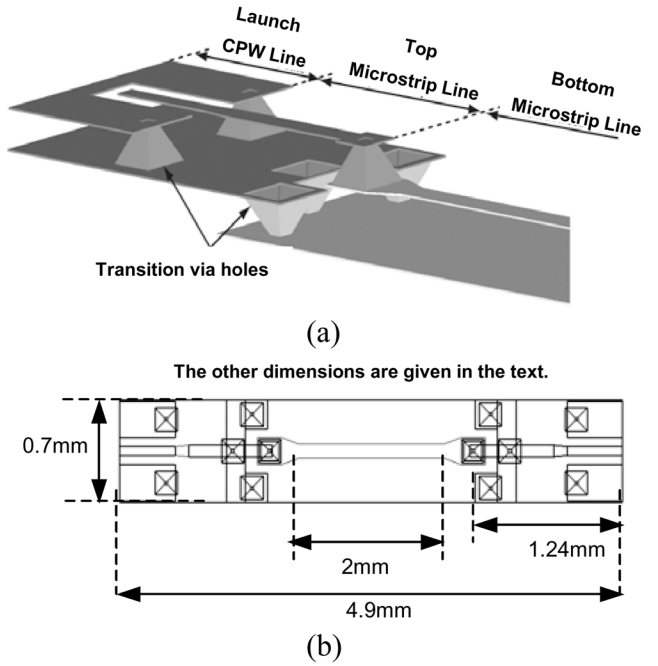

Fig. 2. First architecture (DES1): the optimized microstrip-to-microstrip vertical interconnects on silicon. (a) 3-D view. (b) Top view.

from the bottom wafer to the top wafer. The signal conductor of both wafers is on the front side of each wafer, as depicted in Fig. 1. As shown in this figure, in addition to the signal lines, the ground lines are finite in size and their width has been designed to provide the appropriate characteristic impedance (50 Ω). Both signal and ground lines are transited from a bottom wafer to the top wafer with vias that are etched through the wafers. The presence of vias increases the inductance of the line locally, which has to be compensated by introducing the proper capacitance at the transition point, for the desired frequency range. The design aspect for both silicon and GaAs wafers are identical, but due to the slight difference in fabrication processes, which will be described below, the parasitic elements introduced during transition are different in value. These parasitic capacitances and inductances are responsible for the continuity of the fields, near changes in geometry characteristics. Traditional methods to overcome these field discontinuities lead to either modifications of the geometrical structure in order to eliminate or minimize these parasitic values or to optimize their values so that they compensate the effect of each other (creating a resonance). Hence, different architectures are proposed herein for each case specifically to maintain both the impedance match and the continuity of the fields. Each structure has been modified and optimized using Ansoft HFSS V.9.1, for the best impedance and field match in the desired frequency range (1–20 GHz) on both silicon and GaAs 100-μm-thick wafers. The major difference between the designs originated from the available technology to fabricate the designs. Hence, the designs are reviewed separately herein.

A. Silicon Transition Designs

As mentioned before, the idea is to transition the signal vertically through vias. This transition will delay the signal and introduces some inductance along the transition path, which has to be compensated with proper capacitance accordingly. Two different designs have been established, namely, DES1 and DES2, which are shown in Figs. 2 and 3, respectively. Both designs are optimized for a stacked configuration of two 100-μm-thick high-resistivity ($\rho > 2$ k Ω·cm) silicon substrates. For low resistivity substrates such as the ones used in current CMOS processes, long microstrip lines will introduce substantial loss and should be avoided. However, with some modifications, vertical transition designs presented here can be utilized for 3-D integrated circuits.

As it is obvious from these figures, DES1 has a higher count of vias for the ground transition when compared to DES2. The vias have a pyramidal shape with 162 μm × 162 μm opening windows because they are etched anisotropically through the wafer using silicon wet etching. Hence, the base of each via is 20 μm × 20 μm in area. The width of the signal line on the top wafer is 80-μm wide, while on the lower wafer it is 100 μm so that all lines have a characteristic impedance of 50 Ω. During

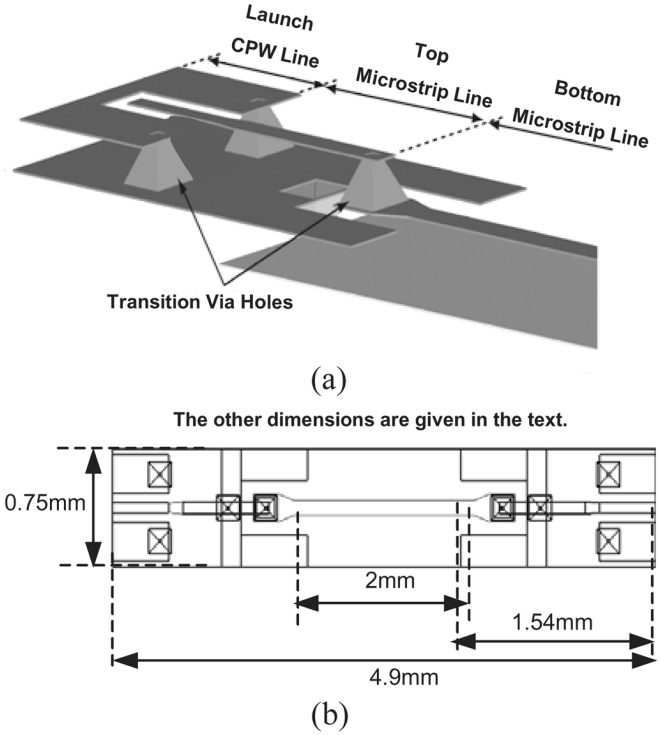

Fig. 3. Second architecture (DES2): the optimized microstrip-to-microstrip vertical interconnects on silicon. (a) 3-D view. (b) Top view.

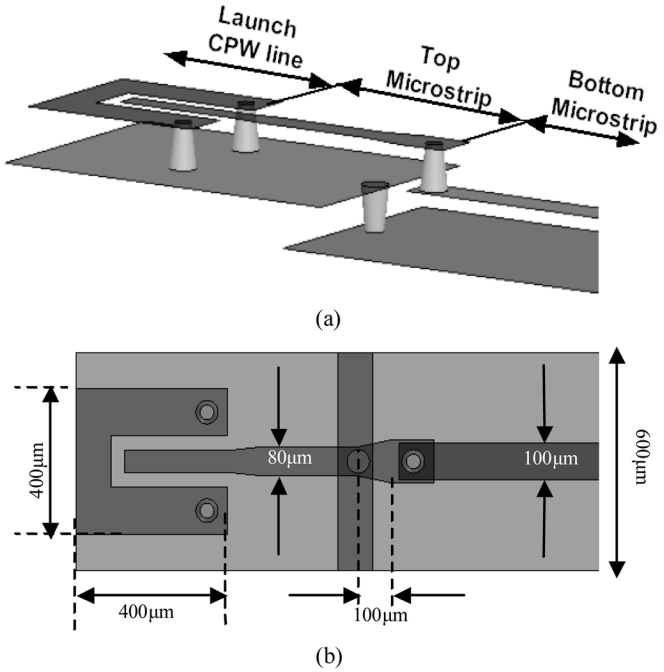

Fig. 4. Architecture of the optimized microstrip-to-microstrip vertical interconnects on GaAs. (a) 3-D view. (b) Top view.

the transition from the top wafer to the bottom wafer, the ground conductor of the top microstrip and the signal conductor of the bottom microstrip are sandwiched between the two wafers, thus causing a change in the characteristic impedance of the line. Specifically, the characteristic impedance increases from 50 Ω to a higher value. It is in an effort to correct for this change that the width of the signal line is widened from 80 μm on the top microstrip to 100-μm-wide line on the bottom microstrip.

In order to measure the s-parameters of the designed structure, a number of back-to-back transitions with different lengths of line in between them were fabricated. Moreover, to be able to make on-wafer measurements, a CPW section of line with a signal–gap–ground size of 60–40–250 μm (50 Ω) was utilized and appropriate CPW-to-microstrip transitions were designed and added at both ends.

In this design, with wet-etched vias, the ground vias open from the front side of the bottom wafer, while the signal via opens from the backside of the top wafer, allowing flexibility in defining the separation between the top and bottom wafer vias. This orientation of the vias aligns the inner sidewalls of the signal and ground vias of the transmission line in a parallel fashion and brings them in close proximity. Hence, the signal and ground currents are forced to flow along the parallel inner sidewalls of the vias, thus resulting in reduced parasitic radiation loss.

B. GaAs Transition Design

A new transition based on cylindrical via architecture has been designed on a 100-μm-thick GaAs wafers. The vias are fabricated by a DRIE so they are smaller in size and provide a more compact size design. In this design, the vias are cylindrical with a 60-μm diameter and with a pad size of 85 μm $\times$ 85 μm. As illustrated in Fig. 4(a), the signal is fed through a 60–40–130-μm CPW section to the top microstrip and transitions to the bottom microstrip through the vias. As in silicon designs, the width of the microstrip line was increased appropriately to compensate the increase in ε_{eff} (effective permittivity) when the conductor is sandwiched between two substrates. Fig. 4(b) shows the dimensions of the fabricated structure.

C. Modeling

As mentioned in the design section, the lines and transitions have been designed to maintain a 50-Ω impedance across the lines and through the vias. A 50-Ω microstrip or CPW line is realized relatively easily, but in order to preserve the impedance along the transition, the effect of the geometrical discontinuities is studied. A simple model has been derived that describes the response of such a transition fairly well [see Fig. 5(b)].

The inductance values are determined by the shape of the via and the via pad sizes, while the capacitance has two components: the parasitic open-end capacitance between the end of the microstrip signal conductor and the ground conductor [C_1, C_2 in Fig. 5(a)] and the gap capacitance between the signal and ground conductors at the midsection of the transition (C_{gap}), the value of which is primarily determined by the separating gap. As the gap size decreases, the value of the C_{gap} increases accordingly, while C_1 and C_2 values remain unchanged. On the other hand, increasing the thickness of the wafer decreases the value of C_1 and C_2. Comparing these effects and the geometry dimensions, the C_1 and C_2 values can be negligible with respect to C_{gap} for small gap sizes and thick wafers. As a result, we can further simplify the model to the one shown in Fig. 5(c), where $C = C_{\text{gap}}$. The extension of the lines beyond the vias

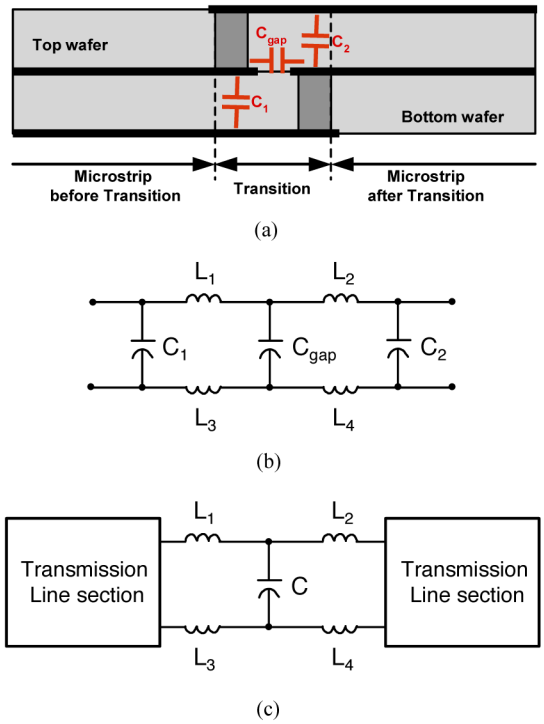

Fig. 5. Modeling the transition. (a) Side view of the transition showing the capacitor components. (b) Simplified model of the geometry shown in (a). (c) Further simplified model of the transition. (Color version available online at: http://www.ieeexplore.ieee.org.)

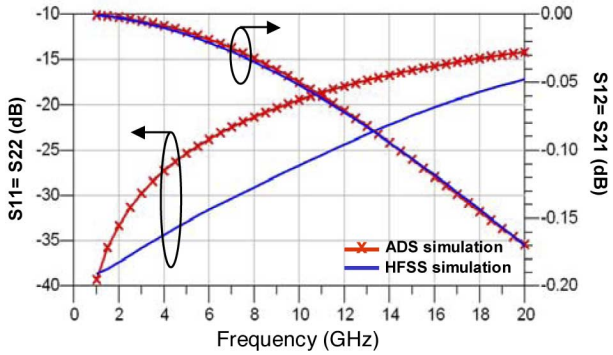

Fig. 6. Simulation results with HFSS for the selected example and the response of the optimized model, which was extracted from ADS. (Color version available online at: http://www.ieeexplore.ieee.org.)

are modeled as simple transmission lines, while the lumped circuit shown in this figure represents the transition section itself. The circuit parameters of this simplified model are derived within ADS 2003, while the physical structure is simulated and optimized using Ansoft HFSS V.9.1 to achieve the optimum impedance and desired field match in the operating frequency range (1–20 GHz). In order to derive the value of the passive components shown in Fig. 5(c) ($L_i, i = 1, 2, 3, 4$ and the capacitance C) as function of the given geometry, a detailed study is performed using both HFSS and ADS software. First by keeping the architecture and all the dimensions the same, the gap size [the distance between the metal traces, as shown in Fig. 1(a)] varies and, at each value, the structure is simulated within HFSS. Next, the wafer thickness [labeled as h in Fig. 1(a)] is varied and, for each value of the wafer thickness, the structure is simulated within HFSS. The simulated scattering parameters of each of the above-mentioned geometry parameters are exported from HFSS and then imported in ADS. By utilizing the gradient optimization, the value of circuit elements shown in Fig. 5(c) are derived so that the response of the circuit is best fitted to each corresponding set of data from HFSS.

To demonstrate the above-described design process, a 100-μm GaAs transition with gap size of 75 μm has been used as an example here. This design is modeled in ADS by using the gradient optimizer to match the s-parameter results derived from simulating the physical 3-D structure in HFSS. Fig. 6 shows the response of this design in HFSS along with the response of the best fit model deduced from ADS by adjusting the values of the elements of the proposed simple circuit. The lumped-element circuit will show a more narrow frequency-band response when compared to the fabricated transmission-line structure. The theoretically calculated results in ADS (the line marked with $\times$'s) follow the real insertion-loss response from the HFSS model, almost perfectly up to 20 GHz, while the reflection coefficients compare less favorably. The discrepancy in the values of the reflection coefficients originates from the fact that the model used is using the lumped-element circuit and has been simplified by consolidating the three capacitances into one. Despite the simplifications, the results from the analysis agree fairly well with the measured behavior of the transition to the third decimal place ($10^{-2} - 10^{-2.7} \approx 8 \times 10^{-3}$). This extraction of the inductance and capacitance values is performed for each geometrical variation in the vertical interconnect structure and the value of the capacitance and inductances are plotted in Fig. 7(a) and (b), respectively. As observed from the graph in Fig. 7(a), the gap size is changed for three different wafer thickness values $h = 50$ μm, 100 μm, and 200 μm. C_1 and C_2 being the open-end parasitic capacitances of the simplified transmission line, dominate when the wafer thickness is small compared to the gap size. Hence, the real value of the model parameter C might deviate slightly from the plotted curve, as the substrate gets thinner [this is the dotted plot in Fig. 7(a)]. However, as the gap size decreases, the value of the C_{gap} increases and becomes a dominant term, thus, any variation of the gap size has a significant effect on C. On the other hand, by keeping the gap size at the nominal value, i.e., 75 μm, and increasing the thickness of wafers, the inductance value increases accordingly. Hence, for a given thickness of the wafer, the value for L_i's can be derived from Fig. 7(b). The C value can also be extrapolated from the graphs in Fig. 7(a) and an estimated value for the gap size can be realized as the starting point of the design. Proper dimensions for the transition can be maintained by using 3-D electromagnetic software such as HFSS and by optimizing the performance for the desired frequency range. For a 100-μm-thick GaAs wafer and gap size of 75 μm, the inductance and capacitances values can be read off the graphs as $L_1 = L_2 = 0.166$ nH, $L_3 = L_4 = 0.124$ nH, and $C = 0.0445$ pF.

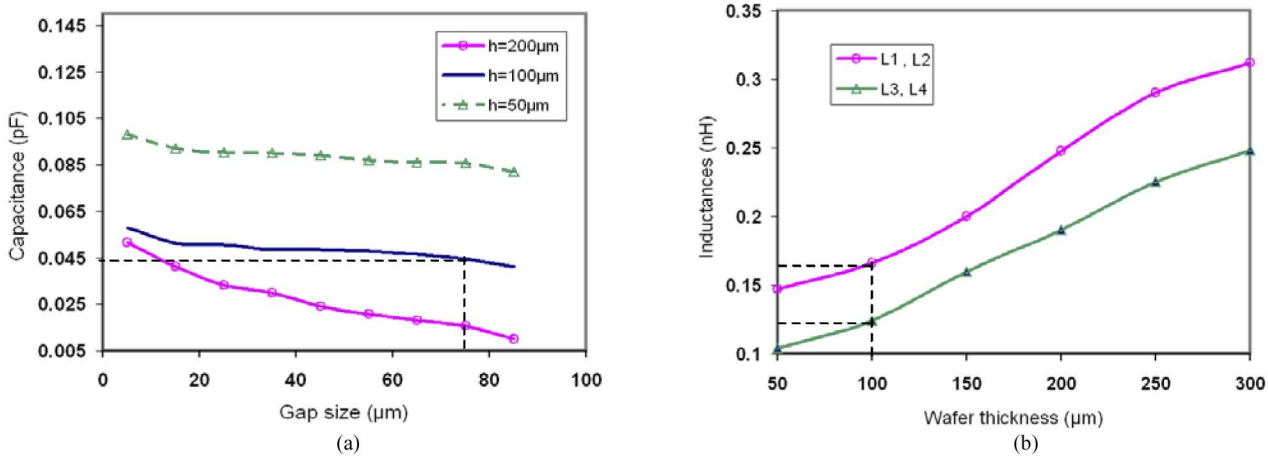

Fig. 7. Variation of the modeled parameter values showed in Fig. 5 with respect to physical changes to the geometry on GaAs. (a) Capacitance. (b) Inductances. (Color version available online at: http://www.ieeexplore.ieee.org.)

III. Fabrication

A. Silicon Design

The fabrication of the proposed silicon multiwafer transition is achieved via a combination of surface and bulk micromachining. Two 100-μm-thick high-resistivity double-sided polished silicon wafers with thermal oxide on both sides are used. 1 μm of gold is deposited on the topside using a liftoff process in order to form the top interconnect. The via structures are anisotropically etched in potassium hydroxide (KOH) and are metallized with 4 μm of gold to form the bottom metallization layer. The required alignment marks for the front and backside of each wafer are formed using optical alignment. After completion of the fabrication steps on each of the two wafers separately (top and bottom wafers), the two wafers were bonded together to form the stacked multiwafer structure. The bonding alignment marks are etched through the wafers (DRIE) so that the two wafers can be aligned through the etched holes at four corners of the wafer. Finally a gold-to-gold thermo-compression bonding is performed at 365 °C [8], [9], which completes the process.

B. GaAs Design

Fabrication of the multiwafer transition on GaAs utilizes industry standard processing and is compatible with active field-effect transistor (FET) fabrication and integration processes. With some minor differences, the process steps are similar to the silicon transition. Starting with full thickness GaAs wafers, one side of the wafers are fully processed and then flipped and mounted on carriers for backside processing. Backside processing includes thinning the GaAs wafer to 100 μm, dry etching the 60-μm-diameter vias, metallization, patterning, and scribing.

As in the silicon architecture, each of the top and bottom wafers is processed separately. After completion of the fabrication steps on each of the two wafers, the top and bottom transition substrates are bonded together by a thermo-compression gold to-gold bond to form the stacked multiwafer structure, similar to the silicon devices. Alignment is achieved by simply aligning the edges of the two wafer pieces.

IV. Measurement and Simulation Results

A. Silicon Design

The fabricated structures have been measured using the 8722 network analyzer with a thru-reflect-line (TRL) calibration for 1–20 GHz. These calibration standards are fabricated on each chip and, in addition to providing calibration of the network analyzer, they serve to provide good measurements of the insertion loss in decibels per millimeter. On the silicon wafers, insertion loss of approximately 0.19 dB/mm has been measured. Fig. 8(a) demonstrates the measured and simulated results of the DES1 shown in Fig. 2, while Fig. 8(b) depicts the results of the DES2 (Fig. 3). As seen from these data, the measured and simulated reflections coefficients agree very well.

For DES1, a reflection of better than -12.9 dB and for DES2 better than -17.3 dB has been achieved for the whole frequency band. The measured insertion loss is slightly higher than the simulated insertion loss due to the fact that the simulations have been done for perfect conductors and the ohmic losses were not included. Assigning a finite conductivity to the lines and considering the ohmic losses in the simulations will not have any substantial effect on the reflection coefficient, but it will increase the insertion loss as the measurements have demonstrated. Comparing the return loss of the two designs $(1 - |S_{11}|^2 - |S_{21}|^2)$, it is seen that DES1 has a better loss at lower frequencies, but it degrades faster as frequency increases. This is due to the fact that the ground metallization of DES1 has multiple vias and, hence, is a more inductive structure with respect to DES2. This plays the dominant role in increasing the return loss at higher frequencies.

Nondeembedded insertion loss of better than 0.87 dB for DES1 and 1.47 dB for DES2 has been achieved. The measured insertion loss of each one of these structures includes the two back-to-back vertical transitions, along with a 2-mm-long microstrip line connecting the transitions. In addition, there are two 600-μm-long sections of microstrip line right after the CPW-to-microstrip transitions.

To get a more accurate characterization of the transition, we deembedded the loss of the microstrip-line sections included in

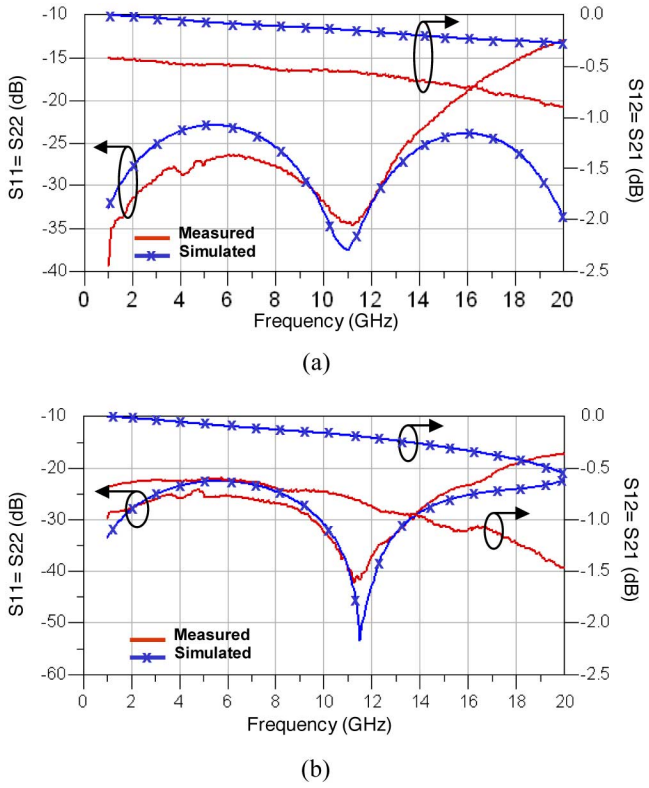

Fig. 8. Measured and simulated response of the whole structure consisting of two back-to-back microstrip-to-microstrip vertical interconnect and CPW-to-microstrip transitions at both ends on silicon. (a) DES1. (b) DES2. (Color version available online at: http://www.ieeexplore.ieee.org.)

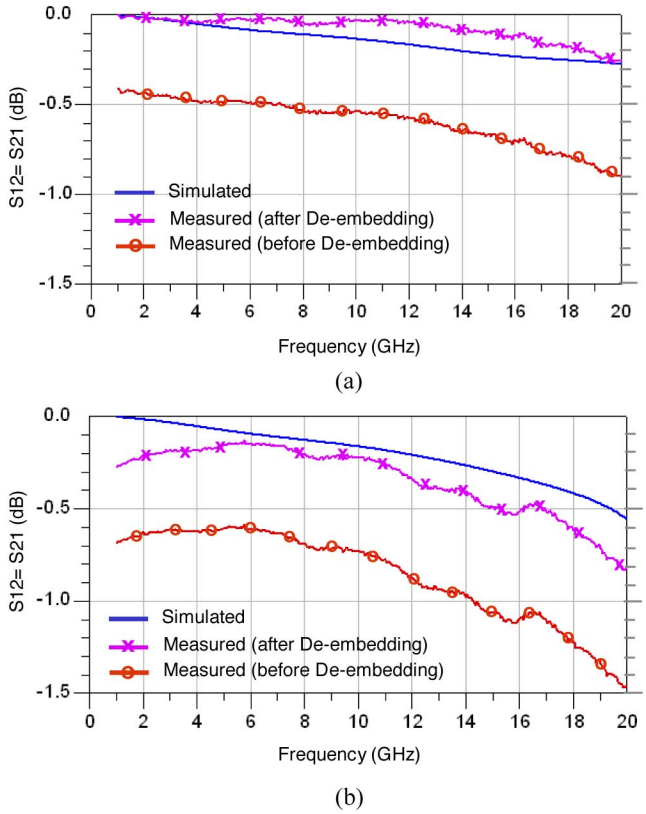

Fig. 9. Simulated and measured response of a back-to-back vertical interconnects on silicon before and after deembedding the ohmic loss due to the excess microstrip sections. (a) DES1. (b) DES2. (Color version available online at: http://www.ieeexplore.ieee.org.)

the designs (a total of approximately 3.2-mm-long microstrip lines). Fig. 9(a) and (b) shows the measured, deembedded, and simulated results for the insertion loss of each back-to-back transition separately. Based on these results, insertion loss of back-to-back transitions better than 0.24 dB for DES1 and 0.77 dB for DES2 has been achieved after deembedding. As a result, the insertion loss per individual vertical transition is 0.12 and 0.38 dB, respectively.

B. GaAs Design

The designed transitions for the GaAs wafer have also been fabricated and measured using the 8722 network analyzer calibrated from 1 to 20 GHz. As mentioned in the design section, the two-port CPW measurement is possible by fabricating a back-to-back microstrip transition with additional microstrip-to-CPW transition at both ends. Fig. 10 demonstrates the measured and the simulated results of this design. As seen from this figure, the measured s-parameters agree very well with the simulated results from HFSS.

For this design, a reflection of better than 13.6 dB for the whole frequency band has been achieved. Similar to the silicon case, the measured insertion loss is slightly higher than the simulated results due to the fact that the simulations include perfect conductors and the ohmic losses were omitted. A non-deembedded insertion loss of better than 1.1 dB up to 20 GHz has been measured. The measured insertion loss of this structure includes the insertion loss of two vertical transitions in a back-to-back configuration along with the ohmic loss of the

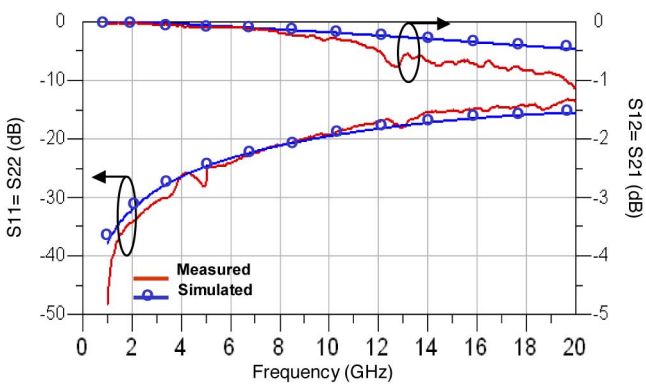

Fig. 10. Measured and simulated response of the whole structure consisting of two back-to-back microstrip-to-microstrip vertical interconnects along with the CPW-to-microstrip feed lines at both ends on GaAs. (Color version available online at: http://www.ieeexplore.ieee.org.)

1-mm-long microstrip line, which connects these two transitions. There are also two 600-μm-long sections of microstrip line, right after the CPW pads, which have to be considered when deembedding the excess loss terms. To get a more accurate characterization of the transition, the loss of the line sections included in the designs (approximately a total of 2.2-mm-long microstrip line) are deembedded. Fig. 11 demonstrates the insertion loss of the simulated and measured structure before and after deembedding. The response of the back-to-back transition has been extracted from the measurements and is plotted in this

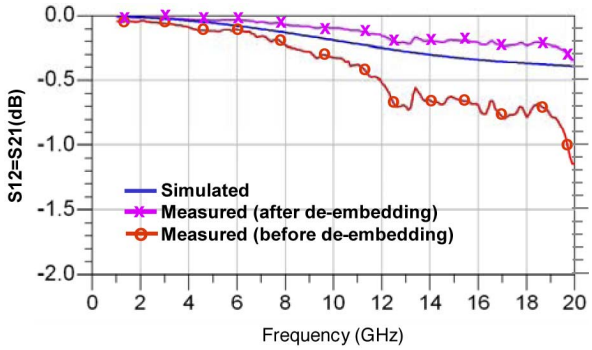

Fig. 11. Simulated and measured response of the whole structure consisting of two back-to-back microstrip-to-microstrip vertical interconnects along with the CPW-to-microstrip feed lines at both ends on GaAs. (Color version available online at: http://www.ieeexplore.ieee.org.)

figure. Consequently, the insertion loss per vertical transition has been found to be less than 0.2 dB for the frequencies up to 20 GHz.

V. Conclusion

Novel microstrip architectures for multiwafer vertical interconnects compatible with industry-standard silicon micromachining and GaAs active wafer technology have been demonstrated. The transitions show very low insertion loss and good return loss for frequencies up to 20 GHz. These designs open new opportunities for further integration of multiwafer architectures in a new class of 3-D circuits. Since these transitions are based on a microstrip architecture, the presented designs are very flexible and will result in significant reduction of chip size along with cost and power consumption.

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