Fig. 3 *Current against voltage of packaged multi-cell MPS diode on 10 μm thick and 1.4×10^{16} cm^{-3} doped epilayer*

——— RT
– – – – 125°C
· · · · · 250°C

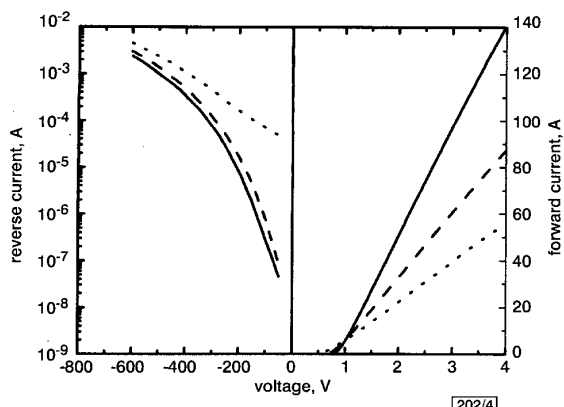**Fig. 4** *Current against voltage of packaged multi-cell MPS diode on 6 μm thick and 2.1×10^{16} cm^{-3} doped epilayer*

——— RT
– – – – 125°C
· · · · · 250°C

Results and discussion: The leakage current for a single MPS cell, with an epilayer of 10 μm and a doping density of 1.4×10^{16} cm^{-3}, was measured first. By way of comparison, a *pin* and a Schottky diode were fabricated from the same substrate, using exactly the same design parameters and optimised MJTE structures. The forward voltage drop and the best reverse leakage current of all three devices are shown in Fig. 2. It is clear that the MJTE region provided excellent edge termination which made it possible for SBD, MPS and *pin* diodes to reach similar high blocking voltages. The forward current was limited by the chip level measurement with a probe station. It should be noted that the MPS leakage current indeed closely resembled that of the *pin*, while the leakage current of the Schottky diode far exceeded that of the MPS. Note also that the forward voltage drop of the MPS closely resembled that of the Schottky. The *pin* diode at 2 V forward drop, however, had not yet turned due to the large bandgap of 4H-SiC. After the chip level probing of the single cells, multi-cell MPS diodes were packaged and tested. Fig. 3 shows the forward and reverse characteristics of a packaged device, based on the 10 μm epilayer structure. Measurements at room temperature (RT), 125°C, and 250°C are shown. Note that at RT, the forward current is 35 A at 2 V and 90 A at 4 V. We were able to achieve the target of 600 V with a total current of 140 A by packaging MPS cells fabricated in the 6 μm 2.1 × 10^{16} cm^{-3} doped epilayer structure, as seen in Fig. 4. This packaged diode consists of 12 MPS cells, with a total active area of 9.4 mm^2. Reverse breakdown occurred at over –800 V for the individual cells although the packaged diode was only measured up to 600 V. The decrease in forward current with temperature is expected, based on a reduction of the carrier mobility. Assuming a mobility temperature dependence of T^{-m}, Fig. 4 provides a value of $m \simeq 1.6$, close to the value of 3/2 for scattering

dominated by lattice vibrations. It should be noted that the change in the reverse leakage current is very small at 125°C, in contrast to that of Si diodes. The leakage current may be decreased further by the elimination of the 'weakest link' among the 12 cells; this then becomes a yield issue. The trend towards SiC wafers with smaller defect densities will help in reducing diode leakage. The packaged diodes have been used in $V_{dc} = 400$ V motor control systems and the conduction power loss due to the reverse leakage current is negligible even at 250°C. Motor control results will be published later.

Conclusions: MPS diodes with optimised MJTE structures have been developed. The results clearly show that the MPS diodes combine the best features of the SiC *pin* and the SiC Schottky diodes. Diodes using multiple MPS cells have been packaged and successfully operated at 125°C and 250°C. Up to 140 A DC current has been achieved for a packaged 4H-SiC MPS diode.

P. Alexandrov, W. Wright, M. Pan and M. Weiner (*United Silicon Carbide, Inc., 100 Jersey Ave, Bldg. D, New Brunswick, NJ 08901, USA*)

J. Zhao (*SiCLAB, Department of ECE, Rutgers University, 94 Brett Road, Piscataway, NJ 08854, USA*)

E-Mail: jzhao@ece.rutgers.edu

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Ku-band (12.6 GHz) SiGe/Si high-power heterojunction bipolar transistors

Z. Ma, S. Mohammadi, P. Bhattacharya, L.P.B. Katehi, S.A. Alterovitz, G.E. Ponchak, K.M. Strohm and J.-F. Luy

Large-area multifinger Si$_{0.7}$Ge$_{0.3}$/Si heterojunction bipolar transistors for high-power and high-frequency operation have been designed, fabricated and characterised. For a nine-emitter finger device, an f_{max} of 100 GHz was achieved with a maximum available gain of 14 dB. The peak power-added efficiency in the Ku-band (12.6 GHz) in the common-base configuration for a 15-emitter finger device was 23% with associated power gain of 7.4 dB and an output power of 22 dBm under class AB operation. The device delivered a maximum output power of 24.4 dBm under the same matching conditions.

Introduction: The development of SiGe-based monolithic microwave integrated circuit (MMIC) power amplifiers can lead to the promise of an Si-based system-on-a-chip. Small-signal amplifiers in the Ka- [1] and Ku-band [2] with SiGe-based heterojunction bipolar transistors (HBTs) have been reported. However, large-signal power amplification with these devices has only been demonstrated up to X-band [3]. In this Letter we report, for the first time, excellent performance characteristics of SiGe/Si HBTs, grown by molecular beam epitaxy, in the Ku-band (12.6 GHz).

The device parameter of importance, which is often used to characterise the high-frequency performance of a power HBT, is the maximum oscillation frequency f_{max}. A high value of f_{max} can be realised in smaller devices, but with lower breakdown voltages and lower power levels [4]. However, in an SiGe-based power

HBT, which should have large emitter area A_E and large-breakdown voltage BV_{CEO}, the largest achieved f_{max} is 74 GHz [5]. To increase f_{max}, it is necessary to reduce the base resistance R_B and the base-collector junction capacitance C_{BC}. A multifinger device layout with high base doping concentration can significantly reduce R_B. To reduce the value of C_{BC}, the common-base (CB) configuration is often used for power applications, in which case the emitter-collector capacitance C_{EC} (which is smaller than C_{BC}) becomes the limiting factor for the frequency response.

emitter cap	Si	n+	Sb	$2 \times 10^{20} \mathrm{cm}^{-3}$	250 nm
emitter	Si	n	Sb	$2 \times 10^{18} \mathrm{cm}^{-3}$	50 nm
spacer	$\mathrm{Si}_{0.7}\mathrm{Ge}_{0.3}$	i			3 nm
base	$\mathrm{Si}_{0.7}\mathrm{Ge}_{0.3}$	p+	B	$1 \times 10^{20} \mathrm{cm}^{-3}$	23 nm
spacer	$\mathrm{Si}_{0.7}\mathrm{Ge}_{0.3}$	i			7 nm
collector	Si	n-	Sb	$2 \times 10^{16} \mathrm{cm}^{-3}$	500 nm
sub-collector	Si	n+	As	$2 \times 10^{19} \mathrm{cm}^{-3}$	1000 nm
substrate	Si(100)	p-		$1 \times 10^{12} \mathrm{cm}^{-3}$	540 μm

a

b

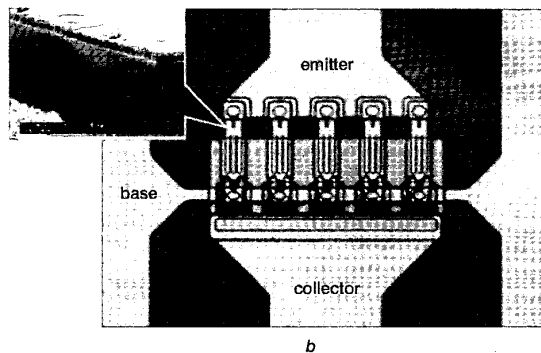**Fig. 1** *Schematic diagram of Si/SiGe/Si double heterostructure bipolar transistor and photomicrograph of 15-finger common-base HBT*

a Schematic diagram of device
b Photomicrograph
Inset: Airbridge structure

Device design and fabrication: The device heterostructure is shown in Fig. 1*a*. The arsenic-doped Si subcollector layer is first grown on a high-resistivity ($>10^4 \Omega$-cm) 001-Si substrate by chemical vapour deposition (CVD). The wafer is then loaded into the growth chamber of a molecular beam epitaxy system and the rest of the heterostructure is grown. The thicknesses and dopings of the various layers have been designed to enable the achievement of high f_{max} and a high collector breakdown voltage. In terms of device layout, a multifinger design was adopted for large power handling capacity. To minimise R_B and maximise f_{max}, the finger widths of 1 and 1.4 μm were used. The number of fingers varied from 9 to 30. To maintain a small C_{BC} and ensure good heat dissipation in these narrow emitter fingers, three emitter fingers are grouped together, surrounded by base electrodes of 1.5 μm width to form the subcell. The emitter finger lengths vary from 15 to 20 μm for different emitter widths. Interdigitated collector metal stripes are inserted between the subcells to form a distributed layout for reducing the thermal effects within the device region. These collector metal stripes are 8 μm in width. To reduce the parasitic capacitance, the layout is also designed to isolate the active device area with the external contact area during the fabrication process. For this purpose, all the electrode metals are connected to the outside via air bridges. The devices are fabricated by standard photolithography, wet and dry (reactive ion) etching, thin film metallisation and SiO₂ passivation. Fig. 1*b* shows the photomicrograph of a typical multifinger device. A device with 15 fingers of size 1.4×20 μm² has $A_E = 672$ μm² and a similar device with nine fingers of size 1.4×20 μm² has $A_E = 403$ μm².

Device performance: The DC characteristics of the fabricated SiGe/Si HBTs were measured with an HP 4145B semiconductor parameter analyser. The measured base-collector breakdown voltage (BV_{CBO}) is 20 V and the open-base collector-emitter breakdown voltage (BV_{CEO}) is about 13 V. No punchthrough was observed at these voltages. The offset voltage $(V_{CB,offset})$ in the CB configuration was measured to be about -0.6 V. The largest measured values of the common-emitter (CE) current gain β and the differential current gain $\Delta\beta$ were 18.6 and 24.8, respectively.
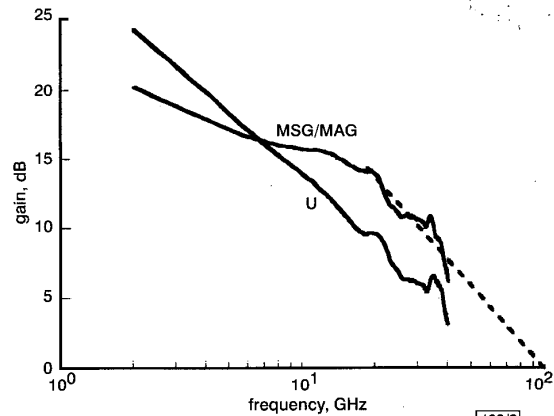

Fig. 2 *RF response of nine-emitter finger $(A_E = 403$ μm²$)$ common-base HBT*

The small-signal RF performance of the SiGe/Si HBTs was characterised by measuring the small-signal S-parameters with an HP 8510C network analyser. Fig. 2 shows the RF response of a nine-finger common-base HBT under the optimum bias conditions with $V_{CB} = 6.5$ V and $I_E = -69$ mA. The device demonstrates an extrapolated f_{max} of 100 GHz based on a -6 dB/octave roll-off. The power gain at 12.6 GHz is $MSG/MAG = 15.5$ dB and $U = 12.4$ dB. The RF response of the 15-emitter finger HBTs with the same type of layout was similarly measured. A slightly lower power gain is obtained from these larger area devices, with $MSG/MAG = 14.8$ dB and $U = 11.5$ dB at 12.6 GHz and exhibiting an f_{max} of 83 GHz.

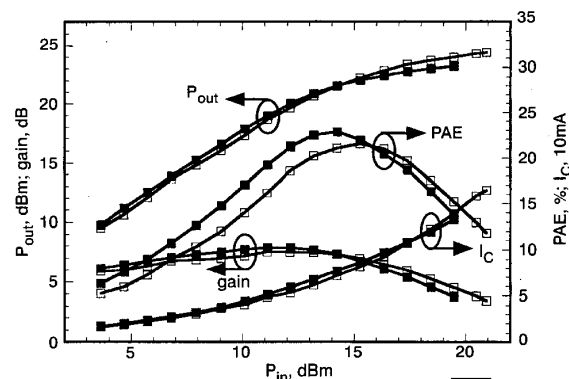**Fig. 3** *Power performance of 15-emitter finger $(A_E = 672$ μm²$)$ common-base HBT biased under class AB operation at optimum source and load impedance matching points*

22 dBm output power (P_{out}) and 7.4 dB associated power gain at peak PAE of 23% were obtained. Highest P_{out} was 24.4 dBm
—■— $V_{CB} = 6$ V
—□— $V_{CB} = 7$ V

The 15-emitter finger $(A_E = 672$ μm²$)$ common-base SiGe/Si HBTs were characterised with a Focus Microwave source/load pull system. The output power P_{out}, power gain and the power added efficiency (PAE) were measured on wafer as a function of input power P_{in} at 12.6 GHz under continuous wave mode. No special heat dissipation technique or external ballast resistors were incorporated. Fig. 3 shows the power performance of a typical device, along with the collector current under different bias conditions. The CB HBT was biased at $V_{CB} = 6$ V and 7 V and $V_{EB} = -0.668$ V in order to provide class AB operation. The matching points ($\Gamma_s = 0.71\angle176°$ and $\Gamma_L = 0.66\angle121°$) were optimised for

maximum P_{out}. The input matching is very close to the edge of the Smith chart, indicating the small input impedance. The class AB operation can be seen from the power gain change with the input power. Smaller power gain values at the low input power levels are ascribed to the low collector current at low bias. As the input power level is increased, the collector current (DC and AC) is also increased and the maximum power gain is then reached. Beyond that point, the swing of the output signal will be limited and the increase of the output power with increase in input power is slowed down. Therefore, the power gain drops. The highest power gain of 7.9 dB at P_{in} of 12.2 dBm was measured with $V_{CB} = 6\,\text{V}$. The peak PAE of 23% was achieved for 0.5 dB power gain compression. The output power P_{out} at the peak PAE is 22 dBm. With V_{CB} biased at 7 V, slightly higher P_{out}, 22.3 dBm at the peak PAE (21.5%), was measured with associated power gain of 7 dB. The P_{-1dB} is ~23 dBm (200 mW) and the maximum P_{out} was measured to be 24.4 dBm. At the quiescent bias point, the collector current is 14 mA and it was driven to 77 and 81 mA at the peak PAE, for V_{CB} of 6 and 7 V, respectively. The final saturation power was not measured owing to the DC current limit, which was set to prevent the device from burning out. No oscillation was observed during the measurements. To the best of our knowledge, these are the first large-signal measurements made on SiGe/Si HBTs in the Ku-band.

Z. Ma, S. Mohammadi, P. Bhattacharya and L.P.B. Katehi (*Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122, USA*)

S.A. Alterovitz and G.E. Ponchak (*NASA Glenn Research Center, 21000 Brookpark Road, Cleveland, OH 44135, USA*)

K.M. Strohm and J.-F. Luy (*Daimler-Chrysler Research Center, Ulm, Germany*)

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Transistor action in GaP/TmP/GaAs heterostructure

Ching-Hsi Lin, R.J. Hwu and L.P. Sadwick

Transistor action in a gallium phosphide/thulium phosphide/gallium arsenide (GaP/TmP/GaAs) structure with a GaP emitter, TmP base, and GaAs collector is reported. The emitter-base junction was constructed through wafer bonding and the base-collector junction was formed by epitaxial growth of TmP on GaAs in a molecular beam epitaxy system. From the I-V measurements, a common base current gain $\alpha \approx 0.55$ measured at $V_{CB} = 0$ was obtained at room temperature.

Introduction: In semiconductor-metal-semiconductor (SMS) transistors [1, 2], electrons are thermionicly injected through the forward-biased emitter-base Schottky junction. These hot electrons then cross the thin metal base with little scattering and are finally collected by the reverse-biased base-collector Schottky junction. Due to the low base resistance and short base transit time, it was predicted that metal base transistors would have a high frequency performance and this has made such devices attractive candidates for ultrahigh speed applications. However, it was demonstrated that, in many cases, the metal base was not continuous and the electrical characteristics were dominated by pinhole conduction, where the electrons directly flow through pinholes in the metal base. The existence of pinholes in the base metal film greatly increases the common-base current gain α. This is primarily due to the barrier lowering by the electrons injected in the pinhole, also to the disappearance of electron loss by scattering at interfaces and in the metal [3]. To limit the pinhole effects, in this Letter we report transistor action in a GaP/TmP/GaAs structure, where the base-collector junction was made by molecular beam epitaxial (MBE) growth of TmP on GaAs substrates, while the emitter-base junction was constructed through wafer bonding. The reason for using rare-earth compound, TmP, is primarily due to its high thermodynamic stability during high temperature growth and annealing.
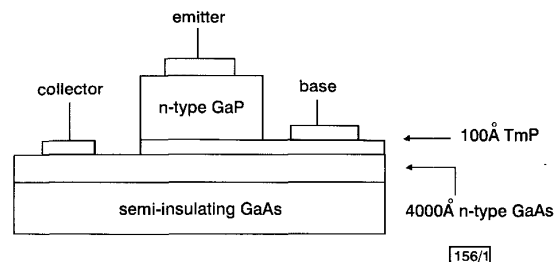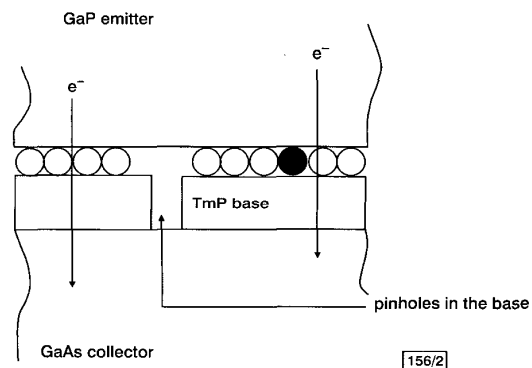

Fig. 1 *Schematic diagram of GaP/TmP/GaAs transistor*

Fig. 2 *Schematic diagram showing bonding between GaP emitter and TmP base, and electron transport through base*

● chemically bonded
○ Van der Waals bonded

Results and discussions: The transistor layer structure is shown in Fig. 1, where the emitter-base junction was formed by annealing a small piece of (001) GaP wafer ($N_D = 2 \times 10^{18}\,\text{cm}^{-3}$, sulphur doped), and the TmP/GaAs Schottky diode together at 500°C for 30 min in a forming gas environment (90% N$_2$ and 10% H$_2$) with the wafer held in compression. The small piece of GaP wafer was face-to-face clamped tightly to the TmP epilayer during annealing. Prior to wafer bonding, the GaP native oxides were removed with a solution of H$_2$O:H$_3$PO$_4$ (10:1 mixture). The use of GaP as the emitter has the advantage of providing a larger bandgap and a higher barrier to the TmP base so as to supply hotter electrons to the collector. The base-collector junction was formed by growing TmP on a GaAs substrate (a semi-insulator (001) GaAs wafer with 4000 Å thick Si-doped ($N_D \approx 5 \times 10^{17}\,\text{cm}^{-3}$) GaAs epilayer on top) at 550°C in the MBE system. Dimensions of the emitter, base, and collector are approximately 4, 9, and 16 mm^2, respectively. Owing to the lower temperature and the lower pressure