nology has been studied. Experimental results show that the He
plus RPN process provides better characteristics in reducing the
gate current and thickness of gate dielectric films for a thinner
gate oxide in the 8-22 A range. In addition, He can drive enough
nitrile into the top of the gate oxide to form a stoichiometric
nitrided layer, thus preventing the gate dielectric films from being
damaged under a high-density plasma environment.

Acknowledgment: The authors would like to thank the members of
R&D in Taiwan Semiconductor Manufacturing Co., Ltd., for the wafer
fabrication and technical support. This work was supported by the
National Science Council under Contracts NSC89-2215-E-
006-035.

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8 January 2001
Electronics Letters Online No: 20010515
DOI: 10.1049/el:20010515

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High power X-band (8.4 GHz) SiGe/Si heterojunction bipolar transistor

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A high-performance double-mesa type SiGe/Si power HBT at
X-band (8.4 GHz) frequency is demonstrated. Under continuous
wave operation, a single 20-finger common-base Si1-xGe2xSi (x = 0.08)
emitter-finger HBT has an output power of
27.4 dBm and an associated power gain
of 7 dB, respectively. Under continuous
wave operation at 8.4 GHz, the device output power and the
associated power gain at a peak PAE of 32.3% are 27.4 dBm and
7 dB, respectively.

Device design and fabrication: The design of the n-p-n SiGe/Si
HBTs was initiated with the heterostructure design and an opti-
mised layout, taking into consideration the requirements for high
power handling capability, thermal stability and high-frequency
operation. A detailed description of the most important factors for
the HBT design can be found in our previous publication [3]. A
schematic diagram of the heterostructure grown by one-step CVD
is shown in Fig. 1a. A 20 nm Si1-xGe2xSi layer was incorporated in
the heterostructure as the active base region with a p-type doping
level of 8 × 1014 cm-3. These parameters ensure a short transit
delay across the base layer with a low base resistance. The thick
and lightly doped (3 × 1015 cm-3) collector layer ensures high
device breakdown voltages and is favourable for achieving high
PAE [3]. The layout of a six-finger (each of size 2 × 30 μm2) com-
mon-base HBT is illustrated in Fig. 1b. In this layout, every two
emitter fingers are grouped in a subcell to form a common contact
area at the end of the fingers and a 10 μm wide collector metal
stripe is inserted in between the two subcells. The total emitter
area of a 20-finger device, including the via-hole contact area in
each subcell, is 1560 μm2. This distributed layout reduces the para-
sic collector resistance of this large-area device and greatly assists
heat dissipation from the centre of the device. The heterostruc-
tures were fabricated into double-mesa type HBTs using standard

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Fig. 1 Schematic diagram of Si/SiGe/Si double heterostructure HBT
and layout of six-finger (2 × 30 μm2) common-base HBT showing distrib-
uted feature

a Schematic diagram
b Layout of six-finger HBT

Total emitter area of 20-finger common-base HBT is 1560 μm2.
Device performance: The measured base-collector breakdown voltage ($B_V(E_B)$) is $-25$ V and the open-base collector-emitter breakdown voltage ($B_V(E_O)$) is $-23$ V. Although the actual base layer of these devices is only 20 nm thick, no punch-through was observed before the avalanche breakdown occurred. These are the highest breakdown voltages that have been achieved for SiGe-based HBTs. Our study has shown that although the strained Si$_x$Ge$_{1-x}$ has a smaller bandgap than Si, high breakdown voltages can still be obtained by careful adjustment of the collector doping level. No collapse in the current gain was observed at any collector current level, indicating the excellent heat dissipation capability of the device. The measured small-signal power gain at (8.4 GHz) at moderate current levels is >11 dB. The large-signal performance of the device was tested on-wafer with no special heat dissipation techniques. Details of this procedure have been described in [4].

Acknowledgment: This work is being supported by NASA-GRC under Grant NCC.3-790.

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Symmetric bulk charge linearisation in charge-sheet MOSFET model

T.L. Chen and G. Gildenblat

An accurate, simplified version of the charge-sheet MOSFET model is developed using symmetric linearisation of the bulk charge as a function of surface potential. The resulting MOSFET model satisfies the Gummel symmetry condition and is verified by comparison with the exact results.

Compact MOSFET models used in circuit simulators are often developed with the help of bulk charge linearisation [1]. This leads to simplified and computationally efficient equations of the I-V characteristics and makes possible closed-form evaluation of the intrinsic charges and capacitances. The well-known disadvantage of this approach is a violation of the Gummel symmetry test [1]. We note in passing that there are numerous other mechanisms for the loss of the Gummel symmetry [2].

The purpose of this Letter is to introduce an alternative linearisation scheme for the bulk charge as a function of surface potential which has all the advantages of the original method [1] but passes the Gummel symmetry test. To separate the linearisation problem from the other aspects of the MOSFET model development we present symmetric linearisation within a context of the charge-sheet model [3]. For this model exact analytical expressions for the drain current and terminal charges are readily available [3, 4], which enables unambiguous evaluation of the accuracy of the symmetric linearisation approach.

Let $\phi$, $\psi$ denote the surface potentials at the source and drain ends of the MOSFET channel. Define the midpoint as a point with the surface potential $\phi_0 = (\phi + \psi)/2$ and set

$$\phi_0(\phi) \approx \phi_0(\psi_0) + \left. \frac{d\phi_0}{d\phi} \right|_{\phi=\psi_0} (\phi - \psi_0)$$

where $\phi_0(\phi)$ is the absolute value of the bulk charge per unit channel area corresponding to the surface potential $\phi$. The absolute values of $\phi_0(\phi)$ and $\phi_0(\psi_0)$ are respectively

$$\phi_0^{(1)} = \frac{1}{2} \left( \phi + \psi - \sqrt{\phi^2 + 4 \phi_0^2} \right)$$

$$\phi_0^{(2)} = \frac{1}{2} \left( \phi + \psi + \sqrt{\phi^2 + 4 \phi_0^2} \right)$$