A 500μW 2.4GHz CMOS Subthreshold Mixer for Ultra Low Power Applications

Hanil Lee and Saeed Mohammadi

School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 47907, U.S.A.

***Abstract* — This paper presents an integrated 2.4GHz ultra low power CMOS frequency down-converting active mixer based on a single balanced Gilbert-cell resistor-loaded topology where all MOS transistors of mixer core are optimally biased in subthreshold region. At only 500μW DC power consumption under 1.0V power supply and small LO power of -9dBm, this mixer has a measured power conversion gain of 15.7dB and DSB noise figure of 18.3dB. At same DC power dissipation and LO power, -9dBm IIP3 and -28dBm input P1dB are obtained while the input return losses at RF and IF ports are better than -20dB and -8dB, respectively. Measured LO to IF and LO to RF isolations are more than 22dB and 33dB, respectively. With a help of a newly defined figure of merit that contains the effects of conversion gain, noise figure, linearity, LO power, DC power consumption and operating frequency, it is shown that the subthreshold mixer presented here is superior to conventional CMOS mixer designs reported in the literature.**

***Index Terms* — Low power, subthreshold, CMOS, mixer.**

I. Introduction

Due to the limited battery lifetime, the demand for low power wireless transceivers operating at GHz band has led to extensive research on novel low power RF circuit and system designs. As one of the power-hungry RF front-end blocks, frequency down-converting mixers are well studied and many low power RF CMOS mixer circuit topologies have been recently proposed [1]-[6].

To achieve low power operation, circuit stacking methods are implemented to reuse the current or share power supply by stacking the LNA on top of the mixer [1] or combining the oscillator and the mixer [2]. These approaches have resulted in an increase in supply voltage due to stacking of transistors as well as requirement for large sized capacitors to make ideal AC ground. Alternatively, cascode implementation can be applied to the mixer design, by stacking PMOS transistors on NMOS transistors [3]. However, high dc supply voltage of 1.8V can cause the device breakdown as well as large power dissipation.

To reduce power dissipation, high-Q passive components in the inductor-capacitor (LC) tanks [4] and transformers [5] can be used. This approach has led to an increase of chip area and fabrication cost. Furthermore, the bandpass response of the transformer causes a narrow 3-dB bandwidth.

Body contact of MOSFET is used as a terminal for RF input of mixers to eliminate the stacked transconductance transistors for low supply voltage and low power consumption [6]. But for this bulk driven technique a twin-well technology is required. In addition, accurate modeling of the back gate, the parasitic p-well resistance and the deep n-well diodes are necessary.

It is challenging to reduce DC power consumption of CMOS RF mixers with other performances properly maintained. As the possibility of RF CMOS subthreshold design for ultra low power LNAs has been demonstrated in our previous work [7], this paper proposes an RF CMOS subthreshold active mixer design based on subthreshold biasing of MOS transistors. In this approach without using large supply voltage, expensive high-Q components or modified processing technologies, the DC power dissipation of the RF mixer is significantly lowered while other performances are maintained.

In order to demonstrate the advantages of subthreshold RF CMOS mixer design, we have implemented a 2.4GHz CMOS active mixer in a 0.13μm technology that operates in subthreshold regime and consumes only a few hundreds of μW of DC power. The proposed subthreshold mixer achieves an improved power conversion gain to DC power dissipation ratio with an acceptable noise figure.

II. Circuit Design

Fig. 1 shows the drain current (I_{DS}) as a function of gate source voltage (V_{GS}) for normal size transistor (width of W1) operating in superthreshold region and relatively larger size transistor (width of W2 > W1) operating in subthreshold region. Drain current is dominated by drift mechanism in superthreshold region resulting in square-root dependence of transconductance g_m on I_{DS}. In subthreshold region, drain current has an exponential dependence on gate voltage due to dominant diffusion mechanism resulting in a higher g_m to I_{DS} ratio of subthreshold region. Therefore, the transconductance g_m that satisfies the required mixer conversion gain in subthreshold region (g_{m2}, slope at Q2), which is equal to

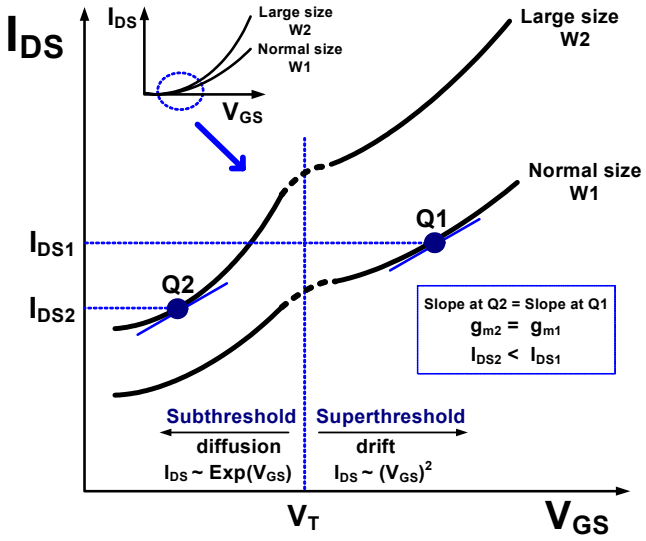

Fig. 1. Characteristic graph of the drain current (I_{DS}) versus the gate source voltage (V_{GS}) around threshold voltage for two different sized transistors.

the transconductance g_m of the smaller transistor in superthreshold region (g_{m1}, slope at Q1), can be obtained at a smaller drain current (I_{DS2}). Hence, the power dissipation of the mixer can be reduced using oversized MOS transistor operating in subthreshold design.

Since oversized transistors in LO switching section are operating in subthreshold region, higher g_m can be obtained at a given bias current. Therefore, switching slope of differential LO section becomes steeper, which leads to more ideal square LO switching and accordingly higher conversion gain. Furthermore, required input voltage swing for switching LO transistors to steer the small subthreshold bias current can be made very small. Therefore, the required LO signal power is expected to be smaller in subthreshold mixer design, which has an additional benefit in reducing the DC power consumption of LO signal generation block.

Additionally, circuits designed with MOS transistors biased in subthreshold regime operate with lowered voltage headroom, resulting in smaller power supply (V_{DD}) and further reduced DC power dissipation.

To demonstrate the expected advantages of RF subthreshold CMOS mixer design, a commonly used single balanced Gilbert-cell mixer with resistor-loaded output topology is chosen as shown in Fig. 2. In this topology there is neither stacked source degenerate inductor nor tail current source to lower the voltage headroom and required supply voltage (V_{DD}). To further reduce DC power consumption of a CMOS mixer, NMOS transistor of transconductance section (M1) and those of

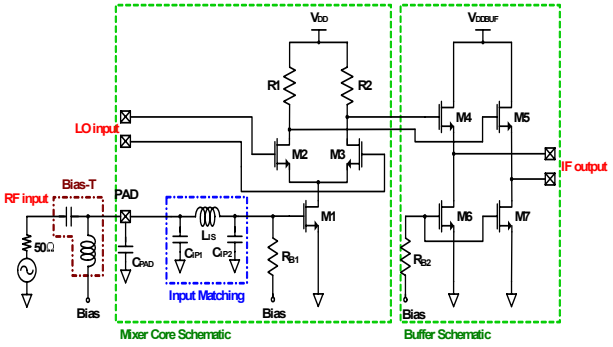

Fig. 2. Circuit schematic of the proposed GHz CMOS mixer with RF input test environments, where MOSFETs of transconductance section and LO switching section are biased in subthreshold region for ultra low power RF applications.

LO switching section (M2 and M3) are biased and optimized in subthreshold region (threshold voltage V_{TH} ~ 0.45V) while the supply voltage (V_{DD}) is lowered to about 1.0V. W/L ratios of these transistors are made larger than normal design and optimally chosen to increase the gain of the mixer at small DC power and to help matching the input impedance to 50Ω without use of a source degeneration inductor (L_S). Although voltage headroom increases due to DC voltage drop at resistors, resistors instead of inductors are used as loads of this mixer for small chip size and low IF output frequency applications. Hence power dissipation can be reduced further by using high-Q inductive loads to reduce voltage headroom for high output frequency applications.

Output buffer is designed as a pair of NMOS source follower (M4, M5) with active current source (M6, M7)

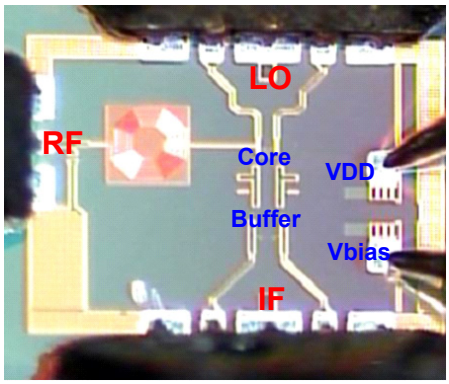

Fig. 3. Microphotograph of the proposed GHz CMOS Mixer with RF and DC test probes. Chip size is 1.0mmx0.8mm including three RF pads and two dc pads.

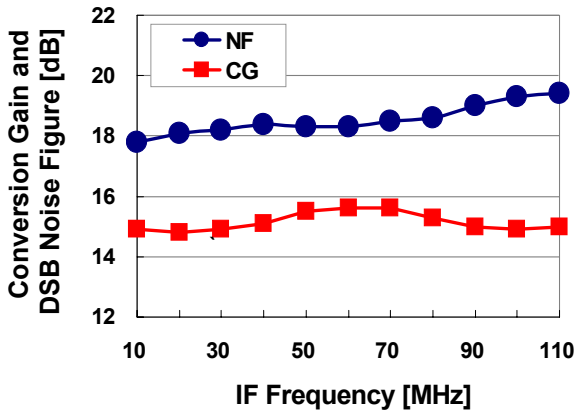

Fig. 4. Measured power conversion gain and DSB noise figure of Mixer for different IF frequency.

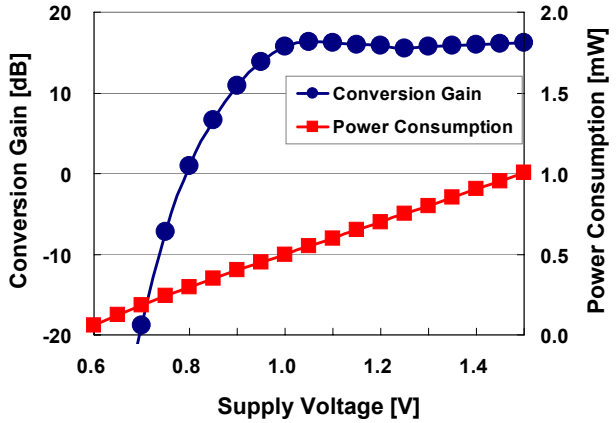

Fig. 5. Measured power conversion gain and DC power consumption with respect to power supply voltage.

for flexible testability, since each source output can be connected with a bias-T for variable DC bias voltage source as well as 50Ω resistor load. Fig. 3 shows a microphotograph of the fabricated chip in 0.13µm CMOS technology. Mixer area is 1.0×0.8mm^2 including the test pads.

III. Measurement Result and Evaluation

All measurements of the proposed subthreshold mixer are made on-wafer using 50Ω coplanar probes. Fig. 4 shows measured power conversion gain and double sideband (DSB) noise figure of the mixer as a function of IF output frequency by tuning -35dBm RF signal from 2.31 to 2.41GHz and -9dBm LO signal fixed at 2.3GHz. The mixer has a 15.7dB power conversion gain and an 18.3dB DSB noise figure at a supply voltage of 1.0V, and a power consumption of 500µW with small LO signal power of -9dBm. To author's best knowledge, this is the first time an integrated 2.4GHz CMOS active mixer with good performances and a power consumption below 1mW is reported. Although mixer core and output buffer share the same supply voltage DC pad for feasible testability, power dissipation of the mixer core itself can be measured by applying 0V at the gate bias of active load transistors in output buffer (M6 and M7). Fig.5 shows the measured power conversion gain and DC power consumption as a function of supply voltage. Conversion gain above 10dB can be obtained over 0.9V supply voltage and 400µW DC power.

Single-tone 1dB compression measurement and two-tone large signal linearity measurement of the mixer under the same bias condition with 500µW power dissipation are shown in Fig. 6. The input referred 1dB compression point (IP1dB) was measured as -28dBm. A two-tone test at 2.355GHz and 2.360GHz was performed to measure the fundamental output signal power and the third order inter-modulation output signal power (IM3). Based on these measurements plotted in Fig. 6, the input third order intercept point (IIP3) of -9dBm is extrapolated.

Matching characteristics of mixer can be found with input return losses at RF and IF ports by S-parameter measurements. RF return loss is less than -20dB over the frequency range from 2.1GHz to 2.5GHz, and IF return loss is less than -8dB at frequencies from 10MHz to 3GHz. The measured LO isolation characteristics are 33dB LO to RF and 22dB LO to IF isolations, respectively, achieved by designing a fully symmetrical layout.

Table I summarized performances of the proposed mixer and other reported low power RF CMOS active mixers [5][8][9]. The overall performance of RF active mixers can be expressed by a newly defined figure of

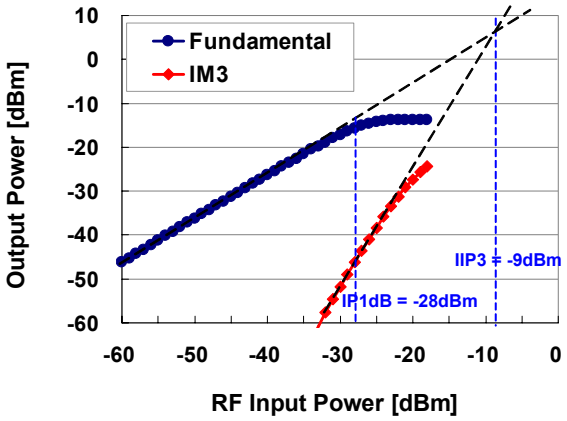

Fig. 6. Measured IIP3 and IP1dB of Mixer at 500µW DC power consumption.

TABLE I

SUMMARIZED PERFORMANCES OF THIS MIXER AND ITS COMPARISON WITH PREVIOUSLY PUBLISHED DATA. A FORMULA FOR FIGURE OF MERIT (FOM) IS IN EQUATION (1).

	Technology	RF	IF	P_{LO}	V_{DD}	P_{DC}	Gain	NF	IP1dB	IIP3	LO-RF	LO-IF	FOM
	CMOS	[GHz]	[MHz]	[dBm]	[V]	[mW]	[dB]	[dB]	[dBm]	[dBm]	[dB]	[dB]	[dB]
This Work	**0.13um**	**2.4**	**60**	**-9.0**	**1.0**	**0.5**	**15.7**	**18.3**	**-28.0**	**-9.0**	**33.0**	**22.0**	**51.3**
Ref. [5]	0.13um	2.5	10	-1.0	0.6	1.6	5.4	14.8	-9.2	-2.8	70.9	54.2	44.0
Ref. [5]	0.13um	2.5	10	-1.0	0.8	7.8	15.0	8.8	-16.9	-9.5	71.1	54.2	44.5
Ref. [8]	0.18um	2.4	1	-2.0	1.8	8.1	15.7	12.9	-	1.0	-	-	46.2
Ref. [8]	0.18um	2.4	1	-2.0	1.0	3.2	11.9	13.9	-	-3.0	-	-	45.3
Ref. [9]	0.18um	5.3	1	-3.6	0.9	5.0	8.3	24.5	-15.0	0.0	33.0	19.0	36.7
Ref. [9]	0.18um	5.3	1	-3.6	0.9	6.6	8.9	24.0	-16.7	-11.6	33.0	19.0	30.5

merit (FOM) which includes the effects of conversion gain (Gain), noise figure (NF), linearity (IIP3), required LO signal power (P_{LO}), operating frequency (f_O) and DC power consumption (P_{DC}) as follows [8].

$$\mathrm{FOM} = 10 \cdot \log\left(\frac{10^{(\mathrm{Gain} - 2\mathrm{NF} + \mathrm{IIP3} - 10 - P_{LO})/20} \cdot \frac{f_O}{1\mathrm{GHz}}}{\frac{P_{DC}}{1\mathrm{mW}}} \right) \quad (1)$$

According to the comparison results in Table I, the proposed subthreshold mixer has better overall performance than circuits designed in strong inversion.

IV. CONCLUSION

An ultra low power CMOS down-converting active mixer using subthreshold design scheme in a standard low cost 0.13μm CMOS technology with six metal layers is designed and implemented. To substantially reduce the DC power consumption while other performance characteristics are maintained, the proposed mixer uses oversized NMOS transistors in transconductance and LO switching sections, which are optimized to operate more efficiently in the subthreshold region. At DC power consumption of only 500μW under 1.0V power supply and small LO signal power of -9dBm, this 2.4GHz mixer achieves a high measured power conversion gain of 15.7dB and DSB noise figure of 18.3dB. Under the same bias condition, the measured IIP3 is -9dBm and the return loss at RF and IF ports are better than -20dB and -8dB, respectively.

This subthreshold mixer has better overall performance than recently published low power CMOS active mixers. Linearity performance can also be made better by increasing the bias current or using a degeneration inductor within permitted chip size. Noise figure of the mixer can be further reduced by utilizing high-Q inductors as input matching and output load ones. By further reducing the supply voltage of the mixer in a more advanced CMOS technology, the power consumption of the proposed subthreshold mixer can be further reduced.

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