Heterogeneously Integrated 10Gb/s CMOS Optoelectronic Receiver for Long Haul Telecommunication

Hasan Sharifi and Saeed Mohammadi

Birck Nanotechnology Center and School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA

***ABSTRACT* — A fully integrated 10Gb/s 1.3 to 1.55µm CMOS optoelectronic receiver is demonstrated for the first time. By heterogeneously integrating of a CMOS transimpedance amplifier (TIA) with an InGaAs/InP PIN photodiode using a recently developed self-aligned wafer-level integration technology (SAWLIT), operation at 10Gb/s is achieved. The CMOS transimpedance amplifier exhibits a transimpedance gain of 51dBΩ and a bandwidth of 6.1GHz.**

***Index Terms* — Advanced Electronic Packaging, CMOS analog integrated circuits, Optoelectronic receiver, PIN photodiode, Transimpedance amplifier.**

I. Introduction

Low-cost wide-band optical communication systems are essential part of the expanding communication market due to their high data rate, extremely high channel capacity and insensitivity to electrical interference. The receiver systems often use a high-gain transimpedance amplifier in conjunction with a photodiode to transform the optical signal into electrical signal. They are traditionally built using either hybrid or integrated approaches based on high speed bipolar, or InP HEMT technologies.

In hybrid receivers, a photodiode is fabricated on a separate die from the amplifier. The two components are either packaged separately or together using an optical package. A loss in sensitivity of hybrid optoelectronic receivers due to small area of the PIN photodiodes is a consequence of extra parasitic capacitances of the hybrid implementation. In integrated optoelectronic receivers, the transistors of the amplifier and photodiode are built on a common substrate using either shared heterostructure (same heterostructure for transistor and PIN diode) or stacked heterostructure (PIN structure is grown on top of the transistor heterostructure). The advantages of using integrated optical receivers are their smaller size, and higher data rate for a given optical power sensitivity, when compared with their hybrid counterparts. The drawbacks of using integrated optical receivers are the high cost associated with integrating photodiode and transistor technology and tradeoffs between the speed of the transistor and the sensitivity of the photodiode when utilizing a common heterostructure approach [1]-[4].

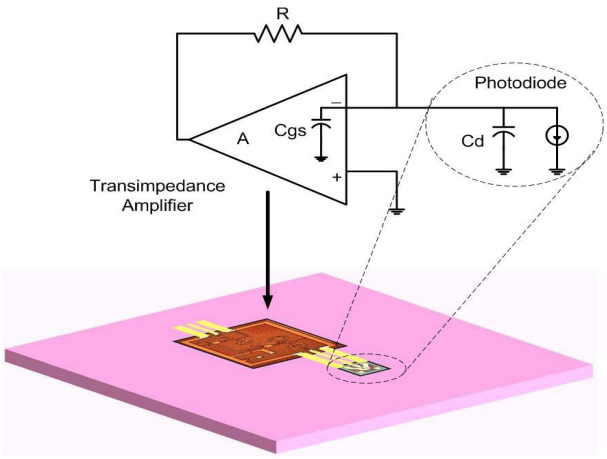

Fig. 1. Schematic and concept of a heterogeneously integrated optical receiver system using a CMOS transimpedance amplifier and an InP PIN Photodiode.

Integrated Photo-detectors based on Silicon CMOS technology have been recently reported in the literature for visible spectrum [5][6][7]. The work presented in [5] is at low data rates (3Gb/s) while [6] and [7] present high data rate application (10-15Gb/s) using silicon-on-insulator (SOI) process for visible spectrum. An apparent performance degradation reported in [7] is due to bondwire inductances as well as other parasitic capacitances. Non of these technologies are appropriate for long haul communication systems as the wavelength is not compatible with optimum spectrum for optical fibers (near infrared wavelengths of 1.3~1.55µm). Due to low absorption of Si around near infrared, long haul 10Gb/s and 40Gb/s systems are only realized in InP technology [8]. The obvious solution to achieve high sensitivity Si based optoelectronic systems for long-haul communications is to heterogeneously integrate InP or GaAs photodiodes with Si circuitry. Along this path, fluidic self-assembly of microstructures on Si substrate has been demonstrated by Smith *et al* [9]. In this technique, GaAs LED microstructures with trapezoidal shapes suspended in a fluid are self-assembled onto

trapezoidal holes etched in Si substrate through fluidic transportation. The technique has not been applied to integration of Si devices/circuits and InP photodiodes.

In this work we have demonstrated for the first time a fully integrated 10Gb/s Si-based optoelectronic receivers at near infrared spectrum. We have utilized a heterogeneous integration technique to integrate the receiver. Fig. 1 shows the schematic and integration concept of the system. By tightly integrating a wide-band CMOS transimpedance amplifier with a commercial InP PIN photodiode, we have substantially reduced parasitic capacitances and inductances between the two chips. As a result, a CMOS-based 10Gb/s optical data at 1.55µm wavelength is made possible.

II. Design of the Transimpedance Amplifier

To demonstrate the integration concept, we have used a 0.13µm RF CMOS technology to design a two-stage cascode transimpedance amplifier with shunt-shunt feedback network, although any commercial transimpedance amplifier can also be used. The Cascode configuration eliminates the bandwidth degradation due to Miller effect. This bandwidth degradation is significant in deep sub-micron CMOS circuits, where the gate-drain capacitance can be as high as gate-source capacitance. The shunt-shunt feedback lowers the input impedance of the amplifier such that most of photocurrent couples to the amplifier instead of the parasitic capacitance of the PIN diode. The dominant pole of the transfer function due to the photodiode junction capacitance (C_d) is significantly improved. As a result, the bandwidth of the amplifier is extended.

In this work, a multi-pole bandwidth enhancement technique for wide-band amplifier designs is used [10]. The schematic of the transimpedance amplifier is shown in Fig. 2. In order to increase the bandwidth, a series inductor (L_1=1.8nH) is inserted between the transistor's gate terminal and PIN diode. This inductor generates a third order low pass filter with the parasitic capacitance of the PIN diode (C_d=200fF) and the input capacitance of the amplifier. R_1=300Ω is used as a shunt-shunt feedback. The width of the transistors M1, M2, M3 and M4 is 140µm. Inductor L_3=0.9nH is used to separate output capacitance of TIA from the capacitance of the next stage. PMOS current mirrors are used to feed both amplifying stages.

Transimpedance gain of optical receivers expressed in dBΩ can be found from the S-parameters of the amplifier based on the following equation [4]. Note that the gain of a perfect through line (S_{21}=1) matched at both ends is about 34dBΩ.

$$Transimpedance\ Gain = 20Log(50.\left|\frac{S_{21}}{1-S_{11}}\right|) \qquad (1)$$

The designed amplifier has a simulated transimpedance gain of 51dBΩ over a bandwidth of 7GHz, while output is matched with better than -10dB. The inset of Fig. 2 shows the photomicrograph of the transimpedance amplifier with dimensions of 1.2mm×0.85mm.

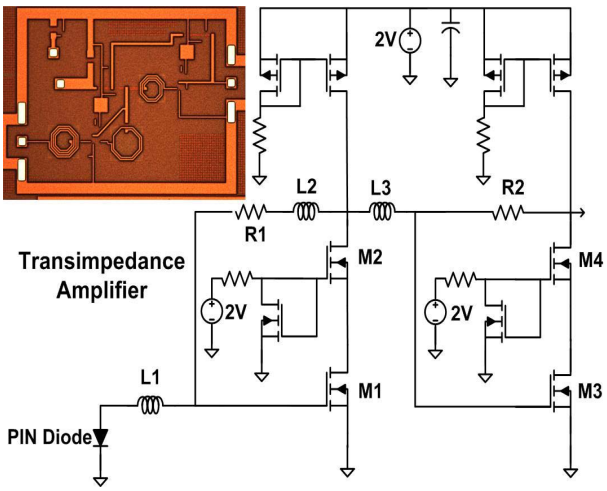

Fig. 2. Schematic of the designed optical receiver in 0.13µm CMOS technology. The inset shows the Photomicrograph of the amplifier.

III. Integration of the Transimpedance Amplifier and Photodiode using SAWLIT

In [11], we have developed a self-aligned wafer-level integration technology (SAWLIT) suitable for Microwave Integrated Circuit (MMIC). The technology is applied to integrate a 10GHz CMOS receiver chip with embedded passive components and a 10GHz filter. In this work, we have utilized the process to tightly integrate two disparate chips namely the designed CMOS amplifier and a commercial 1310nm-1550nm InGaAs/InP PIN Photodiode from Microsemi. The integration technology is briefly described in this section. The details of the integration technology is provided elsewhere [11][12]. First, a Si carrier substrate is etched using deep reactive ion etcher (DRIE) with holes slightly larger (~20µm) than the size of the two chips. Then the chips are inserted in the holes and are self-positioned while the gap between the chips and Si substrate is filled with Poly-Di-Methyl-Silicone (PDMS). After applying a planarization layer (SU-8) and opening vias, chip to substrate interconnects are printed using photolithographic defined metallization with very narrow width (25µm).

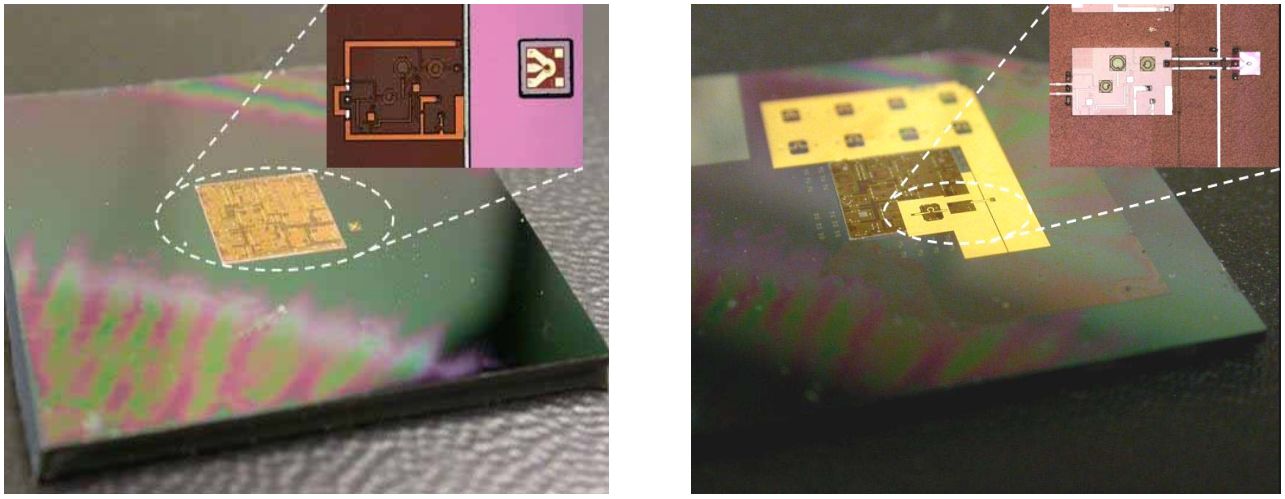

Fig. 3. Integration of the optical receiver using SAWLIT. (left) PIN diode and Si chips are integrated on the carrier substrate. (right) 3μm Au interconnect metallization is printed using a lift-off process.

This is essential for 10Gb/s operation of integrated optoelectronic receivers as extra parasitic capacitances at the input of the transimpedance amplifier or the output of PIN diode can severely limit the bandwidth of the system.

Using SAWLIT, the designed CMOS transimpedance amplifier and a commercial 1310nm-1550nm InGaAs/InP PIN Photodiode are integrated on a high resistivity Silicon carrier substrate. The size of the PIN diode chip is 450μm×450μm. The PIN photodiode in Fig. 1 is usually modeled with a capacitor and a current source. The capacitance value of the diode is 200fF at a bias voltage of 5v. In order to improve the output matching of the transimpedance amplifier, an embedded series inductor (1nH) is added to the output of the amplifier on the carrier substrate. Fig. 3 illustrates the integration of the optical receiver.

IV. Measurement

Agilent 8722 network analyzer with on-wafer probe measurement is used to measure the S-parameters of the integrated optoelectronic receiver. Transimpedance gain is found from measured S-parameters using (1). Fig. 4(a) and (b) show simulated and measured transimpedance gain of the system, respectively. The measured transimpedance bandwidth is slightly degraded compared to the simulation results. Fig. 4(c) and (d) illustrate the output reflection S_{22} before and after integration (with the embedded inductor), respectively. Addition of 1nH embedded inductor to the output of the transimpedance amplifier improves the output matching to better than 10dB for frequencies above 4GHz. The overall power consumption using a 2V power supply is 45mW. Eye-diagram measurement is performed using a 10 Gb/s 1.55μm modulated laser source, Tektronix OTS 9010, gated with a 2^{31}-1 Pseudo-random pattern generator.

On-wafer probe measurement is used to feed the output signal of the optoelectronic system to a HP 54120B sampling oscilloscope. First, a through line (with no laser source) is measured as the reference measurement as shown in the inset of Fig. 5. Then a -10dBm optical signal is applied through a fiber optic to the system. Fig. 5 shows the measured results indicating open eye characteristics at 10Gb/s input data rate.

V. Conclusion

Heterogeneous integration of a high-gain CMOS transimpedance amplifier with InGaAs/InP photodiode is demonstrated using a self-aligned wafer-level integration technology (SAWLIT). To authors' best knowledge, this is the first demonstration of a 0.13μm CMOS based optoelectronic receiver at 10Gb/s for near infrared wavelengths (1.3-1.55μm).

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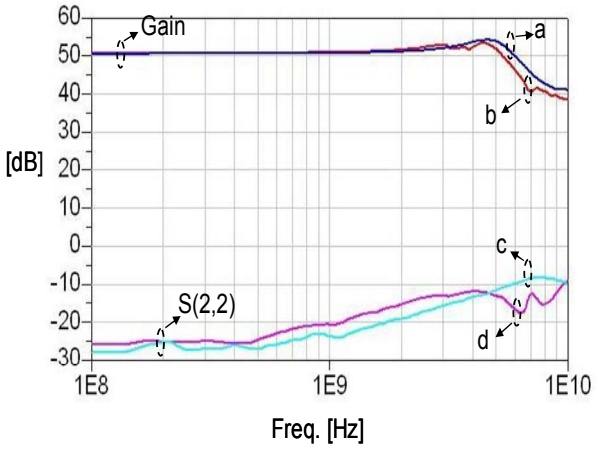

Fig. 4. (a) Simulated result of transimpedance gain of the optoelectronic receiver, (b) measured transimpedance gain of the entire system after integration, (c) measured S_{22} parameter before integration, and (d) measured S_{22} parameter after integration.

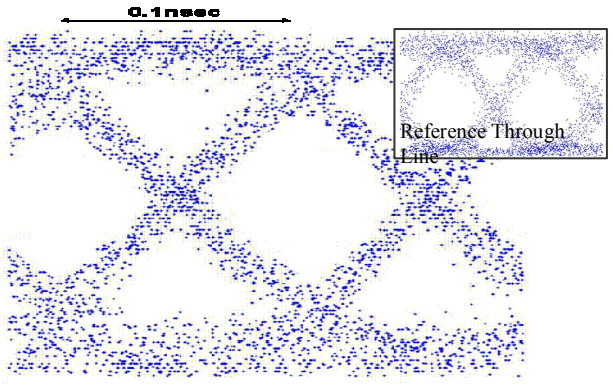

Fig. 5. Measured eye-diagram of the transimpedance amplifier at 10 Gb/s.

REFERENCES

[1] M. Ingels, and M. Steyaert, "A 1Gb/s 0.7um CMOS Optical Receiver with Full Rail-to-Rail Output Swing," IEEE J. Solid State Circuits, vol. 34, pp. 971-977, July 1999.

[2] P. Mitran, F. Beaudoin, and M. El-Gamal, "A 2.5 Gbit/s CMOS Optical Receiver Frontend," Proc. IEEE International Symposium on Circuits and Systems, vol. 5, pp. 441-444, May 2002.

[3] H. Kim, S. Chandrasekhar, C. Burrus, and J. Mauman, "A Si BiCMOS Transimpedance Amplifier for 10 Gb/s SONET Receiver," IEEE J. Solid-State Circuits, vol. 36, no. 5 , pp. 769-776, May 2001.

[4] S. Mohammadi, J. W. Park, D. Pavlidis, C. Dua, J. L. Guyaux and J. C. Garcia, "High-Gain GaInP/GaAs HBT Monolithic Transimpedance Amplifier for High-Speed Optoelectronic," *IEEE International Electron Device Meeting, IEDM,* pp. 661-664, 1998.

[5] S. Radovanovic, A. Annema, and B. Nauta "A 3-Gb/s Optical Detector in Standard CMOS for 850-nm Optical Communication," *IEEE J. Solid-State Circuits,* vol. 40, no. 8 , pp. 1706-1717, August 2005.

[6] B. Yang, J. D. Schaub, S. M. Csutak, D. L. Rogers, and J. C. Campbell, " 10-Gb/s All-Silicon Optical Receiver," *IEEE Photon. Technology Lett.* vol. 15, pp. 745-747, May 2003.

[7] C. L. Schow, L. Schares, S. J. Koester, G. Dehlinger, R. John, and F. E. Doany, "A 15-Gb/s 2.4-V Optical Receiver Using a Ge-on-SOI Photodiode and a CMOS IC," *IEEE Photon. Technology Lett.* vol. 18, pp. 1981-1983, Oct. 2006.

[8] B. Jalali, M. Paniccia, and G. Reed, "Silicon Photonics," *IEEE microwave magazine*, pp. 58-68, June 2006.

[9] H. J. Yeh, and J. S. Smith, "Fluidic Self-Assembly for the integration of GaAs light-emitting diodes on Si substrates," *IEEE Photon. Technology Lett.* vol. 6, pp. 706-708, June 1994.

[10] B. Analui and A. Hajimiri, "Multi-Pole Bandwidth Enhancement Technique for Transimpedance Amplifiers," *IEEE J. Solid-State Circuits,* vol. 39, no. 8, pp. 1263-1270, Aug. 2004.

[11] H. Sharifi, S. Mohammadi, L. P. Katehi, "Self-Aligned Wafer-Level Integration system," US Patent Pending, 2005.

[12] H. Sharifi, T. Choi and S. Mohammadi, "Self-Aligned Wafer-Level Integration Technology with High Density Interconnects and Embedded Passives," *IEEE Transaction on Advanced Packaging,* vol. 30, no.1, pp.11-18, Feb. 2007.