An Extremely Low Power 2 GHz CMOS LC VCO for Wireless Communication Applications

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***Abstract* — An extremely low power low phase noise CMOS LC voltage controlled oscillator (VCO) has been fully integrated in a commercial 0.18 µm CMOS process. To achieve low power and low phase noise, a complementary NMOS and PMOS cross-coupled differential LC structure is used. The LC tank is composed of octagonal-shaped inductors with 2 µm Al metal and standard NMOS varactors. The measured phase noise is -111dBc/Hz at 1 MHz offset from a 1.87 GHz carrier when the VCO core consumes only a 0.5 mW power from 0.9 V supply. The power consumption of 0.5 mW is the lowest reported in the literature for LC VCOs. This VCO has a figure of merit of -180 dBc/Hz and achieves a 7 % tuning range with a control voltage ranging from 0 ~ 1.4 V, while maintaining a tuning sensitivity of 93 MHz/V over its entire frequency range.**

I. INTRODUCTION

Integrated LC voltage-controlled oscillators (VCOs) are standard modules in radio frequency transceivers. These modules are used to up-convert signals typically for transmitter applications, and also down-convert signals, mostly in receivers. VCOs are widely used as sinusoidal signal generating blocks in a phase locked loop (PLL) based frequency synthesizer for wireless or optical communicaton applications. Due to increasing demands for higher data rates, very stringent specifications are necessary for VCO spectral purity. At the same time, a great number of VCOs are used in battery operated mobile systems, that require power conservation. There is usually a trade-off between VCO spectral purity (measured by phase noise) and its DC power consumption. Other VCO specifications are the center frequency of oscillation, tuning range, and tuning sensitivity (VCO gain). All these parameters need to be optimized for a given application. This paper will describe an very low power CMOS LC VCO with relatively good spectral purity suitable for extremely low-power mobile communication devices.

II. TANK DESIGN

To achieve low-power consumption and low-phase noise performance in an LC VCO, it is essential to design and optimize the tank with minimal combined inductance and capacitance loss (R), leading to maximum L/R and L/C ratios [1]. We have used a commericial 2.5D electromagnetic simulator (SONNET) to design the optimum inductor, while the varactor is designed using S-parameter simulation in CADENCE design environment.

A. Inductor

The key parameters for good phase noise performance of LC VCOs are the quality factors of on-chip inductors and capacitors (or varactors) in the LC tank. At lower frequencies (~ 1 GHz for a few nano henries inductor), reduction of series resistance of an inductor has the largest impact on inductor Q. Series resistance can be decreased by either using a thick metal (4 ~ 10 µm) or dual parallel metal. At higher frequencies, Q is dominated by substrate effects. Therefore, reducing the substrate loss through increasing the thickness of the dielectric layer underneath the inductor or through increasing the substrate resistance will maximize the Q at high frequencies (> 2 GHz for a few nano henries spiral inductor) [2].

In this work we have used single layer inductors in a standard low-cost CMOS process with 2 µm thick Al metal to reduce fabrication cost. The inductor uses an opening in the pwell underneath the spiral design to increase the resistivity of the substrate underneath the spiral inductor, resulting in a decrease in substrate loss and an increase in the inductor quality factor [3]. Octagonal-shaped inductors are often used in LC VCO since they have slightly higher quality factor compared to square spirals for the same inductance value. To suppress phase noise of the oscillators, it is important to design a completely symmetrical layout. Therefore, two identical octagonal inductors are designed and optimized in SONNET. Fig. 1 shows the SONNET simulation results of optimized dual inductors including connecting metals. Over the frequency range of 1.8 to 2 GHz, an inductance value is 6.2 nH and a quality factor is 7.5. Self-resonant frequency is about 7.5 GHz.

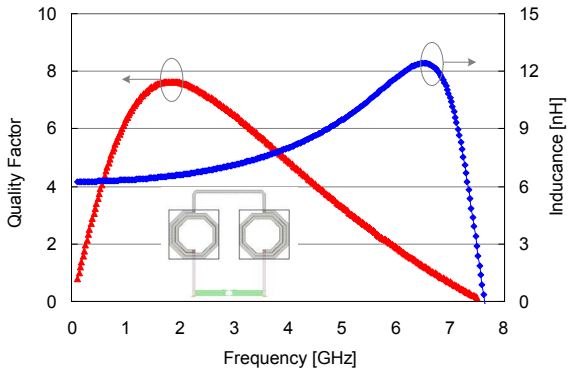
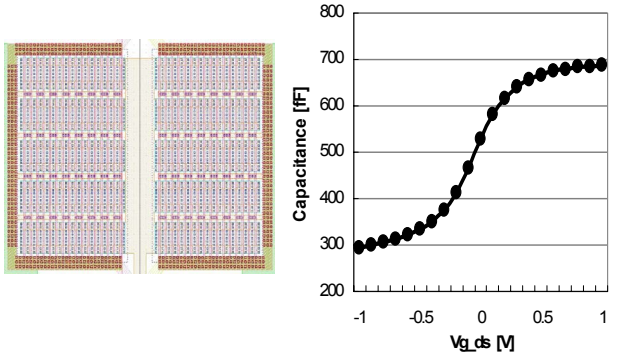


Fig. 1. Quality factor and inductance of equivalent inductor in LC tank by 2.5D EM simulation tool of SONNET. Inset: Layout of dual inductors.

B. Varactor

The tuning range of MOS varactor VCOs is determined by the C_{v_max}/C_{v_min} of the accumulation- or inversion-type NMOS varactors. In a scaled CMOS technology, the tuning range of MOS varactor VCOs can be widened compared to diode varactor VCOs, since an increase of field oxide capacitance enables an increase of the ratio of C_{v_max} to C_{v_min}. MOS varactor VCOs have low power consumption, high quality factor, and low phase noise at large offset frequencies from the carrier due to small MOS varactor parasitic resistance. The disadvantages of MOS varactors are the steep capacitance variation with tuning voltage and reduced linear portion of the tuning characteristics [4]. In this work, we have used standard NMOS varactors instead of diode varactors, leading to a good phase noise with a moderate tuning range.

Fig. 2 (a) is the layout of NMOS varactors drawn in a comb-like fashion. Varactors are made as an array of 16 x 5 unit transistors. The width of the unit transistor is 4μm to keep the gate resistance low, while the length of the unit transistor is 0.18 μm (minimum) to achieve high Q. Fig. 2 (b) is the varactor capacitance at 2 GHz derived from S-Parameter simulations as a function of tuning voltage between gate and source/drain. With a bias voltage between gate and source/drain varying from -1 V to 1 V, the quality factor of NMOS varactor is maintained to be more than 10 over the frequency range of operation up to 3 GHz, leading to good phase noise performance of VCO. The gate terminals of varactors are connected to the oscillation nodes so that the n-well to substrate capacitance appears as common-mode and does not load the tank.



(a) (b)

Fig. 2. (a) Layout of NMOS varactors as an array of 16 x 5 unit transistors, with the width of 4 μm and the length of 0.18 μm. (b) Varactor capacitance versus tunning voltage between gate and source/drain using S-parameter simulation at 2 GHz.

III. Circuit Design

The circuit schematic of the proposed LC VCO is shown in Fig. 3. The topology of proposed VCO is based on complementary NMOS and PMOS cross-coupled differential LC structure (NP-pair) with NMOS tail current source. This structure, once optimized, performs better than other common VCO topologies, in terms of the phase noise value and the overall power consumption under low power levels.

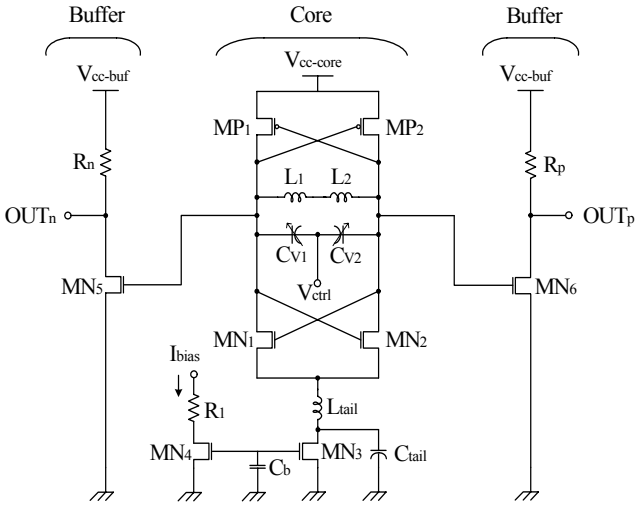


Fig. 3. Circuit schematic of the proposed LC VCO.

The tank amplitude of an NP-pair topology is twice that of an N-pair or a P-pair only topology for a given current. The circuit can be optimized to have more symmetry in the output waveform, which leads further phase noise reduction. The transconductances of the NMOS and PMOS switching devices have been set approximately equal to obtain symmetry in the output waveforms [5]. Asymmetry of the output waveforms is the cause of the additional up-conversion noise. However, with increasing tail-current from a low power supply voltage the NP-pair goes into the voltage-limited region quickly due to reduced voltage headroom. So, if power dissipation is not a concern, N-pair or P-pair only topology can be used for better phase noise performance.

The values of the on-chip inductors, varactors and the sizes of cross-coupled NMOS and PMOS FET pairs are chosen in accordance to the oscillation condition and frequency tuning range. In particular, the inductance was increased as large as possible for low power consumption while maintaining a suitable frequency tuning range. The oscillation frequency of the VCO is given by

$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_{Tank} \cdot C_{Tank}}} \qquad (1)$$

where

$$L_{Tank} = L_1 + L_2 \qquad (2)$$

and

$$\begin{aligned} C_{Tank} = {} & C_{v1} + C_{v2} + \left(C_{gdp1} + C_{gdp2} + C_{gsp1} \middle\| C_{sdp2}\right) \\ & + \left(C_{gdn1} + C_{gdn2} + C_{gsn1} \middle\| C_{sdn2}\right) \\ & + \left(C_{gdn5} + C_{gsn5} + C_{gdn6} + C_{gsn6}\right) \end{aligned} \qquad (3)$$

where f_{osc} is the oscillation frequency, L_{Tank} and C_{Tank} are the inductance and the capacitance of LC tank respectively, C_{v1} and C_{v2} are the capacitance of varactors, C_{gdp1}, C_{gdp2}, C_{gsp1}, and C_{gsp2} are the gate to drain/source capacitance of PMOS pair, C_{gdn1}, C_{gdn2}, C_{gsn1}, and C_{gsn2} are the gate to drain/source capacitance of NMOS pair, and C_{gsn5}, C_{gsn6}, C_{gdn5}, and C_{gdn6} are the gate to drain/source capacitance of NMOS in the output buffer.

The inductor L_{tail} is used to boost the impedance at NMOS common-source node, avoiding Q-degradation by the triode region MOSFETs in the stacked NP-pair without raising the required supply voltage to maintain the voltage headroom. A filtering capacitor C_{tail} is used at the drain of MN_3 to filter out the noise at $2f_{osc}$. The sizes of the tail current source as well as the mirror are made large with moderate W/L so that the flicker-noise up-conversion is minimized without degrading thermal noise. Output buffer is designed as a common source NMOS with 50 Ω resistor load to obtain 50Ω matching.

IV. Layout Issues

The RF LC VCO was fabricated in IBM 7RF 0.18 µm CMOS technology. Fig. 4 shows the microphotograph of the VCO chip including the test pads with a die area of 1 mm x 0.9 mm. Careful consideration has been given to a fully symmetrical layout to minimize the even-order distortion in the differential output waveform and noise up-conversion. The active devices and the NMOS varctors have been laid out as compactly as possible with a shared source/drain to minimize the parasitic capacitance. In order to reduce the substrate noise in the low-resistivity substrate, senstive and noisy circuit parts have been surrounded by guard-rings.

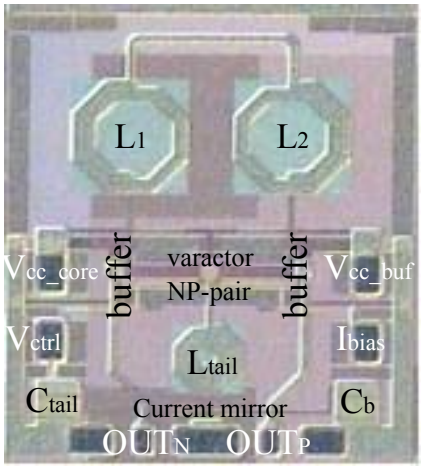


Fig. 4. Die microphotograph of the VCO.

V. Measurement Results

The measurements were made on-wafer using 50 Ω coplanar probes. The DC power consumption of the VCO core is 0.5 mW under 0.9 V supply voltage. Fig. 5 shows the measured phase noise spectrum of the VCO for a center frequqncy of 1.87 GHz. Phase noise @ 1 MHz offset from the carrier is -111 dBc/Hz. The measured output signal power is -17 dBm with at single ended buffer output terminated at 50 Ω. Fig. 6 shows the measured spectrum of the VCO at 1.87 GHz. The measured tuning characteristic of the VCO is shown in Fig. 7. The measured tuning range of 1.86 GHz ~ 2.01 GHz, for control voltage from 0 to 1.4 V, lies between simulation result and layout parasitic extraction (LPE) simulation result. The tuning sensitivity is 93 MHz/V. The tuning range can be extended for wideband applicaions using switched capacitors bank and adaptive frequency calibriation (AFC) tecinques [6-8].

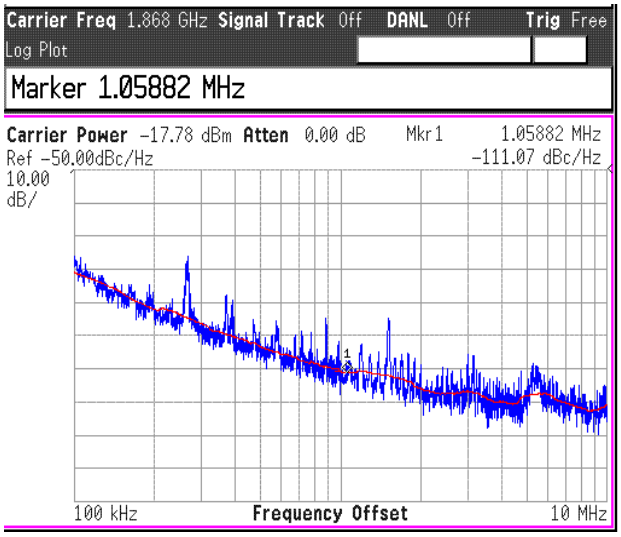


Fig. 5. Measured phase noise of the VCO at 1.87 GHz.

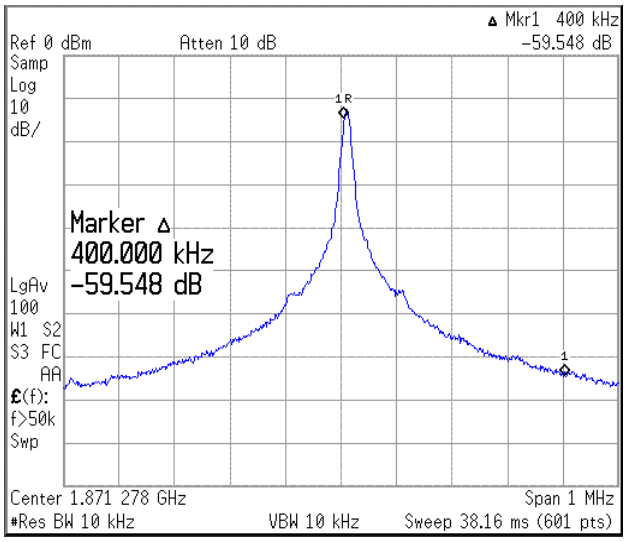


Fig. 6. Measured spectrum of the VCO at 1.87 GHz.

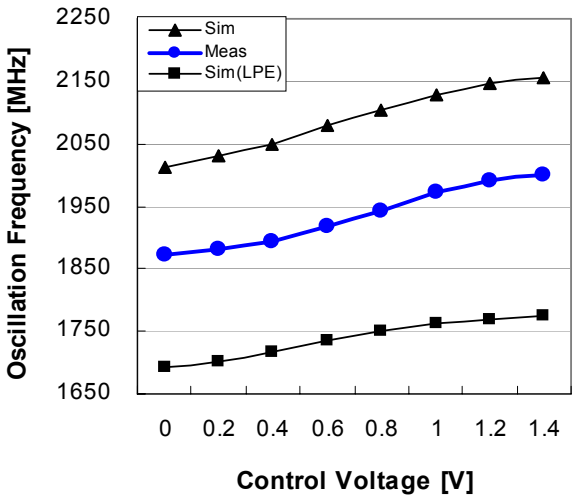


Fig. 7. Measured tuning characteritic of the VCO.

The overall performance of the VCO can be evaulated by a common figure of merit (FOM) which is given by [9]

$$FOM = L\{f_{offset}\} + 10\log\left[\left(\frac{f_{offset}}{f_{osc}}\right)^2\left(\frac{P_{DC}}{1mW}\right)\right] \quad (4)$$

where $L\{f_{offet}\}$ is the phase noise at a certain offset frequency (f_{offet}), f_{osc} is the oscillation frequency, and P_{DC} is the DC power dissipation. The calculated FOM is -180 dBc/Hz. Fig. 8. shows the results of the FOM and DC power consumpton in order to compare the VCO performance with the previously published VCOs. The summary of the VCO characteristics is shown in Table I.

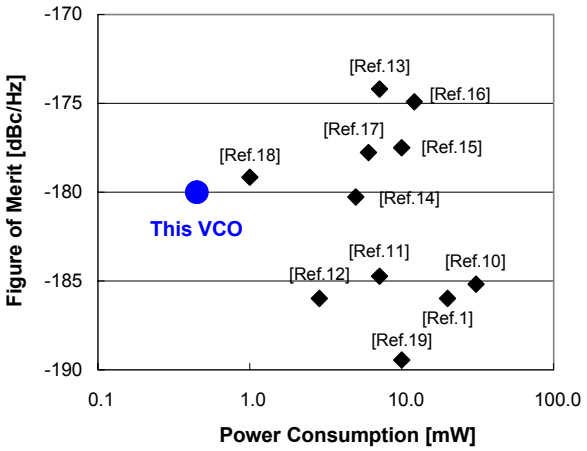


Fig. 8. Comparison results of figure of merit and DC power consumpton with previous VCOs.

Table I. Summary of VCO performances.

Technology	CMOS 0.18 μm
Supply voltage	0.9 V
Power consumption	0.5 mW
Tuning range	1.86 GHz ~ 2.01 GHz
Tuning sensitivity	93 MHz/V
Phase noise @ 1MHz offset	-111 dBc/Hz
Figure of merit	-180 dBc/Hz
Test chip area with probe pads	1 mm x 0.9 mm

VI. Conclusion

An extremely low power and low phase noise fully integrated CMOS differential LC VCO in a commercial 0.18 μm CMOS process has been presented. The VCO core consumes only 0.5 mW of power under 0.9 V supply and achieves -111 dBc/Hz phase noise at 1 MHz offset frequency. The figure of merit is -180 dBc/Hz.

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