A Low Phase Noise 10 GHz VCO in 0.18μm CMOS Process

Tae-young Choi[1], Hanil Lee[2], Linda P.B. Katehi[2], Saeed Mohammadi[2]

[1]University of Michigan at Ann Arbor, Dept. of Electrical Engineering and Computer Science,
1301 Beal Ave. Ann Arbor, MI, 48109, USA
[2] Purdue University, School of Electrical and Computer Engineering,
465 Northwestern Ave. West Lafayette, IN, 47907, USA, 1-765-494-3557

***Abstract* — A fully integrated 10 GHz LC voltage controlled oscillator is presented. The VCO is implemented in 6 metal 0.18μm CMOS process. The VCO achieves a wide tuning range of 20.1% (10.20 GHz to 12.48 GHz), and provides an output power of –3 dBm, while drawing 22.7mA from 2.2V power supply. The measured phase noise is –125.33 dBc/Hz at 1 MHz offset from the carrier at 10.3GHz. The VCO figure of merit is a record low –188 dBc/Hz.**

I. Introduction

The fast expansion of the telecommunication market and the demand for high data-rate transmission has brought about intensive research in high frequency transceiver. The primary challenge is in the design of the front-end which down-converts the high frequency signal to the base band for further data recovery and processing. Implementation of the front end in CMOS is attractive due to low cost and possibility of integration with base band circuits. The feasibility of high frequency front-end in CMOS has been enabled by the aggressive down scaling of CMOS technology, and efforts are being made to improve the performance of the basic building blocks of the front end.

In this paper, a 10-12GHz complementary LC VCO with a wide tuning range and low phase noise is presented. This VCO can be used in a high frequency system applications where stringent requirements on signal spectrum purity are specified.

II. Circuit Design

A. Topology

The schematic of the VCO is depicted in Fig. 1. A complementary cross-coupled differential structure is used to achieve higher transconductance for a given current, thus resulting in faster switching. The differential structure provides a symmetric output wave-form [1].

An NMOS current source transistor is placed below the cross coupled NMOS pair to control the bias current of the VCO core. The output of the VCO core is directly connected to the input of the buffer, which drives 50Ω impedances. To avoid the large process variation of load resistors, PMOS transistors are used as the loads of the buffer, biased by high resistance resistors.

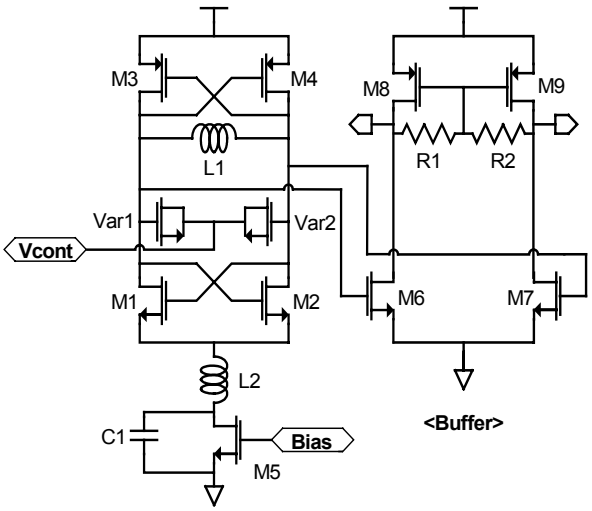

Fig. 1. VCO Schematic.

An inductor (L_2) between the NMOS pair and current source and a capacitor (C_1) in parallel with the current source eliminate the noise around the second harmonic, which results in reduced phase noise. [2]

The oscillation frequency is given by

$$f_o = \frac{1}{2\pi\sqrt{L\ (C_d + C_p + C_v)}} \qquad (1)$$

where f_o is the oscillation frequency, L is the inductance of the inductor, C_d is the parasitic capacitances of transistors and varactors, C_p is the parasitic capacitance due to interconnection, and C_v is the capacitance of varactors seen at the oscillation nodes.

To achieve a wide tuning range, C_d and C_p should be minimized. C_d can be reduced by using small size devices but is limited by the minimum size of devices for sustaining the oscillation. C_p can be reduced by careful layout which minimizes interconnection metals.

B. Inductor

To increase the self resonance frequency, a horse-shoe type one-turn inductor is used in a LC tank. This structure also provides symmetry to the two output nodes

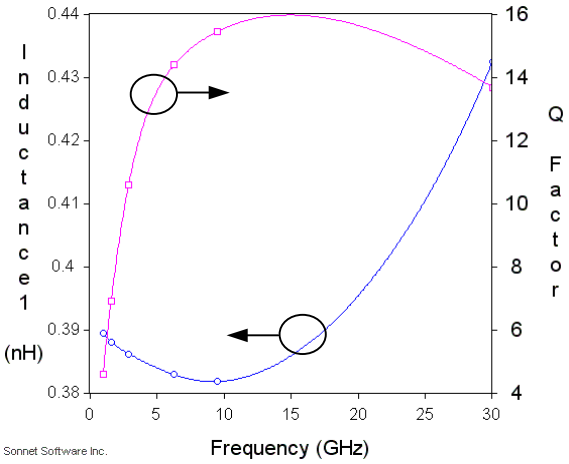

Fig. 2. Simulated inductance and Quality factor of inductor

of the VCO core. The inductor is simulated with Sonnet, an EM simulation software. The expected inductance and the quality factor Q at 10 GHz are 0.38 nH and 15, respecttively as shown in Fig. 2.

C. Varactor

Besides the inductor of the tank, the varactor is also a key element in determining the performance of the VCO. In the technology used in this work, for small horse-shoe type inductors operating in X-band, the Q of the inductor increases as the frequency increases. On the other hand, the Q of the varactor decreases in the same frequency. So, there is an optimum value for the inductance and capacitance of the varactor in the tank circuit to achieve maximum tank quality factor. In our configuration, two NMOS varactors are used in the tank for tuning purpose. The gate length of the varactor is kept at a minimum to maintain small capacitance and high Q at high frequency. The simulated capacitance of the varactor model is shown in Fig. 3

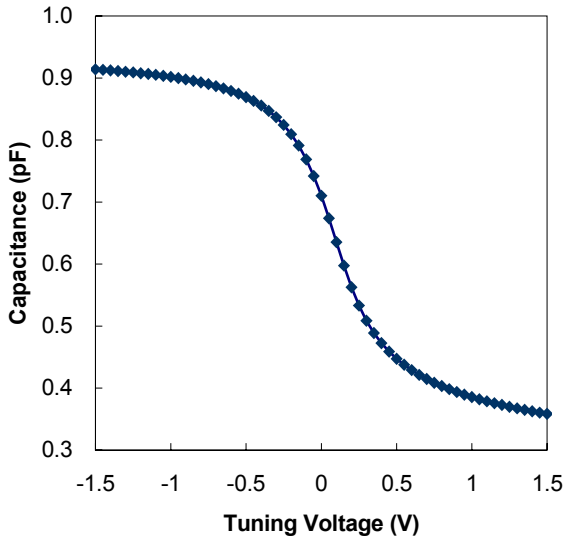

Fig. 3. Simulated Capacitance of Varactor

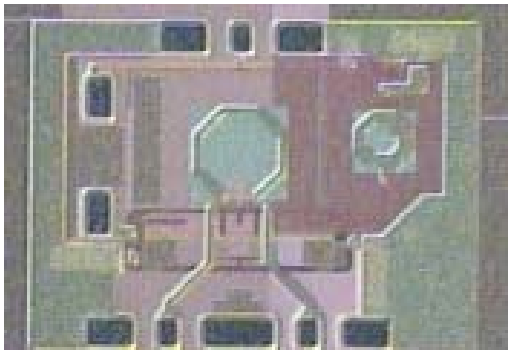

Fig. 4. Photograph of the fabricated LC VCO.

III. Measurement Results

The VCO is fabricated in IBM 7RF 0.18 µm CMOS process. The chip photograph is shown in Fig. 4. The VCO occupies an area of 950×700µm^2 including the output pads.

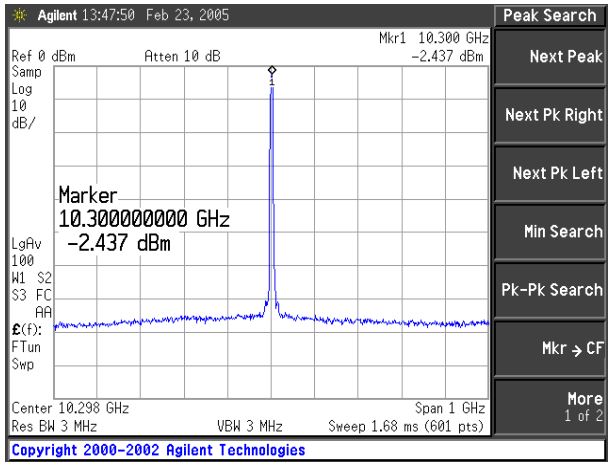

Fig. 5. Output spectrum of the VCO at 10.3GHz

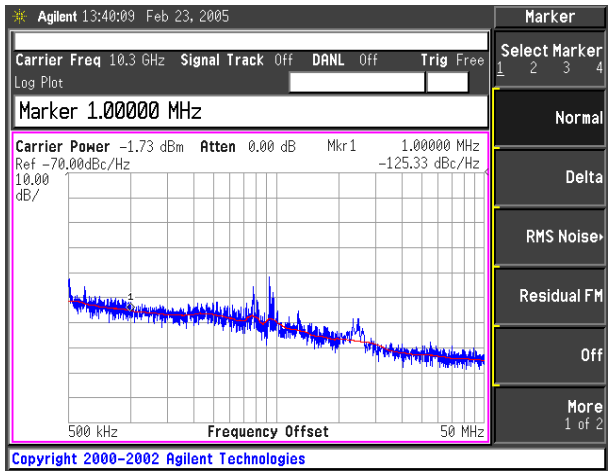

Fig. 6. Phase Noise of the VCO at carrier frequency of 10.3GHz

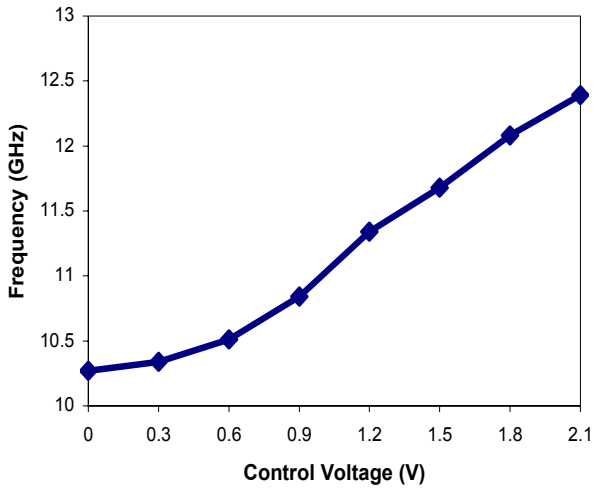

Fig. 7. Tuning Range of the VCO. The gain of the VCO is approximately 1 GHz/V.

An Agilent E4448A spectrum analyzer with phase noise measurement option is used to measure the output frequency, power and phase noise. A Cascade Infinity differential probe and a 180 degree hybrid coupler are used to convert the differential output signal of the VCO to the single ended input to the spectrum analyzer.

The VCO core and the buffer draw 11mA and 11.7mA, respectively, from 2.2V power supply, which corresponds to the total power consumption of 50mW.

Fig. 5. and Fig. 6. show the output spectrum and phase noise of the VCO. At 1MHz offset from the carrier frequency at 10.3GHz, the measured phase noise is –125.3 dBc/Hz.

The figure of merit for a VCO (FOM) can be calculated using [3]

$$FOM = PN(f_{offset}) - 20\log\left(\frac{f_o}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (2)$$

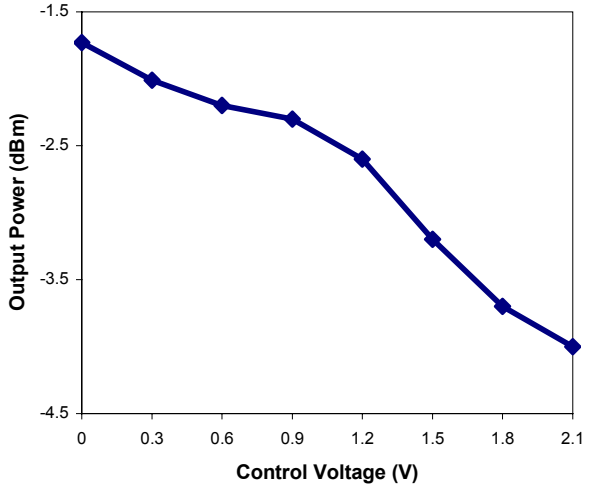

Fig. 8. Output power of the VCO. The output power of VCO is higher than –4 dBm over the entire tuning range.

where f_{offset} is the frequency offset, f_o is the oscillation frequency, $PN(f_{offset})$ is the phase noise at the f_{offset}, and P_{DC} is the DC power consumption. With the measured specification of the VCO, the figure of merit of –188.3 dBc/Hz is achieved. When the buffer power is excluded FOM of –191.7 dBc/Hz can be achieved.

A tuning range of 20.1% from 10.2GHz to 12.48GHz is achieved for the VCO as shown in Fig. 7. The approximate VCO gain is estimated at 1GHz/V.

Fig. 8 shows the output power of the VCO as the control voltage is varied (Frequency tuning). The output power is between –1.7 and –4.3 dBm over the entire tuning range.

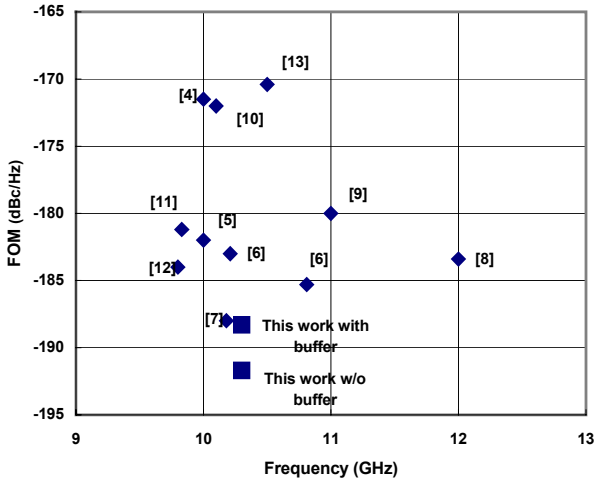

Fig. 9. Comparison of the Figure of Merit for the VCO presented in this work and those reported in the literature.

We have compared the FOM achieved for the VCO presented in this work with those reported in literature. The comparison is shown in Fig. 9. Our VCO achieves the lowest FOM when the buffer is considered as well as when the power consumption of the buffer is not included. The performance of the VCO is summarized in Table 1.

TABLE I.

SUMMARY OF VCO PERFORMANCES

Power supply	2.2 V
Power consumption	50 mW
Tuning range	10.2 GHz ~ 12.48 GHz
Phase noise @ 1MHz offset	-125.33 dBc/Hz
Figure of merit	-188 dBc/Hz
Chip area	0.67 mm^2
Technology	0.18 μm CMOS

IV. CONCLUSION

A complementary LC VCO which operates between 10 and 12 GHz has been designed and fabricated in a CMOS 0.18μm technology and has been measured for its

performance. The VCO core and buffer provides a wide tuning range and low phase noise while consuming 50mW. The calculated figure of merit for the VCO is the lowest reported in the literature.

ACKNOWLEDGEMENT

The authors are grateful for the funding provided by Semiconductor Research Corporation under Task 1114.001 and DARPA Technology for Efficient and Agile Microsystems (TEAM) under project DAAB07-02-1-L430. The authors wish to acknowledge the support of Dr. Mark Johnson at School of Electrical and Computer Engineering, Purdue University. Tae-young Choi is grateful to Purdue University for supporting his research.

REFERENCES

[1] A. Hajimiri, and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid State Circuits*, vol. 34, issue 5, May 1999, pp. 717-724.

[2] E. Hegaji, H. Sjoland, and A. Abidi, "A filtering technique to lower oscillator phase noise," in *Dig. of Tech. Papers of International Solid State Circuits Conference*, February 2001, pp. 364-365.

[3] J.-O. Plouchart, H. Ainspan, M. Soyuer, and A. Ruehli, "A fully-monolithic SiGe differential voltage-controlled oscillator for 5 GHz wireless applications," *IEEE Radio Frequency Integrated Circuits Symposium*, June 2000, pp. 57-60.

[4] A. H. Mostafa, and M. N. El-Gamal, "A CMOS VCO architecture suitable for sub-1 volt high-frequency (8.7-10 GHz) RF applications," *International Symposium on Low Power Electronics and Design*, August 2001, pp. 247-250.

[5] L. Perraud, J.-L. Bonnot, N. Sornin, and C. Pinatel, "Fully integrated 10GHz CMOS VCO for multi-band WLAN applications" *European Solid State Circuits Conference*, September 2003, pp. 353-356.

[6] S. Ko, H.D. Lee, D.-W. Kang, and S. Hong, "An X-band CMOS quadrature balanced VCO," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, June 2004, pp. 2003-2006.

[7] S. Ko, J.-G. Kim, T. Song, E. Yoon, and S. Hong, "20GHz integrated CMOS frequency sources with a quadrature VCO using transformers," *IEEE Radio Frequency Integrated Circuits Symposium*, June 2004, pp. 269-272.

[8] T.K.K.Tsang, and M.N. El-Gamal, "A high figure of merit and area-efficient low-voltage (0.7-1V) 12GHz CMOS VCO," *IEEE Radio Frequency Integrated Circuits Symposium*, June 2003, pp. 89-92.

[9] M. Tiebout, "Physical scaling of integrated inductor layout and model and its application to WLAN VCO design at 11GHz and 17GHz," in *Proceedings of the 2003 International Symposium on Circuits and Systems*, vol. 1. May 2003, pp. I637-I640.

[10] M.A. Do, R. Zhao, K. S. Yeo, and J.-G. Ma, "Fully integrated 10GHz CMOS VCO," *Electonics Letters,* vol. 37, issue 16, August 2001, pp. 1021-1023.

[11] L. Jia, J.-G. Ma, K. S. Yeo, and M.A. Do, "9.3-10.4-GHz-band cross-coupled complementary oscillator with low phase-noise performance," *IEEE Transaction on Microwave Theory and Techniques,* vol. 52, issue 4, April 2004, pp. 1273-1278.

[12] H. Wang, "A 9.8 GHz back-gated tuned VCO in 0.35 μm CMOS," in *Dig. of Tech. Papers of International Solid State Circuits Conference*, February 1999, pp. 406-407.

[13] A. H. Mostafa, M. N. El-Gamal, and R.A. Rafla, "CMOS 5-10GHz oscillators for low voltage RF applications," in *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, vol. 1, August 2000, pp. 478-481.