High Performance Micro-Machined Inductors on CMOS Substrate

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Abstract – **Using a combination of micromachining and three-dimensional (3-D) processing technologies, we have designed, fabricated, and tested inductors on CMOS grade Si substrate (10~20 Ω·cm resistivity) which exhibit very high quality factor and high resonant frequency. A 1.2 nH inductor in this process achieves a record high quality factor of ~140 at 12GHz, with Q > 100 for frequencies between 8 to 20GHz. The technology to fabricate these inductors is based on one step deposition and electroplating of a stressed layered metal combination of Cr and Au and is fully compatible with CMOS technology.**

Index Terms – **high quality factor, high frequency, CMOS compatible, three dimensional, stressed metal, micromachining, integrated inductor.**

I. INTRODUCTION

The requirement for high performance passive elements is the most stringent in designing state-of-the-art radio frequency integrated circuits (RFICs). High-Q inductors play a very important role in the performance achieved by RFICs such as voltage controlled oscillators (VCOs), low-noise amplifiers (LNAs), filters, mixers, and power amplifiers (PAs) [1]-[4]. By the advent of deep submicron CMOS and SiGe heterojunction bipolar technologies, the operating frequency of Si-based RFICs has been increasing up to W-band frequency range. While at very high frequencies (>30GHz), transmission line sections are the inductive elements of choice because they exhibit reasonably high quality factors [5], at lower frequencies (< 20GHz) lumped element inductors are preferred because of their relatively small dimensions.

The quality factor and resonant frequency of integrated spiral inductors on a CMOS substrate are usually very low, because of substrate losses and ohmic losses due to the finite thickness of inductor metals. Several papers have reported unconventional on-chip inductors integrated with RF circuits, such as voltage controlled oscillators (VCOs) [6],[7] and power amplifier (PA) [8]. There have been reports on suspended spiral inductors [9]-[11] and vertical spiral inductors [12], all of them limited to modest quality factors and relatively low self-resonance frequencies. Recently, spiral inductors with a quality factor above 100 and self resonant frequency above 50GHz have been demonstrated. These inductors were suspended over a low loss ceramic substrate and had a copper metal thickness above 50μm [13].

We have previously reported a novel micromachined technology developed specifically for the design and fabrication of high performance 3-D inductors [14]. In that demonstration, a 1nH inductor was fabricated on high resistivity Si substrate (>10k Ω·cm) and exhibited a quality factor of Q > 60 at frequencies from 3 GHz to 7 GHz. In the work presented herein, we are reporting a variety of micro-machined high-Q and high frequency 3-D inductors fabricated on low resistivity Si substrates (10~20 Ω·cm) using a stressed metal technology. A combination of backside dry and wet etching has been utilized to improve the performance of these inductors by removing the substrate material and thus reducing the substrate parasitics. A 1.2nH inductor using this technology achieves a self-resonant frequency, f_{sr} > 40GHz and a quality factor, Q > 100 at frequencies from 8GHz to 20 GHz. To our knowledge these are the highest reported quality factors and self-resonance frequencies for inductors fabricated on CMOS grade substrate.

II. TECHNOLOGY

The inductors presented herein are based on a recently developed stressed metal technology [14] in which a Cr/Au metal layered-combination is deposited to create a metal with a built-in stress.

This built-in stress is used to create a spiral inductor printed on a thin dielectric membrane. The CMOS substrate underneath the inductor is removed by using a combination of dry and wet etching. This post-CMOS fabrication method results in three-dimensional inductors with excellent high-frequency performance. This technology has allowed us to use CMOS grade substrate to achieve record high performance inductors.

Fig. 1 shows the process sequence that is followed to fabricate the demonstrated micro-machined inductors. First, the oxidized Si substrate is etched by DRIE from the backside of the areas underneath the inductors to achieve a thinned Si substrate with a thickness of less than 100 μm (Fig. 1(a)). Then, the three dimensional inductors are fabricated (Fig. 1(b) and (c)) on these areas using the previously reported stressed metal technology [14]. A Au electroplating step is then performed to improve the metal contact resistance and also the rigidity of the structure. Fig. 2 shows the fabricated one-turn and two-turn inductors at this stage. Finally, the remained Si substrate was etched from the back using TMAH (Fig. 1(d)). The 3-D inductors on a 0.85 μm SiO_2 diaphragm after TMAH etch are shown in Fig. 3. With the lossy Si substrate underneath the inductors replaced by a thin SiO_2 diaphragm, the inductors show a high quality factor and high self-resonant frequency.

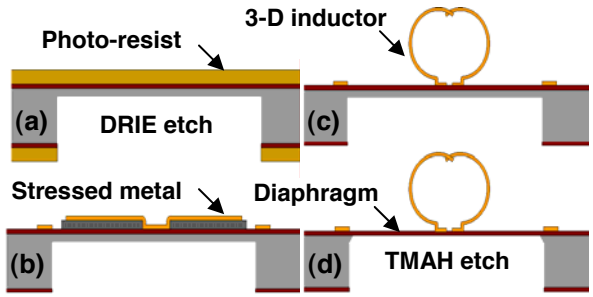

Fig. 1. Schematic cross-sectional views of the fabrication process flow for 3-D inductor on SiO_2 diaphragm.

To investigate the effects of the substrate and resulting loss and parasitic capacitances on the performance of the inductors, we have fabricated and characterized inductors with one and two turns and metal line widths of 25 μm, 35 μm, and 45 μm before and after substrate etch. In addition, to assess the impact of the substrate loss we compared the performance of inductors fabricated on low and high resistivity substrates.

III. RF CHARACTERIZATION

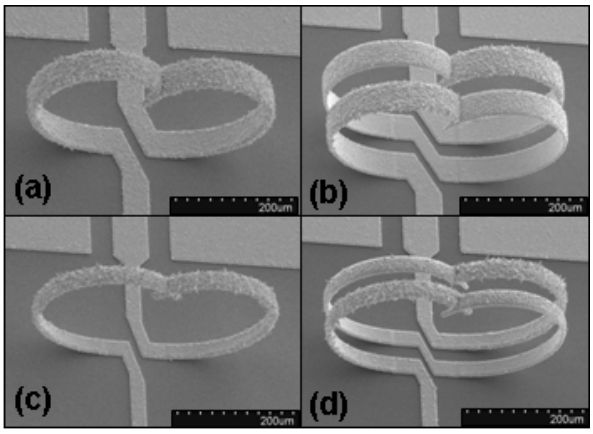

Fig. 2. SEM microphotographs of 3-D inductors fabricated on partially thinned Si substrate (a) 1 turn and 45 μm width (b) 2 turn and 45 μm width (c) 1 turn and 25 μm width (d) 2 turn and 25 μm width.

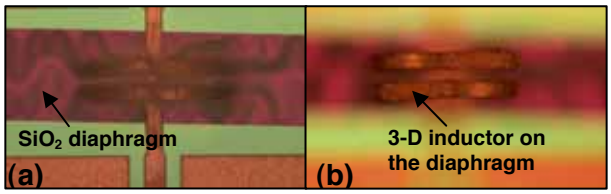

Fig. 3. Microscope images of 3-D inductor (2 turn and 45 μm width) fabricated on SiO_2 diaphragm (a) focused on the diaphragm (b) focused on the inductor.

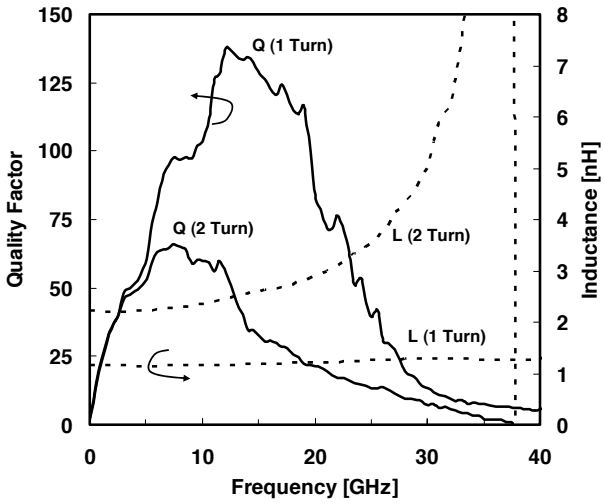

Fig. 4. Measured quality factor and inductance value of 1-turn and 2-turn inductors fabricated with 45 μm width on SiO_2 diaphragm.

The S-parameters of the fabricated inductors were measured using the Agilent 8722 network analyzer. To perform accurate quality factor measurements when the values are very high, a very thorough calibration and accurate de-embedding of pads parasitics is needed [16]. Herein, several inductors of the same geometry were measured to ensure repeatability in the measurements. The deviation of the measurement values was within 3%. Fig. 4 shows the measured quality factor, Q, and inductance, L, extracted from the measured S-parameters for one-turn and two-turn inductors fabricated using the presented technology. As can be seen from this figure, for one-turn inductor, a peak Q of 138 is achieved at 12GHz. The self-resonant frequency of the inductor is over 40GHz. For the two-turn inductor, a maximum Q of 66 and self-resonant frequency of 38 GHz are achieved.

# of Turns	Width [μm]	L [nH]	Quality Factor	SRF [GHz]
1	25	1.23	38.2@7.0GHz	>40
1	35	1.22	51.6@7.5GHz	>40
1	45	1.16	137.5@12GHz	>40
2	25	2.60	30.5@3.0GHz	33
2	35	2.45	32.8@3.5GHz	35
2	45	2.20	66.1@7.5GHz	38

Table 1. Extracted parameters of 3-D inductors calculated from S-parameters measurement. Inductors in this table have 20μm gap between the fingers and 350μm diameter and 4.0μm electroplated Au thickness.

Fig. 5 shows the quality factor, Q, and inductance, L, extracted from the measured S-parameters for one-turn and two-turn inductors fabricated on a 0.85μm SiO_2 diaphragm with different widths of the spiral turns. As shown in the figure, the inductor with 45μm width has a higher quality factor and self-resonant frequency than the inductor with 25μm finger width. Table 1 summarizes the performance of several inductors fabricated using the presented this technology. The data is extracted from the S-parameter measurement.

The following conclusions have been derived from the measured data were:

- The inductance value increases with the number of turns in a perfectly quadratic manner. This is due to the high mutual inductance in the two-turn inductors.
- Increasing the width of the conductor increases the quality factor significantly while it changes the self-resonant frequency only marginally.

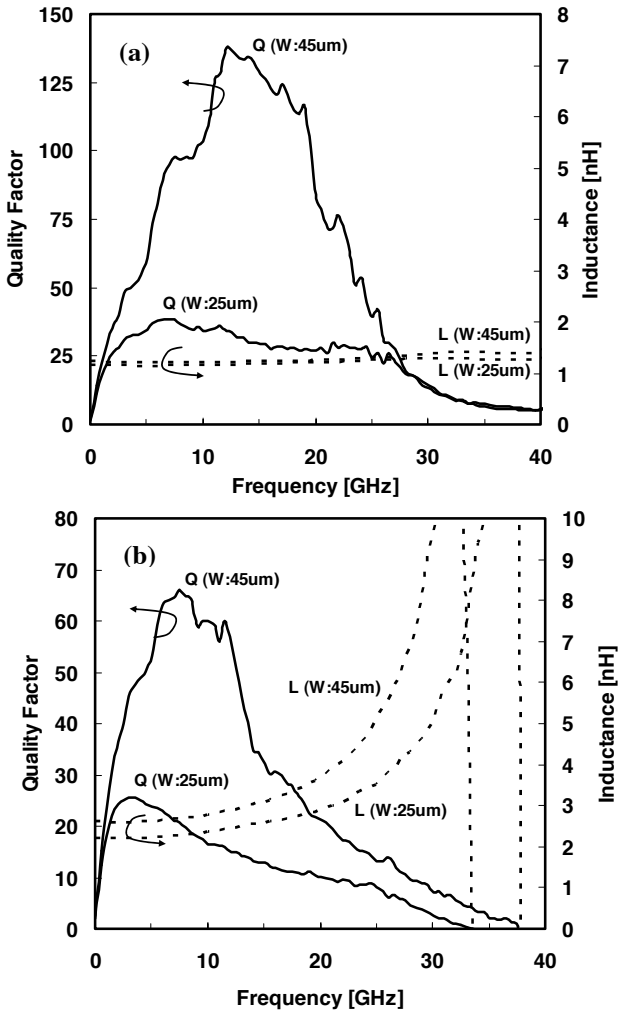

Fig. 5. Measured quality factor and inductance value of (a) 1-turn inductors (b) 2-turn inductors with different finger widths on SiO_2 diaphragm.

To investigate the effect of the Si substrate on the inductor performance, we have also measured the RF performance of two-turn inductors in terms of the quality factor, Q, and inductance, L, as functions of frequency. The Q and L values were extracted from the measured S-parameters. The inductor had a metal width of 45 μm and was fabricated on a low-resistivity Si substrate (10~20 Ω·cm), high-resistivity Si substrate (>10k Ω·cm) [14], and a 0.85 μm SiO_2 diaphragm. As expected, the inductors printed on the diaphragm have the

highest quality factor and self-resonant frequency as compared to those fabricated on the low and high resistivity substrates.

The following conclusions were deducted from the measurements:

- The quality factor increases with the resistivity of the substrate.
- Eliminating the substrate drastically increases quality factor of the inductor.
- High-Q and high frequency inductors can be fabricated with CMOS substrate using a post CMOS micromachining process.

IV. CONCLUSION

Various three-dimensional inductors were fabricated on a low resistivity silicon substrate using a post-CMOS stressed metal technology [14]. These inductors exhibited a very high self resonant frequency and a very high quality factor compared to their printed spiral counterparts. Quality factors above 100 were measured at frequencies up to 20GHz. The availability of high-Q and high self-resonant inductors on CMOS technology will open up new design directions for RF and microwave integrated circuits.

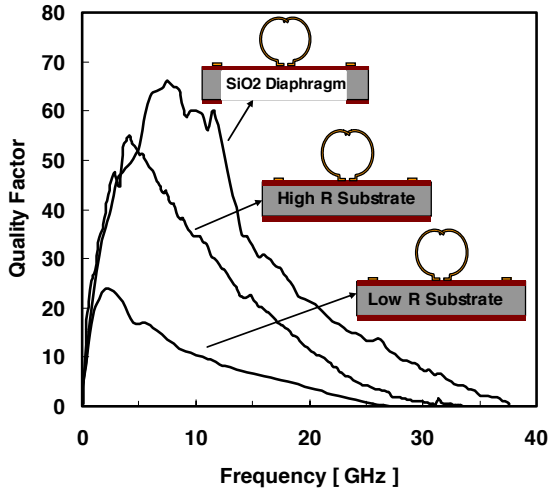

Fig. 6. Measured data of quality factor and inductance of 2-turn inductor fabricated on low resistivity Si substrate, on high resistivity Si substrate and on SiO_2 diaphragm.

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