High Yield Reduced Process Tolerance Self-Aligned Double Mesa Process Technology for SiGe Power HBTs

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***Abstract*— Two novel high yield reduced process tolerance process technologies were developed for double mesa SiGe power HBT. DC and RF results from both 10 and 20 finger devices were presented. A reduced tolerance process is essential in the further development of MMICs using these transistors.**

***Index Terms*— HBT, MMIC, SiGe, transistors**

I. Introduction

This work describes the development of two novel fully self-aligned process technologies that improves yield due to improved process tolerance. The work is necessary for the further development of Silicon Germanium (SiGe) Monolithic Microwave Integrated Circuit (MMIC) with multiple active devices.

II. Design and Fabrication

The design and development of a high performance n-p-n Si/SiGe/Si Heterojunction Bipolar Transistor (HBT) begins with the device heterostructure design and lateral layout. The factors to consider for optimization of the heterostructure and layout while taking into account the requirements for high power handling capability, good thermal stability, and high frequency operation have been described in [1]. The heterostructure for this work was grown in one-step using Chemical Vapour Deposition (CVD) with the design shown in Table I. The measured Secondary Ion Mass Spectroscopy (SIMS) profile of the device is shown in Fig. 1.

TABLE I
Si/SiGe/Si HBT heterostructure.

Emitter cap	Si	n+	P	$2 \times 10^{19}cm^{-3}$	2000Å
Emitter	Si	n	P	$1 \times 10^{18}cm^{-3}$	1000Å
Spacer	$Si_{0.75}Ge_{0.25}$	i			50Å
Base	$Si_{0.75}Ge_{0.25}$	p+	B	$1 \times 10^{20}cm^{-3}$	200Å
Spacer	$Si_{0.75}Ge_{0.25}$	i			50Å
Collector	Si	n-	P	$1 \times 10^{16}cm^{-3}$	5000Å
Subcollector	Si	n+	P	$2 \times 10^{19}cm^{-3}$	1μm
Substrate	Si(100)	p-		$1 \times 10^{12}cm^{-3}$	540μm

Previously, our group has developed a self-aligned mesa structure SiGe HBT process [1]. This process technology was not fully self-aligned, and required a very critical optical lithography for the collector contacts beside a region with vertical topography of 1.6 μm. The conflicting requirement of high yield through larger gap between collector contacts and base mesa, and the requirement for high performance obtained with the smallest gap, was not achieved satisfactorily. Fig. 2 shows a graphic of the HBT cross-section where the area of critical alignment is highlighted.

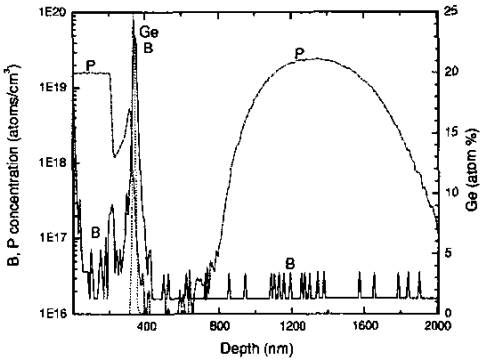

Fig. 1. SIMS profile of CVD-grown device (20371S).

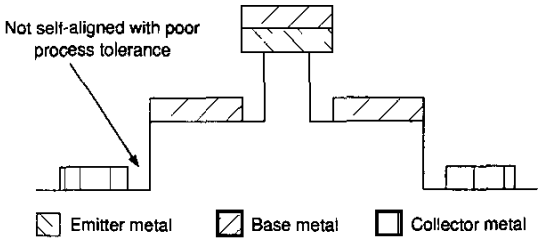

Fig. 2. Original process with non-self-aligned base collector.

An alternative fully self-aligned process was later developed to address the issues of the original process. This was reported in [2]. This fully self-aligned process improves on device performance but has a limitation of a very fragile base overhang with a thickness of about 200 Å during processing, which leads to poorer yield. Fig. 3 shows a pictograph of the HBT with the thin base overhang.

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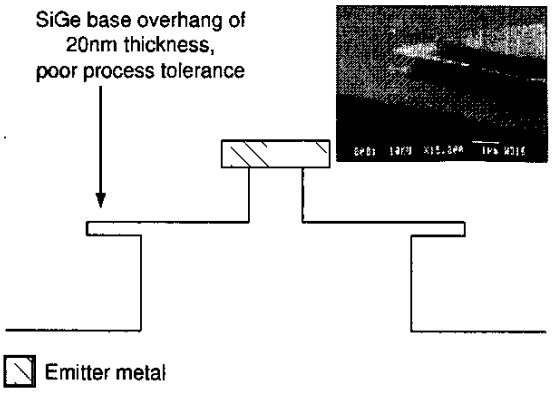

Fig. 3. Improved process with very thin overhang of SiGe base leading to poor process yield. Inset from [2].

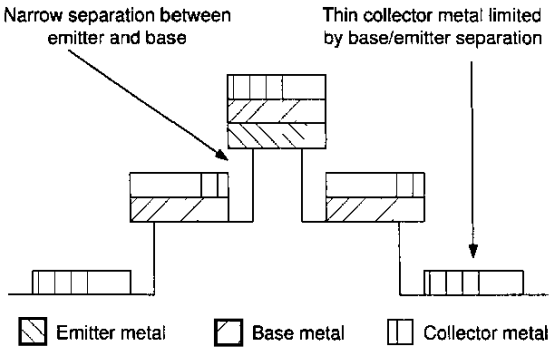

Fig. 4. HBT-PT1 developed for reduced process tolerance. This process has concerns of collector metal thickness being limited by the base emitter separation.

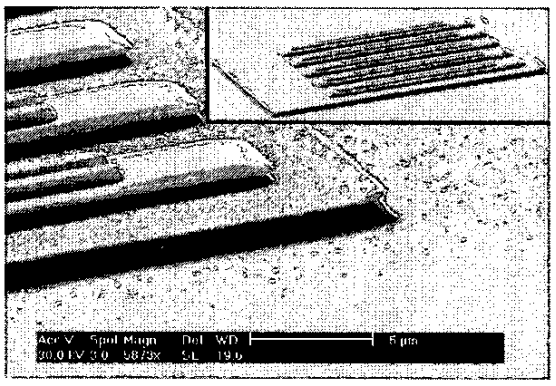

Fig. 5. SEM photographs of completed HBT using HBT-PT1.

Recognizing the limitations of our previous processes in achieving high yield requirement for MMIC applications, we have developed two new fully self-aligned process technologies that overcome the previous shortcomings. The first new process technology (HBT-PT1) has its own attendant limitations, while the second new process technology (HBT-PT2) has completely resolved our process problems with an added advantage of using one less lithography step.

HBT-PT1 follows closely the ideas of [2] while trying to overcome the weakness of the thin base overhang. This technology has its own restrictions where the collector metal is limited by the base-emitter separation. Fig. 4 shows the schematic of HBT-PT1 with the limitations highlighted and Fig. 5 shows the Scanning Electron Microscope (SEM) photographs of the completed 10 finger HBT. The process follows [1] except that base metal deposition is composed of Pt/Au = 200/600 Å. The base mesa is formed using isotropic Reactive Ion Etching (RIE) etching with photoresist protecting the emitter-base area. The isotropic RIE etching is achieved by increasing the chamber pressure to reduce the mean free path of the ions. This reduces the vertical etching profile of the RIE. The collector metal is then deposited self-aligned to the base metal using Ti/Pt/Au/Ti = 100/100/800/50 Å. The 50 Åthin layer of Ti acts as a visual cue for a later contact via holes process step by changing the underlaying color of the gold. A completely etched via hole will show a bright gold color as the Ti will also etch away, while an incompletely etched via hole will still show a dull gold color due to the presence of the Ti layer.

HBT-PT2 has completely resolved our process limitations, while maintaining a high performance with reduce process tolerance by using two self-alignment process. Fig. 6 shows an illustration depicting the self-aligned base-collector in HBT-PT2, while Fig. 7 shows the SEM photographs of the completed HBT. The process follows [1] except that after the base metallization of Pt/Au = 200/1000 Å, the collector metal lithography is done. This photoresist mask, which exposes the area where the collector metal should be deposited on the sub-collector, is used for the next three steps. First, a vertical RIE etch is performed to etch away the collector layer of about 6000 Å. Second, an isotropic RIE etch is performed to etch to the highest doped depth in the sub-collector. This step also creates a self-alignment to the photoresist. Third, collector metal of Ti/Pt/Au/Ti = 300/200/2500/50 Å is deposited self-aligned to the photoresist pattern on top of the base metal. The final 50 Åthin layer of Ti acts as a visual cue for a later contact via holes process step as previously described in HBT-PT1.

III. Device Characteristics

The DC and RF characteristics of both 10 finger and 20 finger common emitter devices developed based on HBT-PT2 have been measured, showing the typical results from the heterostructure, lateral layout design and process technology.

The 10 finger common-emitter device has an emitter area of 780 μm^2. The common-emitter forward Gummel

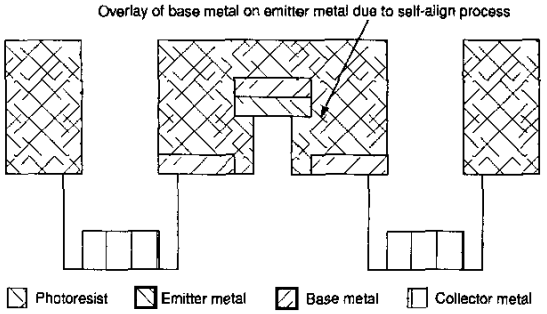

Fig. 6. HBT-PT2 developed for reduced process tolerance. This process has eliminated disadvantages from our previous process technologies while using one less lithography step.

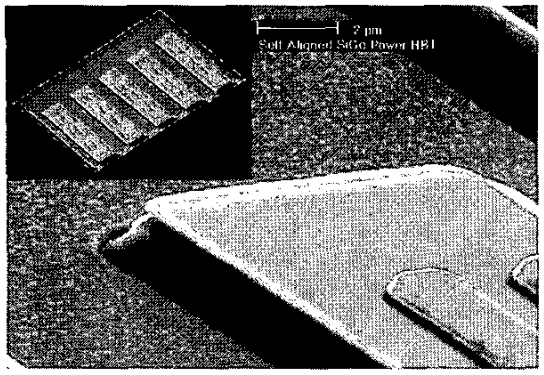

Fig. 7. SEM photographs of completed HBT using HBT-PT2.

plot was measured and is shown in Fig. 8. The collector current-voltage characteristics are shown in Fig. 9. The maximum collector current here is about 200 mA, and a collector-emitter voltage swing of 8 V was easily tolerated. Using (1), it is estimated that the device will have a linear high power performance of about 23 dBm.

$$P_{out} = \begin{pmatrix} V_{swing} \\ 2\sqrt{2} \end{pmatrix} \cdot \begin{pmatrix} I_{swing} \\ 2\sqrt{2} \end{pmatrix} \quad (1)$$

On-wafer small signal RF characteristics were measured using an HP8510C vector network analyzer from 50 MHz to 18 GHz. Fig. 10 shows the current gain $|h_{21}|$ and the unilateral power gain U of the 10 finger device at DC bias of I_C = 70 mA and V_{CE} = 3 V.

Similar performance characteristics were measured for a 20 finger common-emitter HBT. The results are shown in Figs. 11 to 13.

IV. Conclusion

Two new process technologies for reduced process tolerance have been demonstrated. HBTs fabricated using these technologies have shown good DC and RF performance useful for future MMIC power amplifier work.

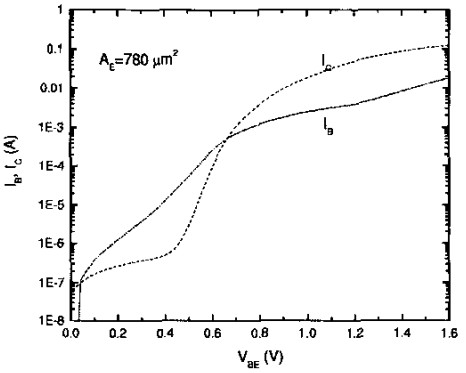

Fig. 8. Forward Gummel plot measured in common-emitter configuration of 10 finger HBT.

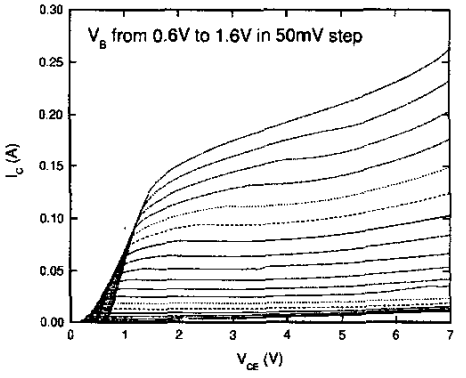

Fig. 9. DC I-V characteristics measured in common-emitter configuration of 10 finger HBT.

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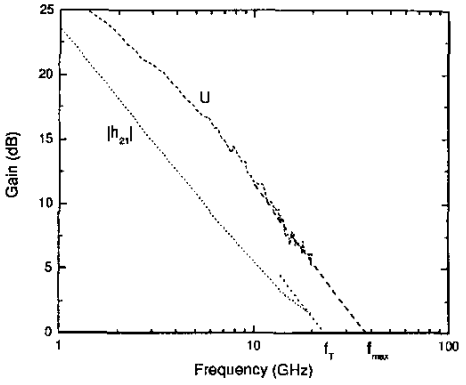

Fig. 10. Measured small-signal frequency response of the 10 finger device at DC bias of I_C = 70 mA and V_{CE} = 3 V.

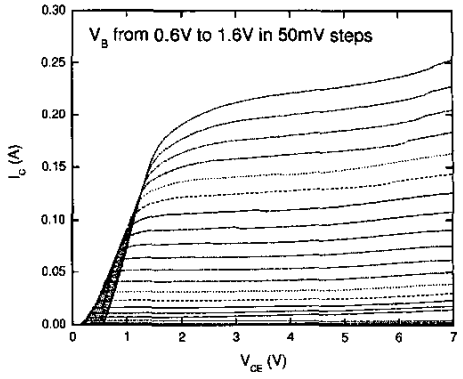

Fig. 12. DC I-V characteristics measured in common-emitter configuration of 20 finger HBT.

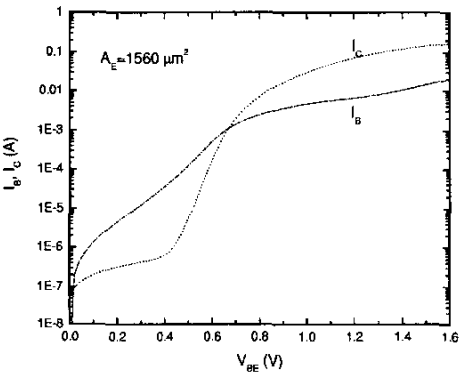

Fig. 11. Forward Gummel plot measured in common-emitter configuration of 20 finger HBT.

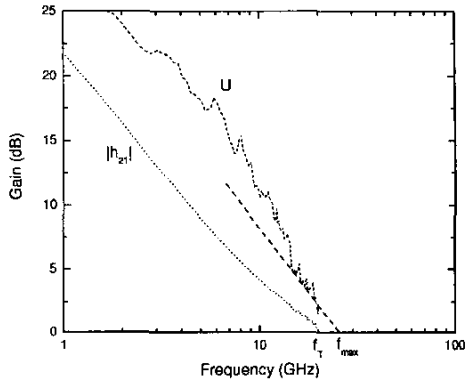

Fig. 13. Measured small-signal frequency response of the 20 finger device at DC bias of I_C = 160 mA and V_{CE} = 4 V.