Optimal Design and Experimental Characterization of High-Gain GaInP/GaAs HBT Distributed Amplifiers

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Abstract– **The design methodology of high-gain GaInP/GaAs HBT distributed amplifiers is presented. Distributed amplifiers with different active cells and number of stages have been compared for high-gain (>12 dB) and high-bandwidth (>25 GHz) performance. Based on the results, a 3-stage distributed amplifier with a S_{21} gain of 12.7 dB over 27.5 GHz bandwidth was successfully fabricated and tested.**

I. INTRODUCTION

High-speed optical communication (≥40 Gb/s) requires ultra-wide bandwidth optical receivers. Such receivers should meet the low-phase jitter requirement of optical systems which can only be met by using HBT distributed amplifiers due to HBT good threshold voltage uniformity and low phase jitter properties [1][2]. Traditional amplifier designs fail to meet this requirement due to their limited frequency performance while HEMT or MESFET-based distributed amplifiers have in principle smaller threshold voltage uniformity and higher phase jitter.

InP-based HBT distributed amplifiers have achieved flat gain of 7 dB over a bandwidth of 55 GHz [1] while record performance has been demonstrated from DC up to 100 GHz using InP-based HEMTs [3]. The use of InP-based technology offers the advantage of integration possibility with InGaAs PIN diodes and thus operation at 1.55 μm wavelength. Employment of GaAs-based technology allows realization of integrated optical receivers for short wavelength (~0.8 μm) communication. It can also be used in conjunction with InGaAs diodes in hybrid form for long wavelength systems. GaAs technology offers the advantage of high throughput, high yield and process maturity over its InP-based counterpart. Moreover, the lack of integration capability with 1.55 μm photodiodes can be compensated by the significant progress made recently in flip-chip mounting technology [4].

In this work, we present a methodology to design high-gain HBT distributed amplifiers and demonstrate its validity through experimental results. Distributed amplifiers with different active cell designs and various number of stages have been compared for high-gain (>12 dB) and high-bandwidth (>25 GHz) requirement. Based on the results, a 3-stage large bandwidth 50 MHz-27.5 GHz distributed amplifier with a S_{21} gain of 12.7 dB was fabricated. GaInP/GaAs HBT technology has been employed for its realization since it offers several advantages over AlGaAs/GaAs such as high injection efficiency and excellent etching selectivity between GaInP and GaAs which, contributes to process yield.

The fabricated circuit has a common-collector cascode active cell designed using the attenuation compensation technique [5]. The gain-bandwidth product of this amplifier is among the highest reported for HBT distributed amplifiers [1][5][6].

II. DESIGN OF THE GAINP/GAAS DISTRIBUTED AMPLIFIER

On-wafer probe measurement of discrete 2×30 μm^2 HBTs was used to model the device inside the HP-EESOF LIBRA environment. A physical small-signal model was extracted from cold and hot S-parameter measurements. The developed small signal model was used to design distributed amplifiers with different active cell designs and various number of stages. Fabricated 2×30 μm^2 HBTs showed a

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DC gain of 35 and cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of 55 and 65GHz, respectively.

Distributed amplifiers using traditional approaches such as common-emitter and cascode active cells were examined first. These designs were found to provide limited values of gain due to the relatively high access resistance of the HBT base and collector terminals; $S_{21} < 8$ dB under input and output matched condition. Increasing the number of stages only increased the gain of the amplifiers at low frequencies. The high losses introduced by the HBT input and output series resistances resulted in an overall gain reduction at high frequency (> 20 GHz) as the number of stages exceeded four. Therefore, we concluded that such designs are not suitable for high-gain distributed amplifiers and pursued alternative design approaches as explained in this paper. Reduction of the base and collector access resistances could, however, help to improve the gain-bandwidth characteristics of distributed amplifiers using common-emitter or cascode active cell designs.

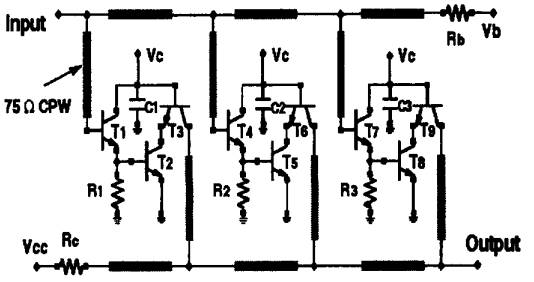

Fig. 1: Circuit schematic of the 3-stage GaInP/GaAs HBT distributed amplifier using common-collector cascode scheme (Circuit A).

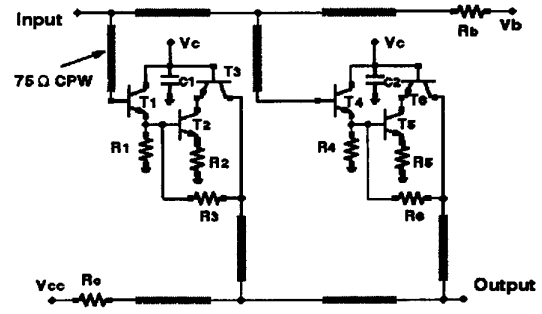

Fig. 2: Circuit schematic of 2-stage HBT distributed amplifier using common-collector cascode scheme with additional feedback resistors (Circuit B).

The alternative design approach explained in this work is based on the attenuation compensation technique [5], namely a common collector stage followed by a cascode transistor pair. This scheme provided high gain and high bandwidth as described later. No active load was employed at the input and output transmission lines as reported by [2], [7]. The common-collector stage (T_1, T_4 or T_7 in Fig. 1) provides at the base and thus input CPW line a transformation of the capacitive loads C_{BE} seen at the emitter of HBT T_1, T_4, T_7 into a negative resistance for the frequencies of interest. The effective negative resistance, compensates the losses due to the loading effect of the CPW line and the other transistors. Resistors R_1, R_2 and R_3 serve as biasing resistors. Our simulation showed that the required gain and bandwidth specifications of $S_{21} > 12$ dB, BW > 25 GHz can be achieved using only three stages of amplification of this design scheme. Fig. 1 shows a 3-stage distributed amplifier based on the "common-collector cascode" active cell approach (Circuit A).

Addition of two feedback resistors (R_2 and R_3 in Fig. 2) to the common-collector cascode active cell improved the overall performance of the circuit in terms of bandwidth (Circuit B, Fig. 2). These resistors were inserted from the collector of output transistors (T_3 and T_6) to the emitter of input transistors (T_1 and T_4) and also in the emitter of T_2 and T_5. Using this approach it was found that only two stages of amplification are adequate for achieving high-gain and high-bandwidth performance ($S_{21} > 12$ dB, BW > 25 GHz); equivalent performance using Design A necessitates three stages of amplification. The feedback resistors helped to stabilize the gain of individual stages and led to suppression of ripples in the gain-frequency characteristics despite the use of only two stages of amplification.

Fig. 3 shows the simulated S-parameters of the circuits of Fig. 1 (circuit A) and Fig. 2 (circuit B) using the HBT small-signal model inside the HP-EESOF LIBRA environment. As the figure indicates, both circuits provide high gain, high-bandwidth characteristics. The input and output matching of both circuits are better than –8 dB over the operation bandwidth under 50 Ω input

and output termination. Fabrication and measured characteristics of Circuit A are reported in the next section.

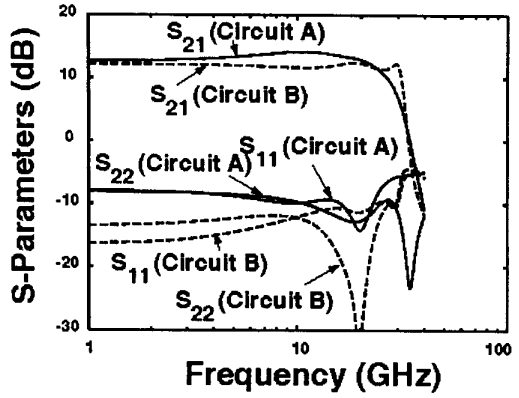

Fig. 3: S-parameter simulation of distributed amplifiers with (a) 3-stage common-collector cascode (Circuit A) and (b) 2-stage common-collector cascode with additional feedback resistors (Circuit B).

III. GaInP/GaAs HBT MMIC Technology and Characterization

The distributed amplifier circuit of Fig. 1 (Circuit A) was fabricated using the GaInP/GaAs HBT MMIC technology developed at the University of Michigan. GaAs technology offers the advantage of high throughput, high yield and process maturity over its InP-based counterpart. This technology takes advantage of several advanced techniques that proved to permit realization of high performance discrete and integrated HBT circuits of high-reliability and yield [8][9].

The HBT layers were grown using a special developed hydride and hydrogen-free chemical beam epitaxy (CBE) process with very low defect density (<10 def/cm^2). Details of the process have been previously reported by the authors [10]. Self-aligned GaInP/GaAs single HBTs were fabricated on these layers using simple, all wet chemical etching which minimizes layer damage and allows excellent selectivity. Non-alloyed metals were deposited for emitter, base and collector contacts. A laterally etched undercut (LEU) technology was developed and applied in the base-collector region to reduce the base-collector capacitance by 25% (C_{BC}) while avoiding base resistance degradation. The overall maximum oscillation frequency (f_{max}) was improved by 20% due to employment of lateral etch undercut. The associated gain improvement and extension of operation frequency range led to improved gain and bandwidth performance of the amplifier. Silicon dioxide was used for passivation.

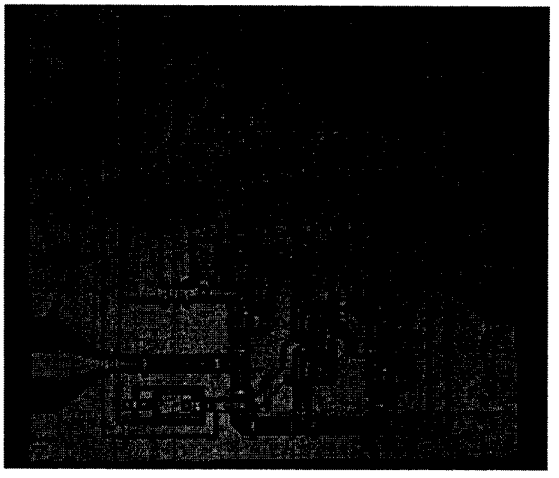

Fig. 4: Photomicrograph of fabricated distributed amplifier (Circuit A). The chip size is 1125 × 1200 μm^2.

Integrated resistors were realized using 700Å Ni/Cr thin metal film deposition. MIM monolithic capacitors for high-frequency grounding were fabricated using Al_2O_3. The amplifier chip was connected to the high-frequency test ports via 50Ω CPW lines. Airbridge interconnects along the transmission lines reduced line moding, allowing, therefore, support of pure CPW mode operation. Fig. 4 shows a photomicrograph of the fabricated distributed amplifier in GaInP/GaAs HBT technology. The chip size is 1125 × 1200 μm^2.

On-wafer testing was used for circuit characterization. The S-parameters of the distributed amplifier were measured from 50 MHz to 40 GHz using an HP8722D network analyzer.

Fig. 5 shows the measured S-parameters of the amplifier. A S_{21} gain of 12.7 dB over a bandwidth of 27.5 GHz was achieved. This corresponds to a 118 GHz Gain×Bandwidth product, which is among the highest reported values for HBT-based distributed amplifiers

[1][5][7]. Amplifier isolation (S_{12}) ranged from –50 to –12 dB in the operation bandwidth while input and output matching (S_{11}, S_{22}) ranged from –13 to –4 dB. The input and output matching was higher than the expected values from the simulation.

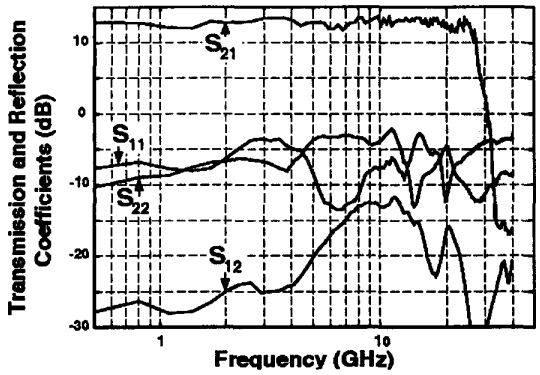

Fig. 5: Measured S-Parameters of distributed amplifier (Circuit A).

V. CONCLUSIONS

The design methodology for high-gain high-bandwith HBT distributed amplifiers has been discussed. The study suggests that, common-emitter or cascode active cell designs are not suitable for high-gain distributed amplifier characteristics. Designs based on a common-collector cell followed by a cascode pair with or without additional feedback resistors (Circuit A, Fig. 1 and circuit B, Fig. 2) can provide high-gain, high-bandwidth performance of S_{21} > 12 dB and BW > 25 GHz. The introduction of feedback resistors in Circuit B allows one to reduce the number of stages and as a result only 2 stages of amplification are needed. Further addition of stages leads in gain improvement at low frequency and gain degradation at high frequency due to the enhancement of resistive losses through the device and passive components of the circuit.

Based on the performed analysis, a 3-stage GaInP/GaAs-based HBT distributed amplifier with common-collector cascode active cell design was fabricated and tested. A gain of 12.7 dB over a bandwidth of 50 MHz-27.5 GHz is reported using this approach which corresponds to 118 GHz gain-bandwidth product.

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