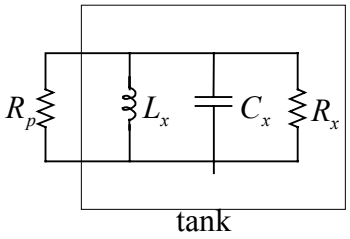
Loading of a LC ckt



$$Q_{orig} = \frac{R_x}{\omega_0 L_x} \qquad \sim 50{,}000$$

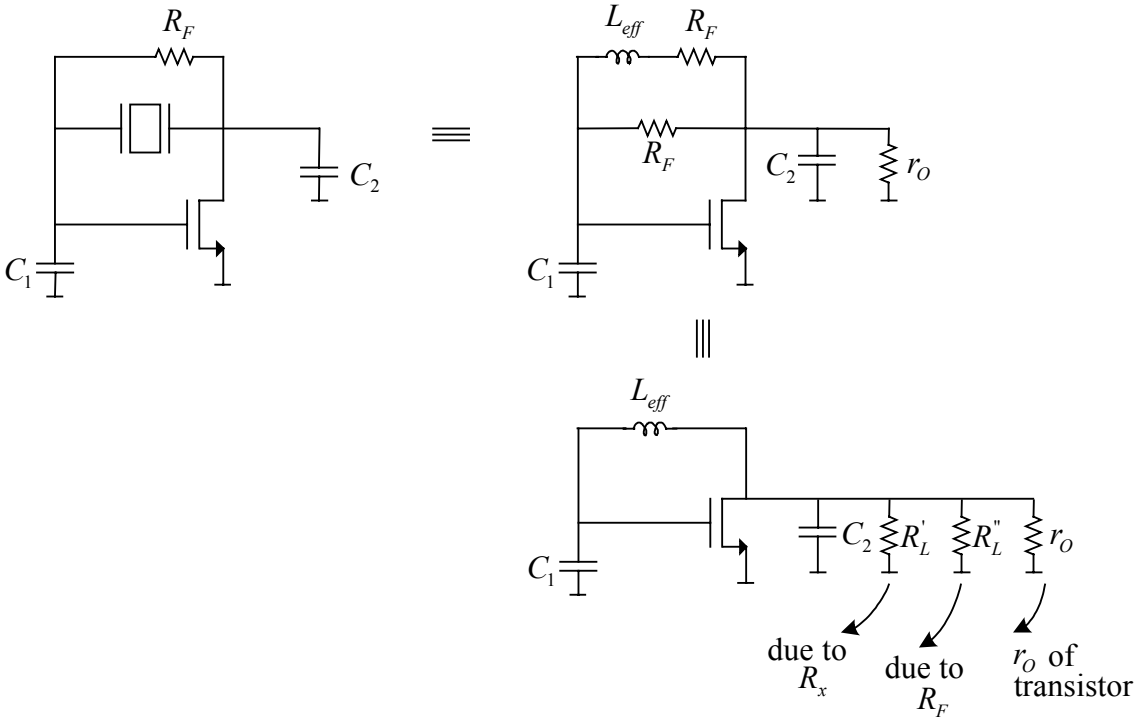
$$\omega_0 = \frac{1}{\sqrt{L_x C_x}}$$

$$Q_{eff} = \frac{R_p \| R_x}{\omega_0 L_x} = Q_{orig}\left(\frac{R_p}{R_x + R_p}\right)$$

$$R_L = R_p \| R_x \quad \rightarrow \quad Q_{eff} = Q_{orig}\left(\frac{R_L}{R_x}\right)$$

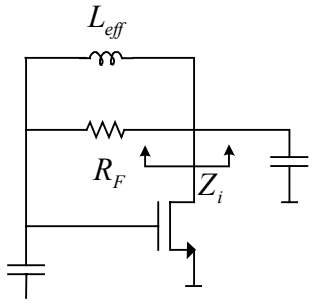
* Biasing the device in xtal Osc. through R_F

Pierce Osc.



Let's find $R_L^{"}$

Assume the only resistance is R_F



$$Z_L^{"} = \frac{jX_2\left(\frac{R_F jX_C}{R_F + jX_C} + jX_1\right)}{jX_1 + jX_2 + \frac{R_F jX_C}{R_F + jX_C}} =$$

skipping a lot of math

$$Z_L^{"} = \frac{R_F X_2^2}{X_C^2} - \frac{jX_1X_2}{X_C}$$

$$= R_F\left(\frac{C_1}{C_1 + C_2}\right)^2 + \frac{1}{j\omega_1(C_1 + C_2)}$$

$R_F = 200K\Omega$ ↓ $\sim 50\Omega$; ↓ 400Ω

$$\rightarrow R_L^{"} = R_F\left(\frac{C_1}{C_1 + C_2}\right)^2$$

$$R_L = R_L^{'} \| R_L^{"} \| r_O \longrightarrow Q_{eff} = Q_{orig}\left(\frac{R_L}{R_L^{'}}\right)$$

internal xtal loss

Xtal Power

$$Xtal\ Power = \frac{\hat{V}_0^2}{2R_L^{'}} \longrightarrow$$

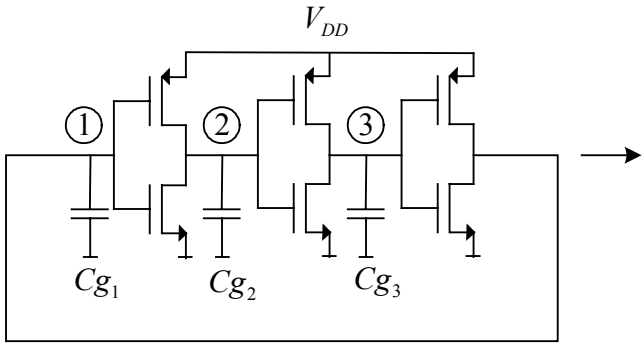
make sure that this power level is within xtal sating

AT - cut → take 10mws

models loss in xtal

Relaxation Oscillators

Astable Ring Oscilaator



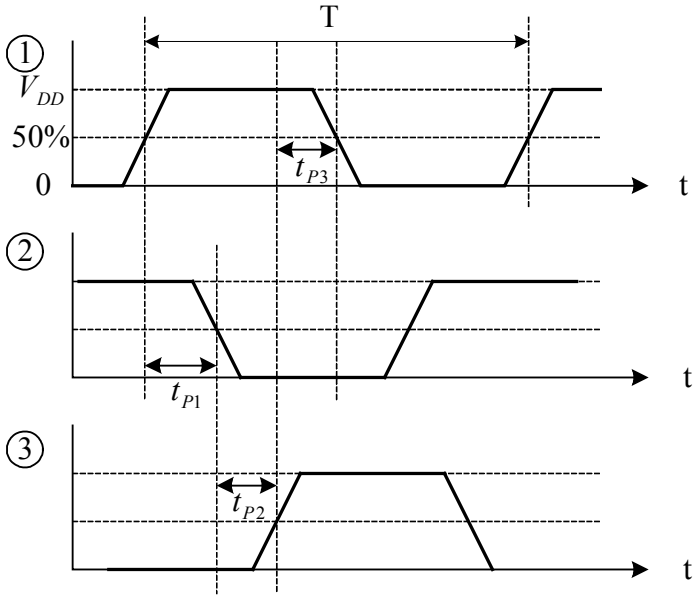
→ size of capacitances and strength of driving determines the freq. of oscillation

$$\frac{1}{2}T = t_{P1} + t_{P2} + t_{P3} = Nt_P$$

$$T = 2Nt_P \longrightarrow \boxed{f = \frac{1}{2Nt_P}}$$

→ gate propagation delay 50% → 50%

# of inverters has to be odd to get oscillation



Calculating average propagation delay

$t_{PLH} \triangleq$ response time of a gate to a low → high output transition

$t_{PHL} \triangleq$ response time of a gate to a high → low output transition

$$t_P = \frac{t_{PHL} + t_{PLH}}{2}$$

different as driving capabilities of NMOS and PMOS are different

$$t_P = C_L \int_{V_1}^{V_2} \frac{dV}{i(V)}$$

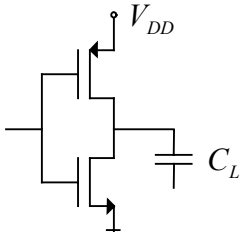
$t_{PHL} \longrightarrow V_1 = 0 \longleftarrow$ initial V_{out}

$V_2 = \frac{V_{DD}}{2} \longleftarrow$ final V_{out}

$$t_P = \frac{C_L(V_2 - V_1)}{I_{avg}}$$

average of currents at the each points of the voltage transition

$$t_P = C_L \frac{(V_{OH} - V_{OL})/2}{|I_{avg}|}$$



calculate t_{PLH}

* assumption
- V_{in} changes abruptly
- NMOS is off immediately
- PMOS contribute to charging current

note :

PMOS is in saturation as long as $V_{out} < |V_{tp}|$

$$I(V_{out}=0) = I(saturated)$$

$$I\left(V_{out}=\frac{V_{DD}}{2}\right) = I(linear) \quad \longleftarrow \quad V_{DD} = V_{OH} - V_{OL}$$

$$I_{avg} = \frac{I(V_{out}=0) + I\left(V_{out}=\frac{V_{DD}}{2}\right)}{2} = \frac{I_{sat} + I_{lin}}{2}$$

long channel device $\quad I_{sat} = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS} - V_{Th})^2$

$$I_{lin} = \frac{\mu C_{OX}}{2}\frac{W}{L}\left(2(V_{GS} - V_{Th})V_{DS} - V_{DS}^2\right)$$

let's make another approximation

PMOS is in saturation for the whole range

$\longrightarrow$ 5% error on less

$$\longrightarrow \quad I_{avg} = \mu C_{OX}\frac{W}{2L}(V_{DD} - |V_{ThP}|)^2$$

$$\longrightarrow \quad t_{PLH} = \frac{C_L V_{DD}}{\mu C_{OX}\frac{W}{L}(V_{DD} - |V_{ThP}|)^2} \approx \frac{C_L}{\mu C_{OX}\frac{W}{L}V_{DD}}$$

to decrease t_P

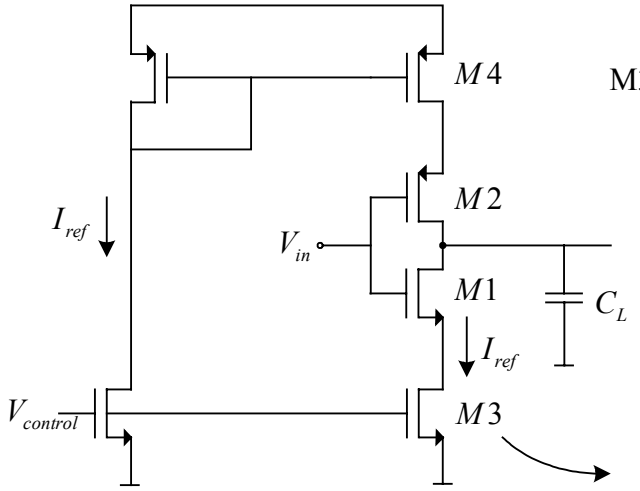
① reduce C_L

② increase W/L $\longrightarrow$ note : it also increases C_L

③ increase V_{DD}

Voltage Controlled Ring Oscillators

use current-starved inverter



M3 & M4 act as additional resistances

stays saturated for a large portion of a cycle

size of M1 dictates maximum current available to discharge C_L

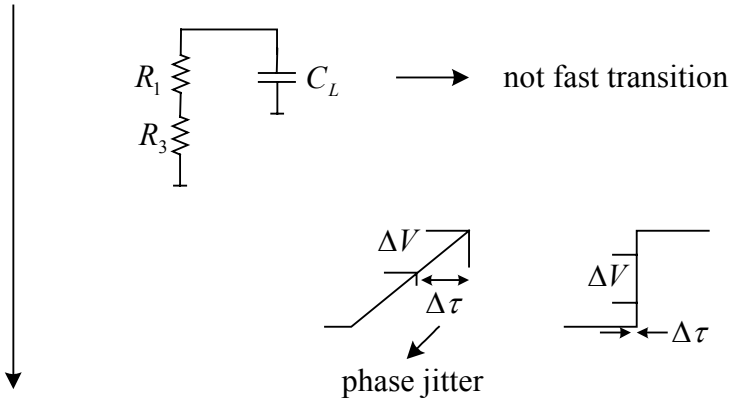
M3 cannot pull more current off C_L than M1 allows

Assuming short channel devices

$$t_{PLH} = \frac{C_L V_{DD}}{Const\,(V_{cont} - V_{Th3})}$$

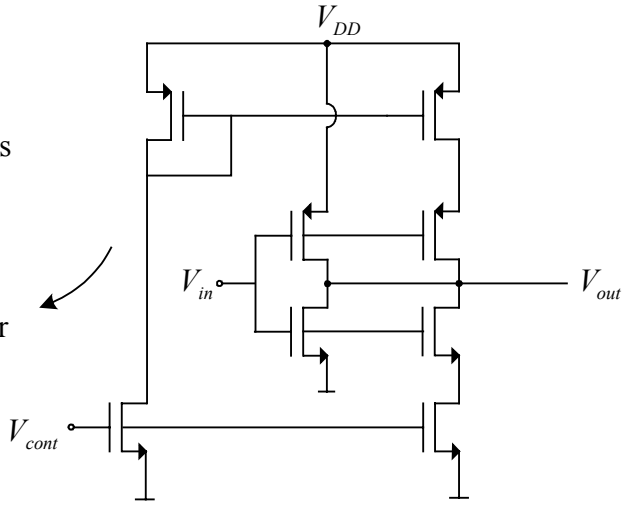
by changing V_{cont} you can change t_{PLH} → period and therefore freq. of oscillation

Problem



to reduce phase jitter you need faster transition

to solve this problem
put additional inverters

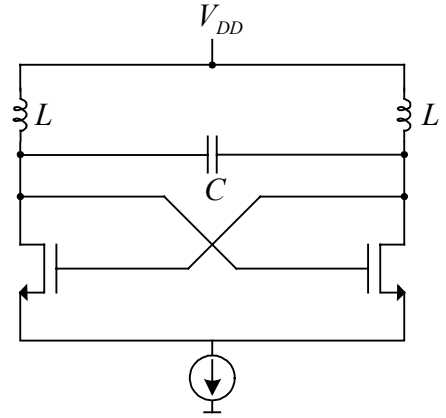


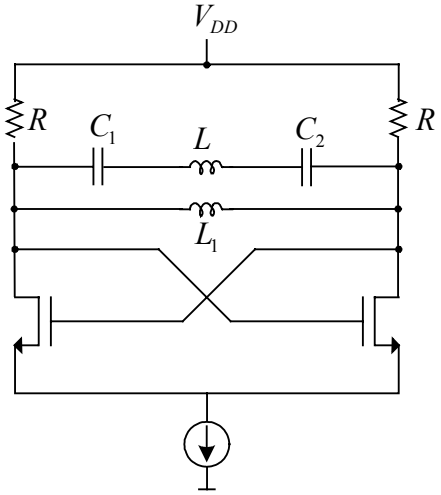
better phase jitter
performance
but less
tunability

still Ring Oscillators have a lot of phase noise
because of switching on/off the transistor

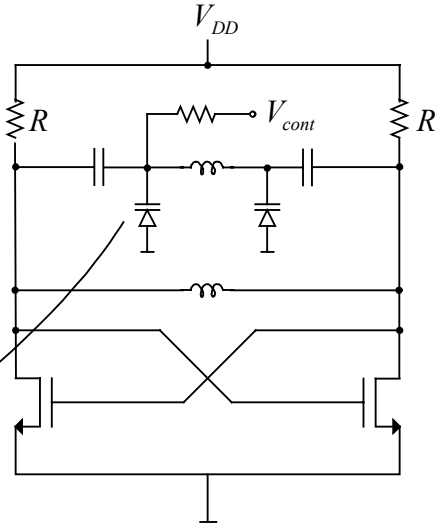
Source coupled multivibrators

based on negative resistance



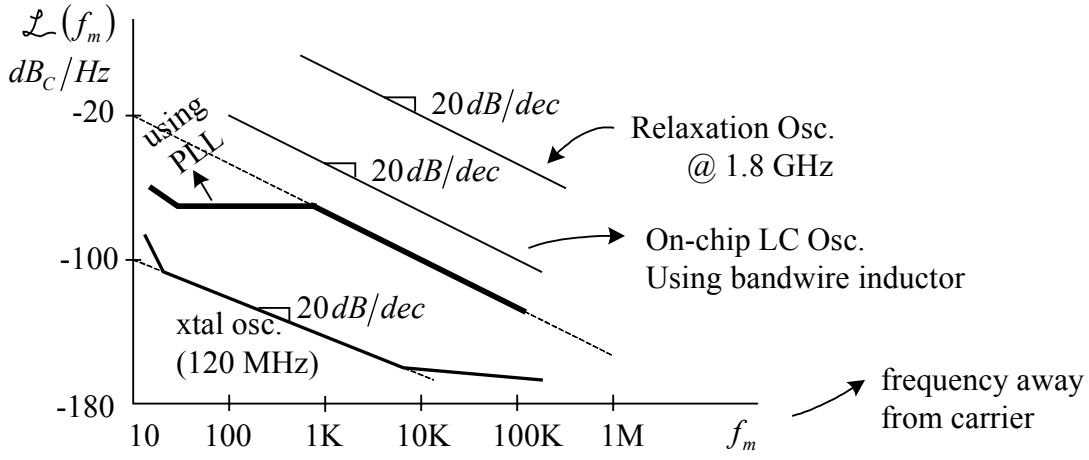


to make VCO



PMOS junction capacitances

Phase Noise



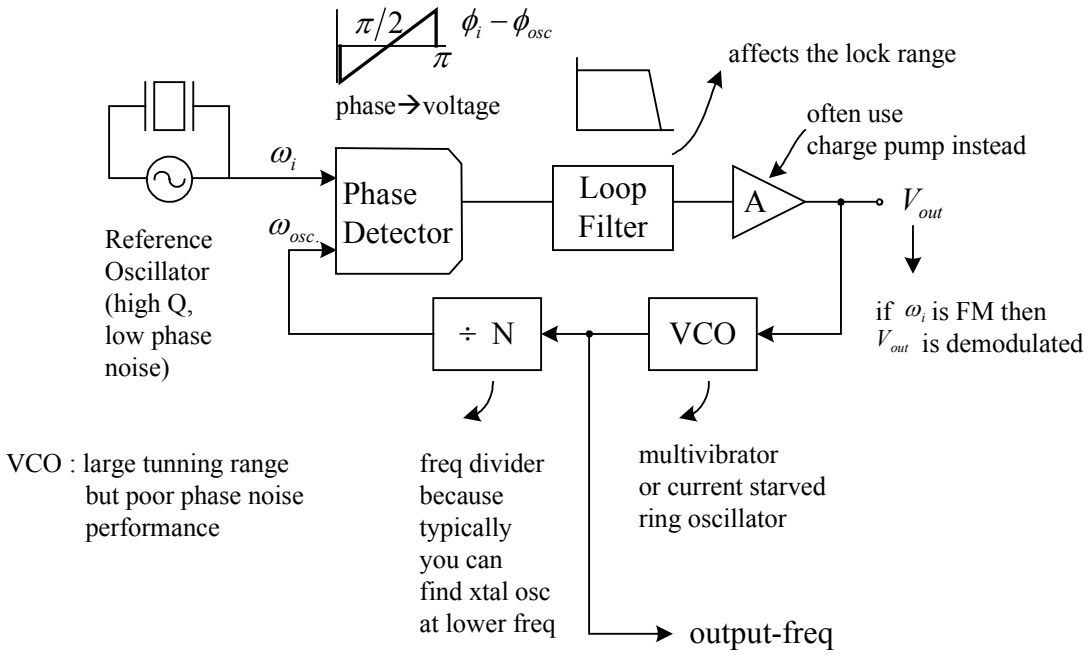
Phased-locked loop

wide variety of applications

* FM demodulators
* coherent digital transmission / defection
  (spread spectrum)
* clock synchronization
* tone detectors
* frequency synthesizers

main function : locks phases of two frequency sources

Block Diagram

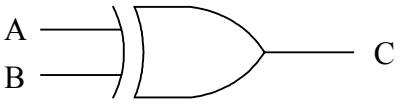


Phase detector

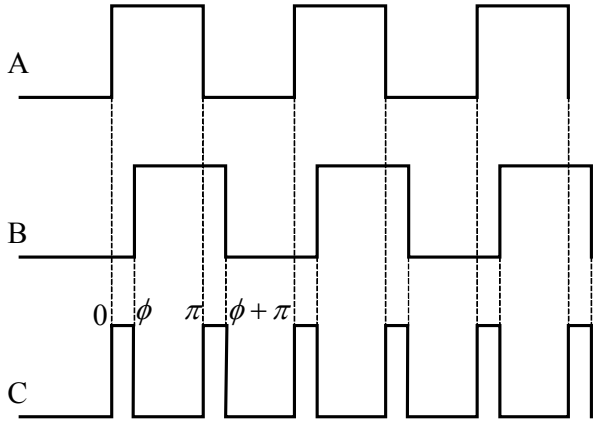
main function : change phase difference to voltage

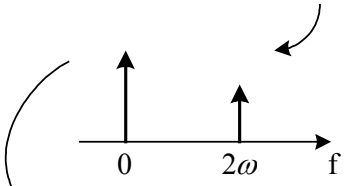
typical phase detectors
- balanced multipliers (mixers)
- exclusive OR
- edge sensitive FF

Exclusive OR phase detector



A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

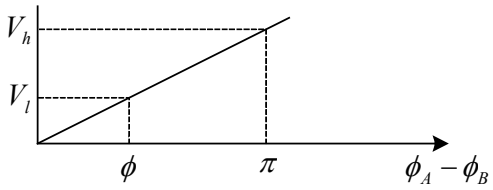




we need DC components

phase

$$V_{avg} = \frac{1}{2\pi}\int_0^{2n} V_C(t)\,d(\omega t)$$
$$= \frac{1}{2\pi}\left[2\phi(V_h - V_l)\right]$$
$$= \frac{\phi}{\pi}(V_h - V_l)$$



Multipliers as phase detectors

$V_1 = \hat{V}_1 \cos(\omega_1 t + \phi)$

$V_2 = \hat{V}_2 \cos(\omega t)$

multiply and invert

PD_{out}

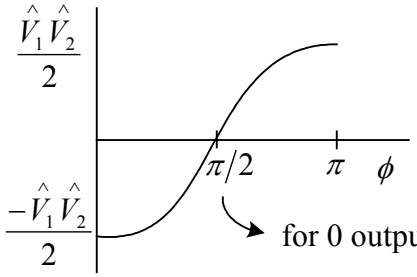
$-\hat{V}_1 \hat{V}_2 \cos(\omega_1 t)\cos(\omega t + \phi)$

$= \frac{-\hat{V}_1 \hat{V}_2}{2}\left(\cos(2\omega t + \phi) + \cos\phi\right)$

hf term to be filtered out by loop filter

dc term

$PD_{out} = \frac{-\hat{V}_1 \hat{V}_2}{2} \cos\phi$



for 0 output you need to have $\pi/2$ phase difference

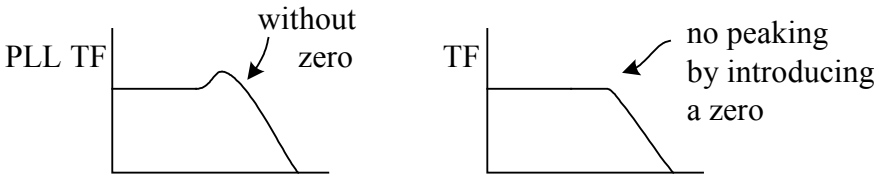
$(\pi/2 - \phi)$ → small

$PD_{out} \approx \frac{\hat{V}_1 \hat{V}_2}{2}(\phi - \pi/2)$

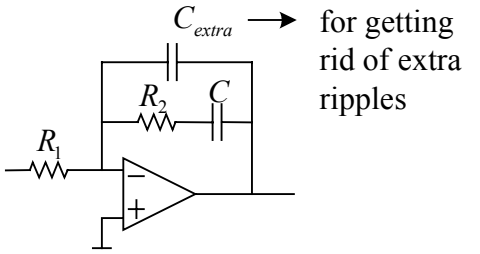
Loop filter

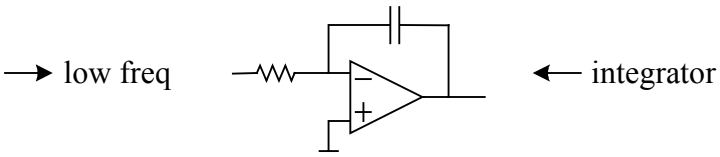
* must do averaging (integration) to get rid of higher freq. Components coming from PD

* for loop stability you also need a zero in the transfer function



Typical loop filter

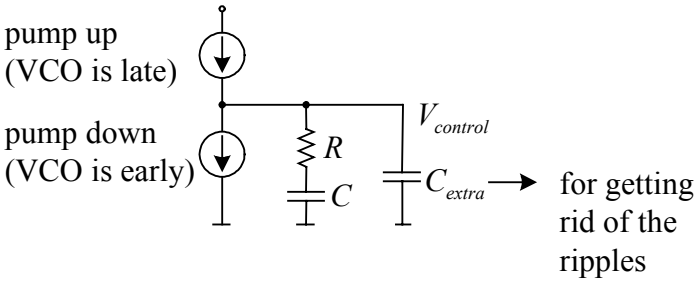




high freq : R_2C provides a zero in the transfer function

in reality you do not need an op-amp to do the filtering

A charge pump is enough

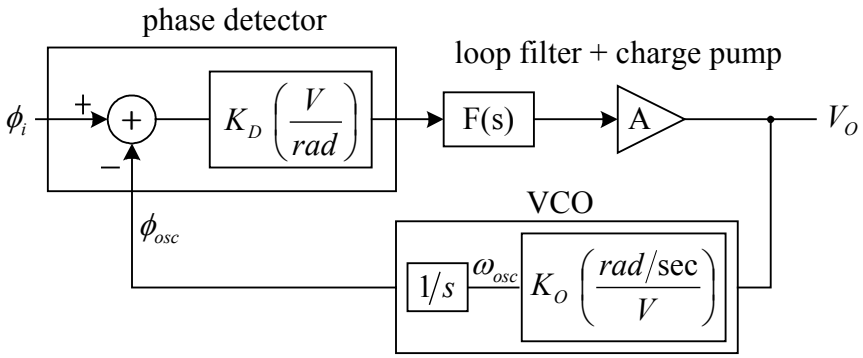


Lock condition

once the VCO frequency settles to follow the reference freq.
PLL is in lock condition

Linearized model for PLL in locked condition

think about your signals as phase not amplitude



$$\frac{V_O(s)}{\omega_i} = \frac{K_D F(s) A}{s + K_O K_D A F(s)}$$

depending on what loop filter you use
you can analyze your PLL function

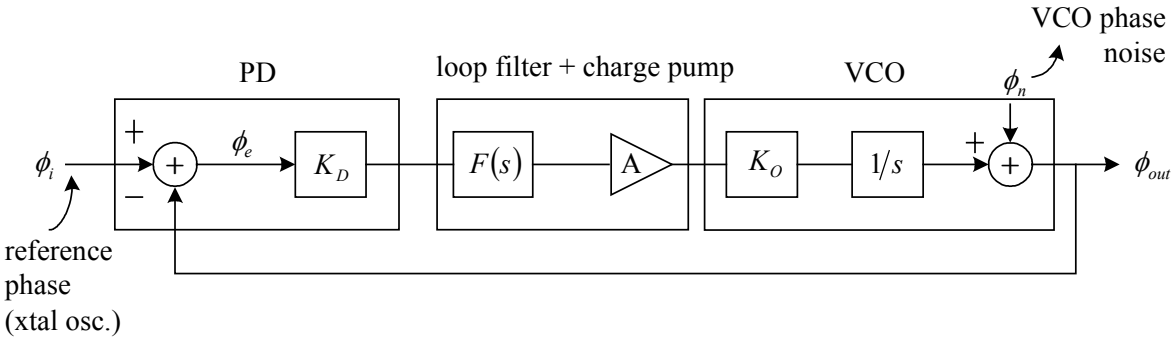
Important issues on PLL

Lock Range : The range of ω_i's over which
the PLL can maintain lock ⟶ depends on PD

Capture Range : has smaller range than lock range
This is the range when we are going from un-lock
to lock condition

capture range depends on loop filter
so by appropriate design of filter, you can make
capture range much different than lock range

Phase noise reduction using PLL



you can find the TF for phase

$$\phi_{out} = \frac{K\,F(s)}{s + K\,F(s)}\;\phi_i + \frac{s}{s + K\,F(s)}\;\phi_n$$

a lag-lead loop filter $\quad F(s) = \dfrac{1 + s/\omega_2}{s/\omega_1}$

crystal phase noise ↓ $\qquad$ VCO phase noise ↓

$$\phi_o = \frac{\omega_n^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}\;\phi_i + \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\;\phi_n$$

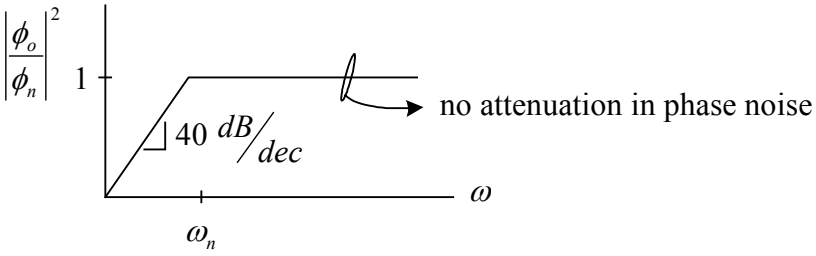
$$\zeta = \frac{1}{\sqrt{2}} \longrightarrow \text{no peaking is PLL response}$$

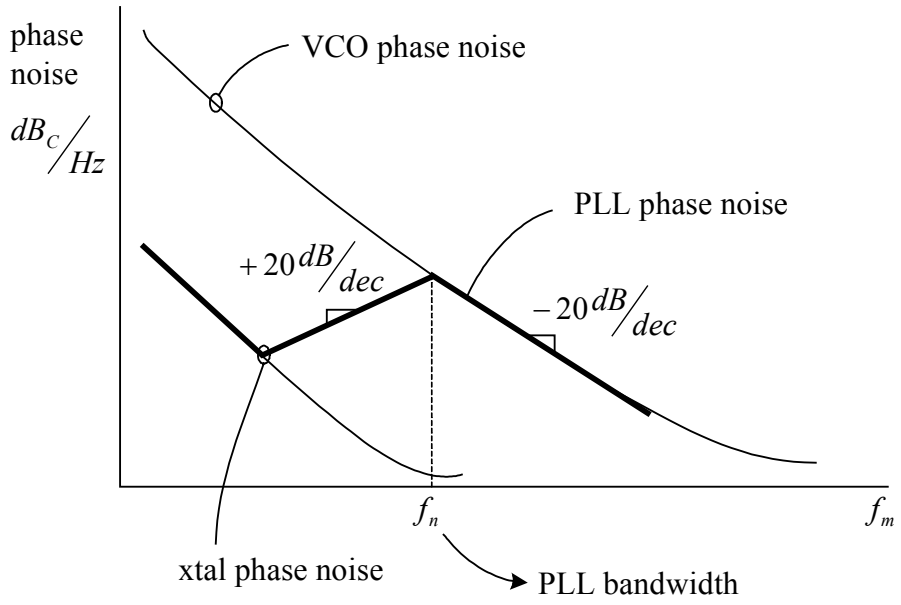
$$\left|\frac{\phi_o}{\phi_n}\right| = \frac{\omega^2}{\sqrt{\omega^4 + \omega_n^4}}$$

$$\omega << \omega_n \longrightarrow \left|\frac{\phi_o}{\phi_n}\right|^2 = \frac{f^4}{f_n^4} \qquad -40\ {}^{dB}\!/_{decade}$$

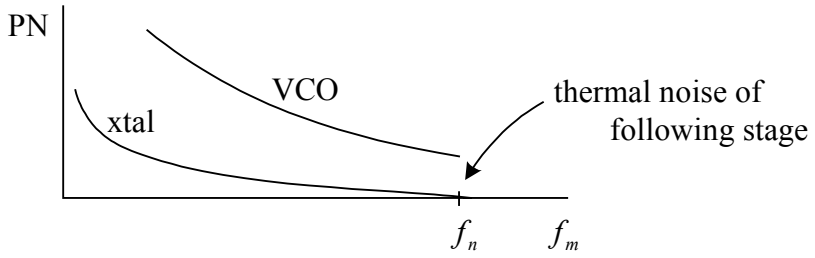
$$\omega = \omega_n \longrightarrow \left|\frac{\phi_o}{\phi_n}\right| = \frac{1}{\sqrt{2}}$$

$$\omega >> \omega_n \longrightarrow \left|\frac{\phi_o}{\phi_n}\right| = 1$$

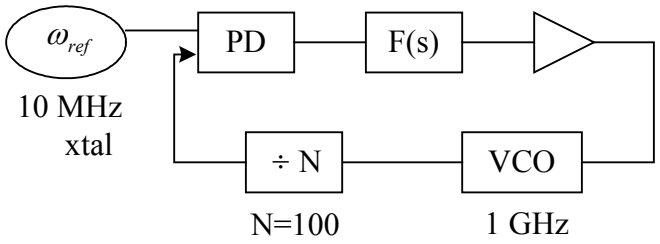


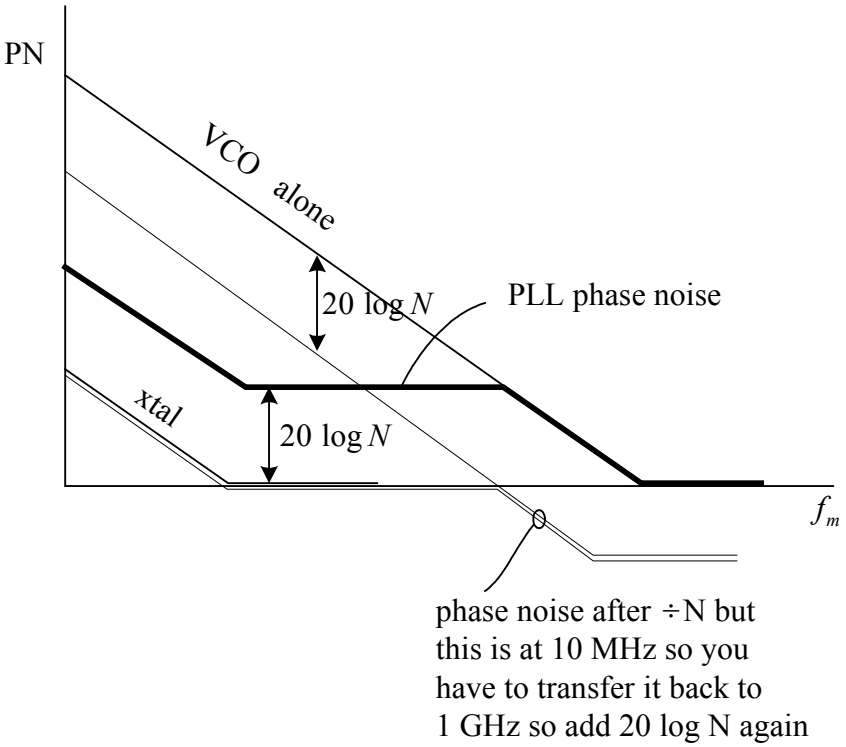


so make $\omega_n(f_n)$ as high as possible
but limit is xtal freq. of oscillation



So use freq. divider to compare $\frac{f_{VCO}}{N}$ *and* f_{xtal}



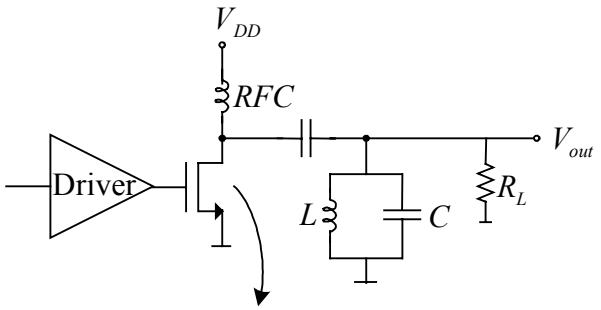


Power Amplifiers

typically bipolar transistors are preferred over CMOS (heterojunction bipolar transistor) due to higher freq. of operation and higher gain, higher efficiency

efficiency
- drain efficiency $\eta = \frac{P_{O\,RF}}{P_{DC}}$
- power added efficiency $PAE = \frac{P_{O\,RF}}{P_{DC} - P_{INRF}} < \eta$

Typical Power Amp Ckt :



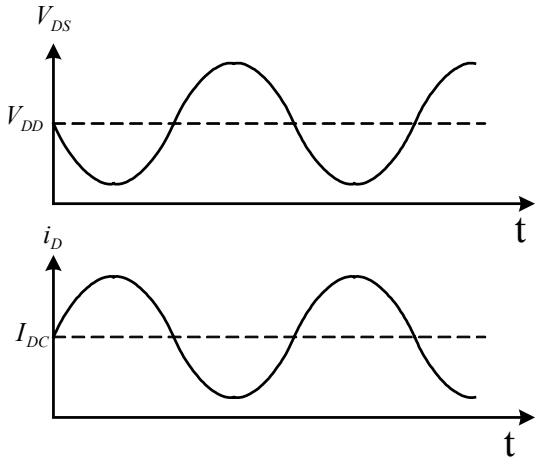
multi-finger : W ~ several mm

Different Classes of PA

Class A

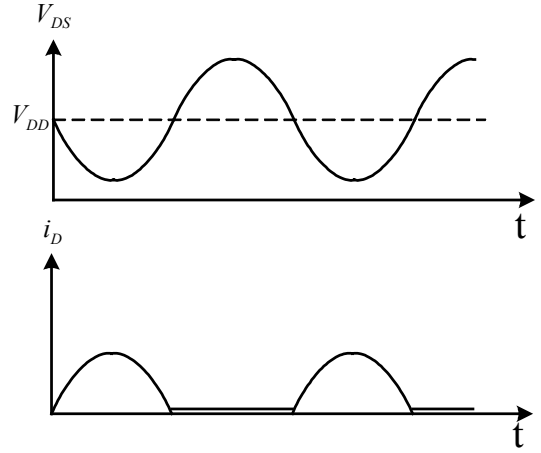
- linear
- low efficiency
- no clamping in V_{DS} , i_D

Class A



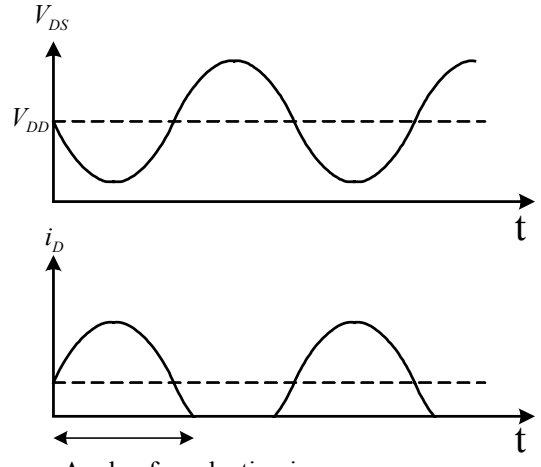
$\eta < 50\%$

Class B



$\eta < \frac{\pi}{4} = 78\%$

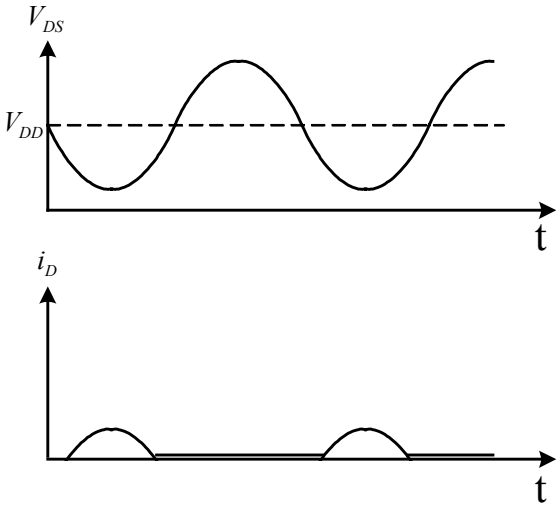
Class AB



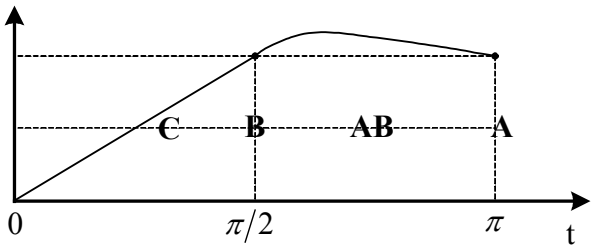
Angle of conduction increases

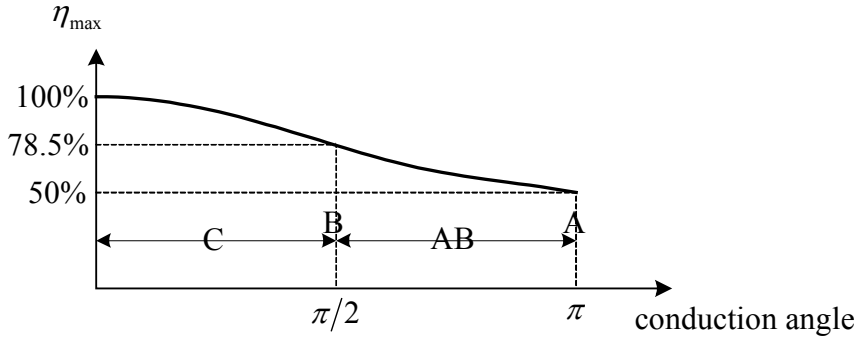
Class C

Reduced
conduction angle

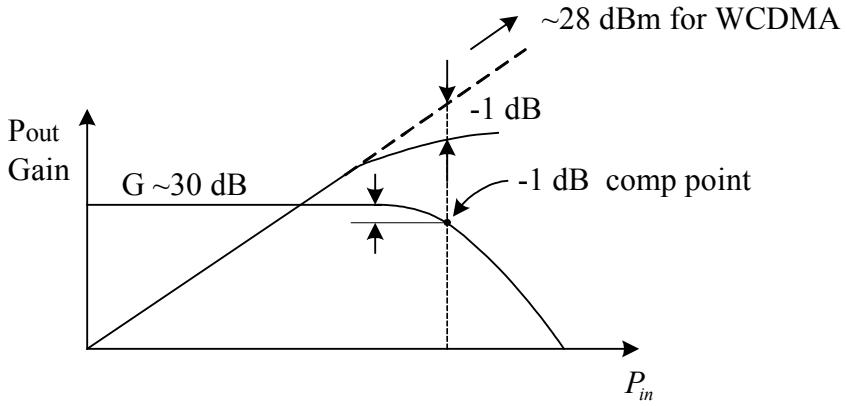


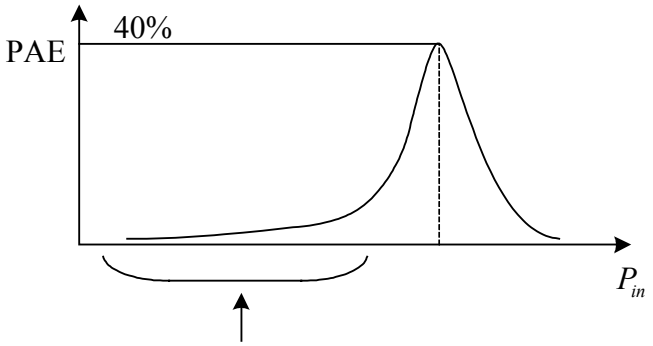
Port in terms
of condition angle





* what you typically observe





Problem is this range that your P_{out} (P_{in}) is low (urban areas) but your efficiency is also low

→ so you are still wasting a lot of DC power

→ to solve the problem use dynamic biasing or smart power Amp

There are higher classes of Amps (class E, F, S)

Problems * too non-linear

* often good for audio freq.

Advantages * very efficient $\eta \rightarrow 100\%$