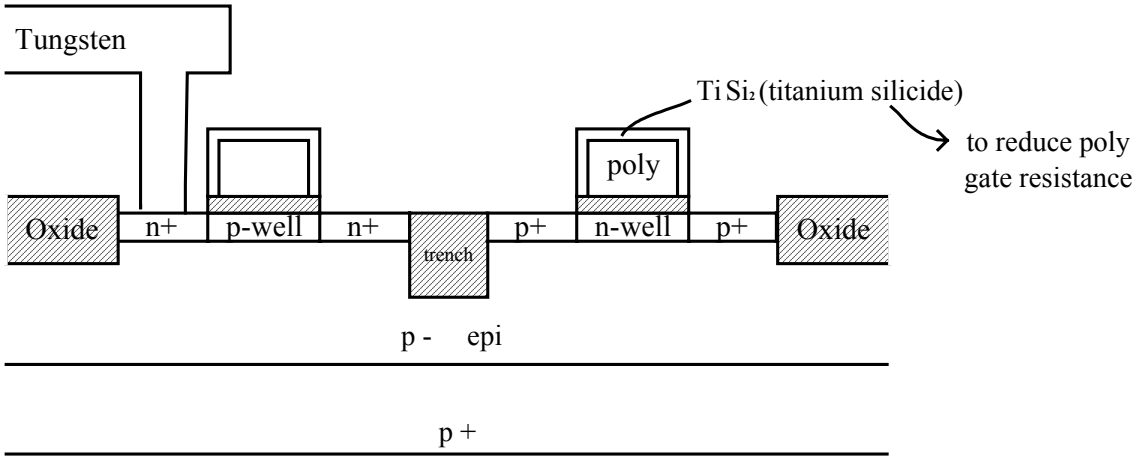
MOS Devices and Technology



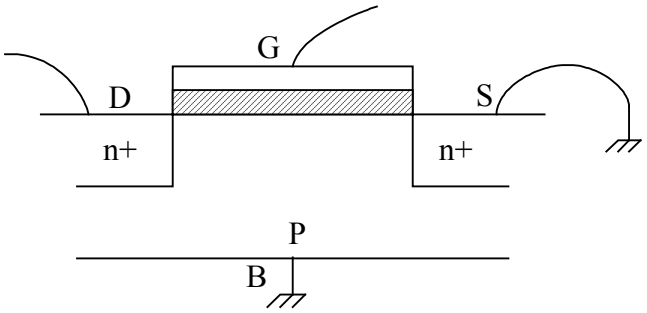
Dual-well epi process

MOS (Metal-Oxide-Semiconductor)

→ unipolar transistors → only one carrier exists

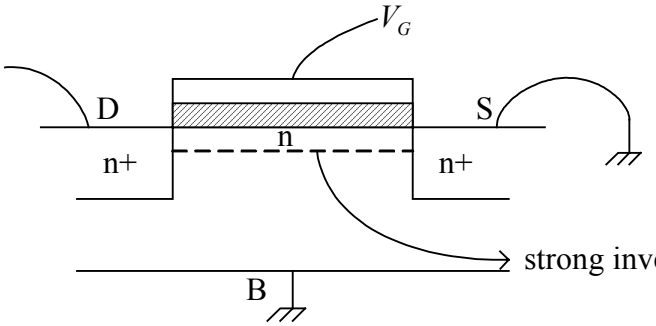
carrier
- hole → PMOS : slower transistors as holes have lower mobility compared to electrons
- electron → NMOS

Technology that uses both NMOS and PMOS is called CMOS (Complementary MOS)



at $V_G \sim 2\phi_F \Rightarrow$ channel forms and there will be conduction of electrons from source to drain

↳ fermi level $\phi_F = \frac{kT}{q}\ln(\frac{N_A}{n_i})$



→ strong inversion results in conduction

at strong inversion there is a fixed charge in the channel

$$Q_B = \sqrt{2qN_A\varepsilon|2\phi_F|}$$

→ potential for strong inversion

by increasing gate voltage this charge + channel thickness do not change

if the body is not grounded

$$|2\phi_F| \rightarrow |-2\phi_F + V_{SB}|$$

→ source-body voltage

V_{GS} needed to reach strong inversion is called

Threshold

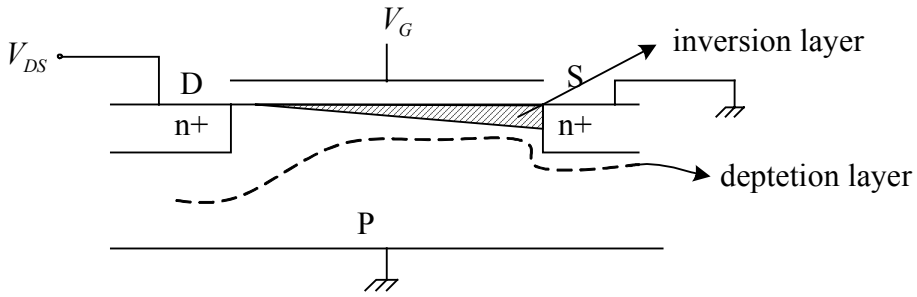
$V_T = V_{GS}$ @ strong inversion

$$V_T = V_{TO} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|})$$

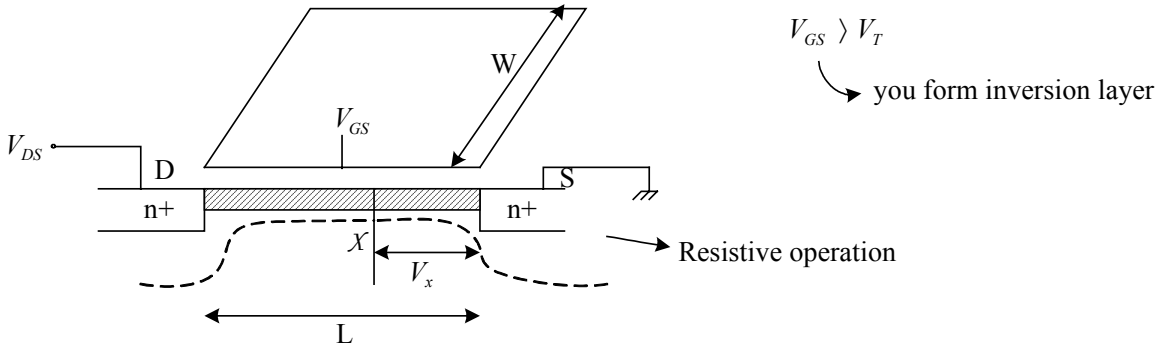
V_{TO}: relates to process and can be adjusted by shallow ion implantation → Threshold adjustment

γ: body-effect coefficient

→ Threshold voltage varies with substrate voltage (body effect)



Small V_{DS}



Induced charge $Q_i(x) = -C_{OX}(V_{GS} - V_x - V_T)$

$I_D = -v_n Q_i(x) W$

current that goes to drain(D)

electron velocity

mobile charge

width of channel

$v_n = \mu_n \frac{dV}{dx}$

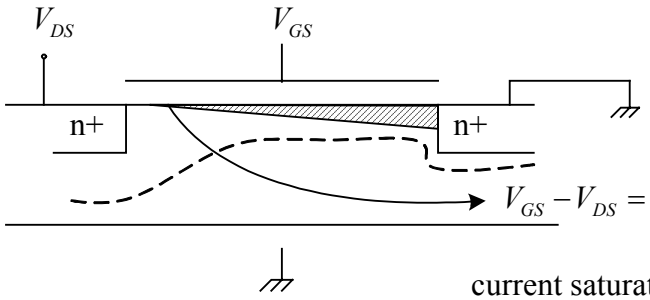
$$\Rightarrow \quad I_D dx = \mu_n C_{OX} W (V_{GS} - V - V_T) dv$$

$$\int_0^L \qquad \int_0^{V_{DS}}$$

$$I_D = \frac{W}{L} \mu_n C_{OX} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$K'_n = \mu_n C_{OX}$: Transconductance factor

when you increase V_{DS}



point of strong inversion

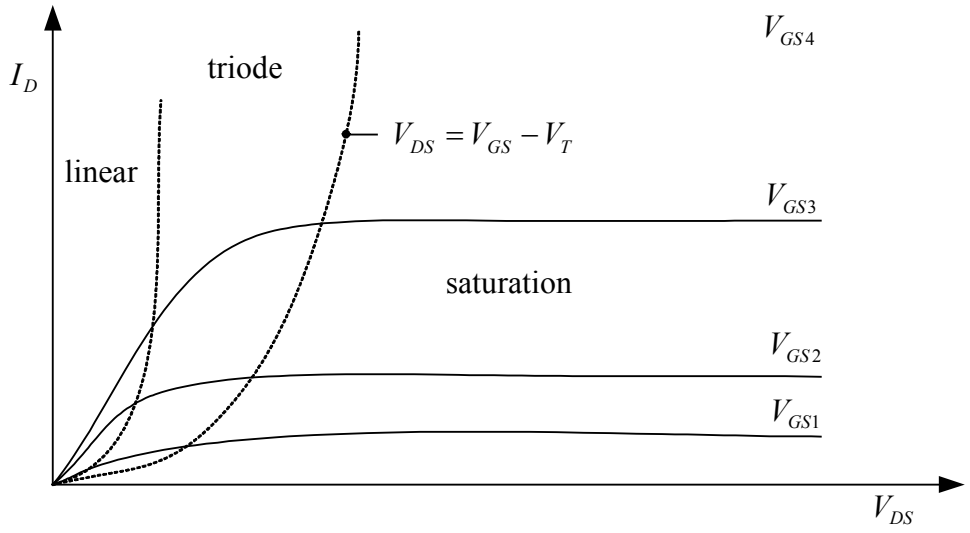
current saturates (I_D becomes independent of V_{DS})

$$V_{DS} = V_{GS} - V_T$$

put it in previous equation

$$I_D = \frac{\mu_n C_{OX} W}{2L}(V_{GS} - V_T)^2$$

constant (not a function of V_{DS})



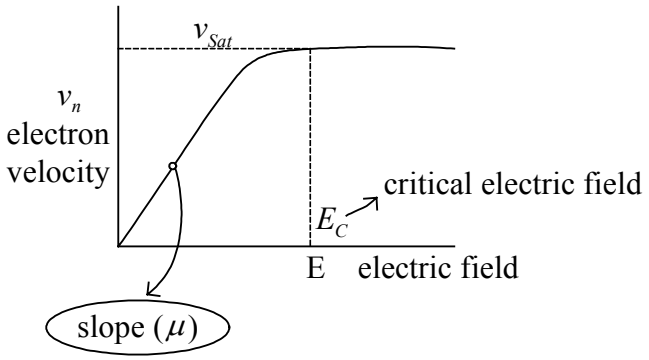
for small L (short channel)

V_{DS} ↕ ⟶ depletion region @ drain ↕ ⟶ Leff ↕

$I_D = I_D^{'}(1 + \lambda V_{DS})$ λ : channel length modulation factor

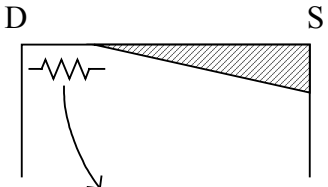
There are other problems with small size transistors :

velocity saturation

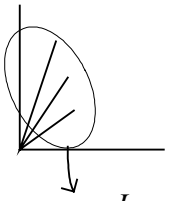


in small size transistors (sub-micron) E-field can be very large

velocity saturation effect starts @ drain part since there is higher electric field there



higher voltage drop
since it is more resistive

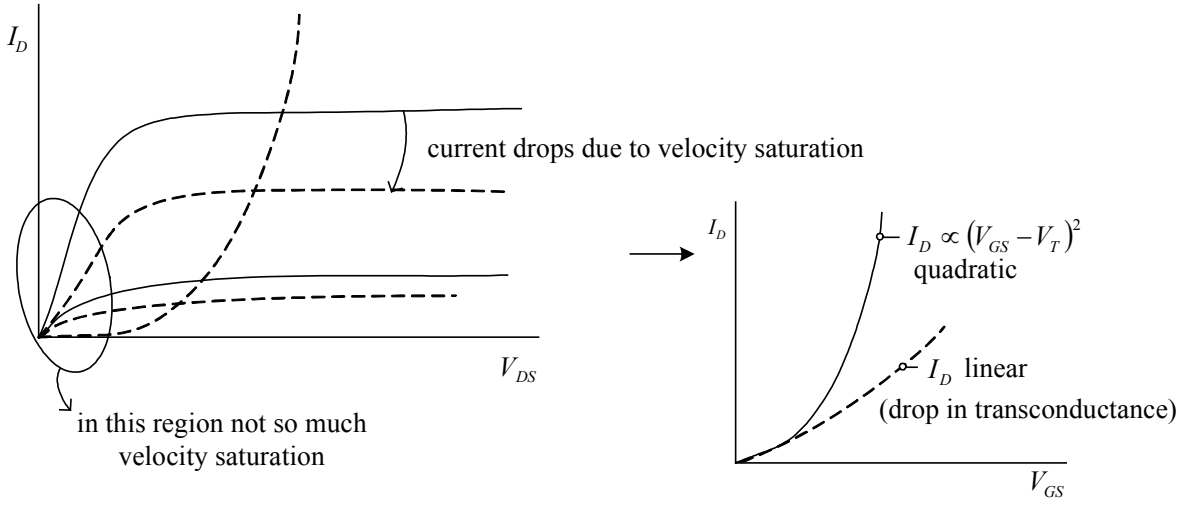


$$I_D = I_D' \underbrace{K(V_{DS})}_{\searrow \ < 1}$$

→ velocity saturation reduces the current

at $V_{DS} = V_{DSat} \Leftarrow$ on-set of velocity saturation

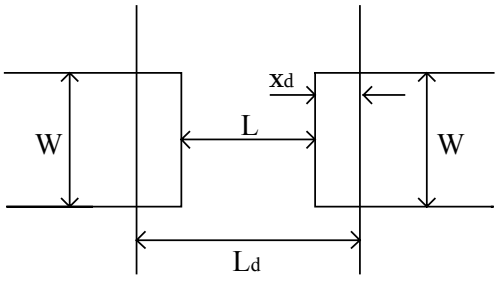
$$I_{DSat} = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_T)V_{DSat} - \frac{V_{DSat}^{\ 2}}{2}\right] \cdot K(V_{DSat})$$



Dynamic behavior

determined by various capacitor

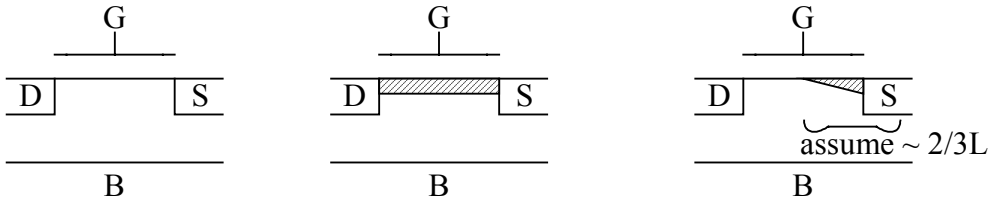
*** Overlap capacitance**



$$C_{GSO} = C_{GDO} = C_{ox} \cdot x_d \cdot W = C_o \cdot W$$

C_{gso}, C_{gdo} in spice model

*** Channel capacitance**



cut-off | resistive | saturation

$C_{GC} = C_{GCB}$ → gate-channel, body

$C_{GCB} = 0$

$C_{GC} = C_{GCS} + C_{GCD}$ (equal)

$C_{GC} = C_{GCS}$

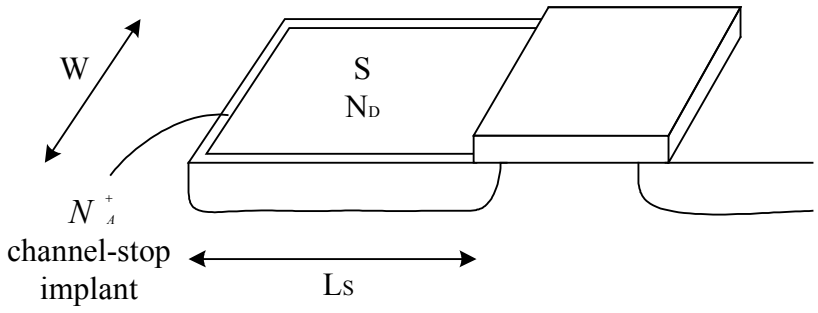
$C_{GCD} = 0$

$C_{GCB} = 0$

	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
cut-off	$C_{OX}WL$	0	0	$C_{OX}WL$	$C_{OX}WL + 2C_OW$
resistive	0	$C_{OX}WL/2$	$C_{OX}WL/2$	$C_{OX}WL$	$C_{OX}WL + 2C_OW$
saturation	0	$\frac{2}{3}C_{OX}WL$	0	$\frac{2}{3}C_{OX}WL$	$\frac{2}{3}C_{OX}WL + 2C_OW$

add overlap and channel capacitances

* **Junction capacitance** (diffusion capacitance) between source/drain and body

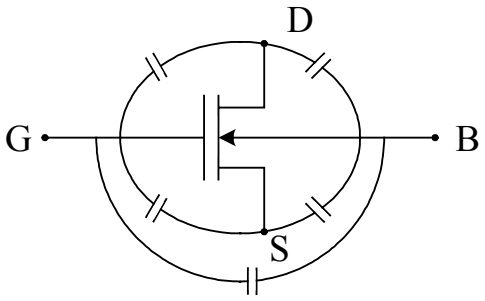


$$C_{diff} = C_{bottom-plate\,junction} + C_{sidewall\,junction}$$

$$= \underbrace{C_j}_{\text{cap/unit area}} \cdot area + \underbrace{C_{jsw}}_{\text{cap/length}} \cdot perimeter$$

$$= C_j L_s W + C_{jsw}(2L_s + W)$$

(L_s: length of source pad)



Various Capacitance Parameters

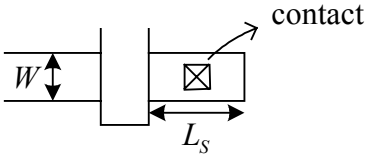
how cap varies with voltage

C_{OX} C_O	C_j m_j ϕ_b	C_{jsw} m_{jsw} ϕ_{bsw}
determine gate cap.	determine bottom-plate cap.	determine sidewall cap.

Source/Drain Resistance

$$R_S(R_D) = \frac{L_S}{W} R_{\square} + R_C$$

(R_C: contact resistance)



MOS Transistor Models

Spice models (non-linear model) :

Level I
Level II
Level III
} not suitable for sub-micron

BSIM version 3 → standard non-linear model now

Geometry related parameters

W, L, A_S, A_D, P_S, P_D, NRS, NRD

A_S, A_D: source & drain areas

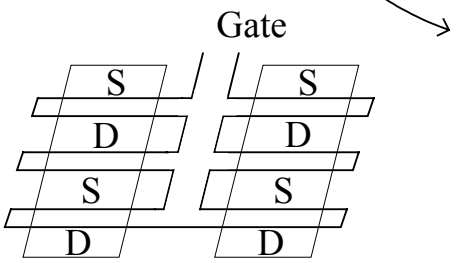
P_S, P_D: source & drain perimeter

NRS, NRD: # of squares in source & drain diffusion

For accurate parasitic source & drain resistance

MOS devices for RF application

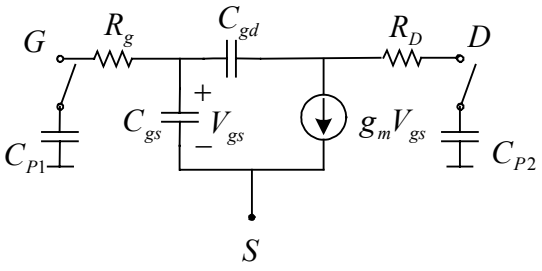
Generally use large transistors (multi-finger)



* to increase the current drive
* lower noise
* lower variations in device parameters

For the purpose of hand-calculation we also use small-signal incremental model

- valid for only one bias point
- varies as bias condition changes
- valid only when we have small-signal condition → nV ~ few mV range



Passive Components

* Resistors

- MOS transistor as a resistor

$$r_{ds} = \frac{1}{\mu C_{OX} \frac{W}{L}\left[(V_{GS} - V_T) - V_{DS}\right]}$$

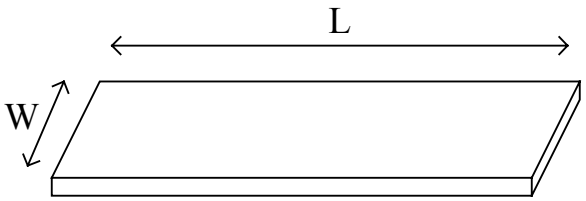
high temp coefficient

non- linear

loose tolerance

n+, p+

- metal, poly-Si, diffusion layer as resistor



$$R = \frac{L}{W} R_{\square}$$

sheet resistance of the layer

$R_{\square}$ can be anything between $0.01\Omega/\square \sim 100\Omega/\square$

Most resistors are PTAT (Proportional To Absolute Temperature)

$$R(T) = R_O \frac{T}{T_O}$$

Al for instance $R_{\square} = 50m\Omega/\square$

TC = temp coeff. = 3900 ppm/ °C ppm: part per million

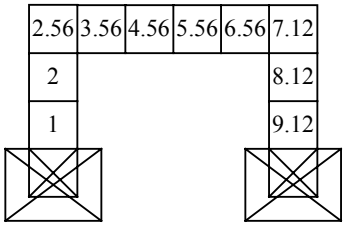
TC: varies little with temp -55 °C~125 °C

Therefore: $R(T) = R(300K)\left[1 + (T - 300K) \times 3.9 \times 10^{-3}\right]$

- Counting squares

$$R = \frac{L}{W} \times R_{\square}$$

# of squares

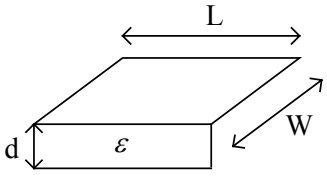


$R = 9.12 \times R_{\square}$

*** Capacitors**

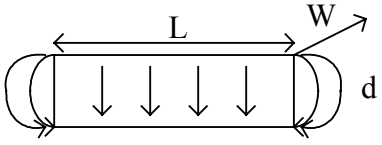
parallel plate

$$C = \varepsilon \frac{W \cdot L}{d}$$



$\frac{cap}{area} \sim 10^{-5}\ pF/\mu m^2$

when the size of capacitor plate becomes small fringing field become important:



1st approximation add 2d (1*d on each side) to W and L

$$C = \varepsilon \frac{(W + 2d)(L + 2d)}{d} = \varepsilon\left(\frac{WL}{d} + 2W + 2L\right)$$

$TC \sim 30 \sim 50\ ppm/^{\circ}C$ varies because of ε

You can also use MOS gate capacitor

(gate capacitance) $\longrightarrow 1 \sim 5 \; {fF}/{\mu m^2}$

gate cap is 20 ~ 100X larger than parallel plate cap.

MOS Cap has small positive TC ~ 30 ${ppm}/{^\circ C}$

when using gate capacitance → Transistor should be in strong inversion

$V_{GS} \rangle\rangle V_T$

Otherwise capacitance will be small, lossy and non-linear

Diffusion Capacitance → junction Cap

P+ region / n-well

→ C varies with applied bias → variable capacitance → reactor

→ Varactor

$$C_j = \frac{C_j}{\left(1 - {V_F}/{\phi}\right)^n}$$

→ abrupt junction n=1/2
linearly graded junction n=1/3

built in potential ~0.7V

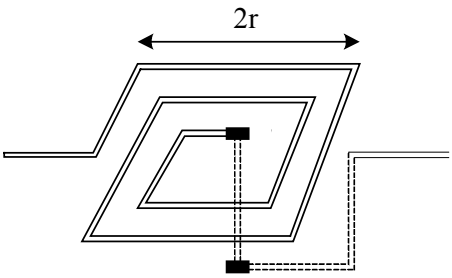
junction caps have large temp coeff.

$\sim 200 \; ppm/^\circ C$ reversed bias

$\sim 1000 \; ppm/^\circ C$ ~ zero bias

Q of varactor ↓ as C ↑

*** Inductors**



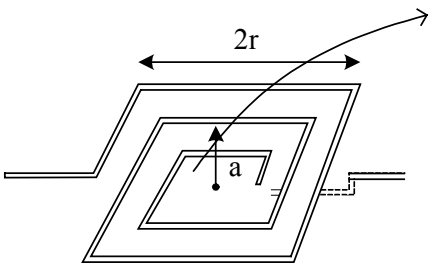
$\mu_0 = 4\pi \times 10^{-7}$

$L \approx \mu_0 n^2 r$

→ foot print of square inductor

number of turn

most often to keep the quality factor high you do the following



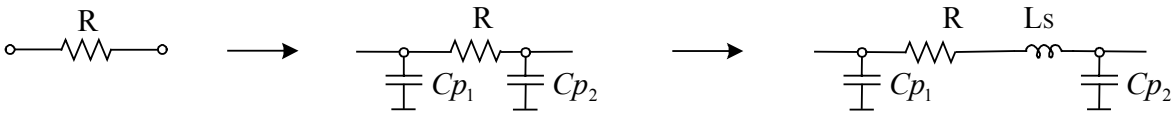
You don't continue to center as you don't gain much inductance but add loss → Q↓

a: square spiral's mean radies

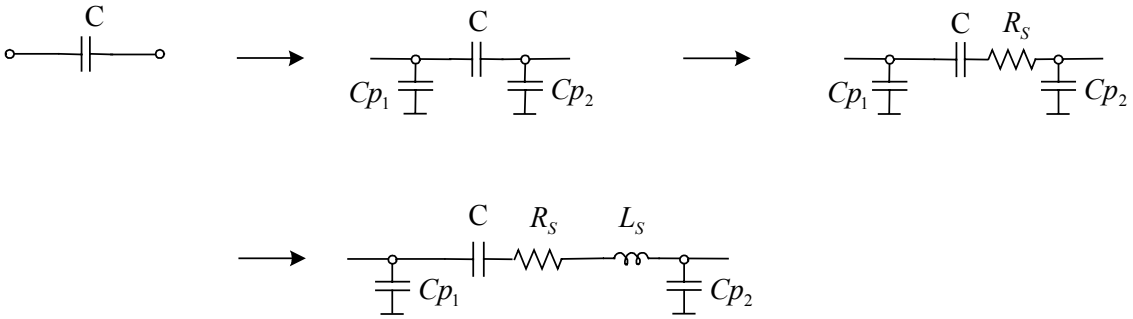
$$L = \frac{37.5\mu_0 n^2 a^2}{22r - 14a}$$

Model for passive components

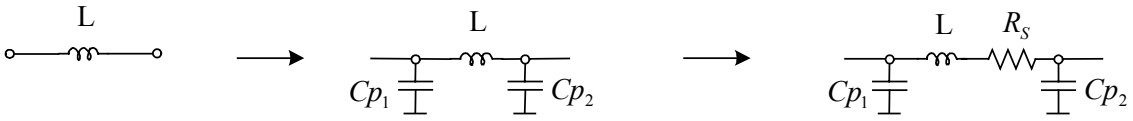
Resistor



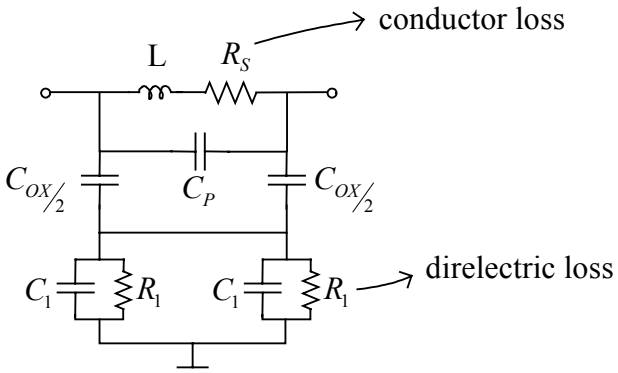
Capacitor

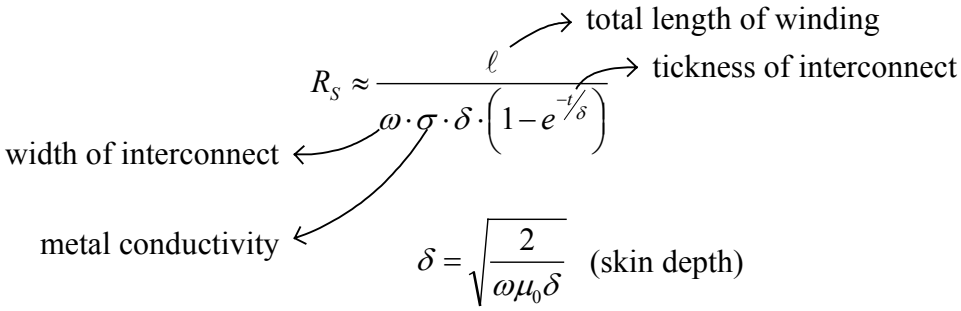


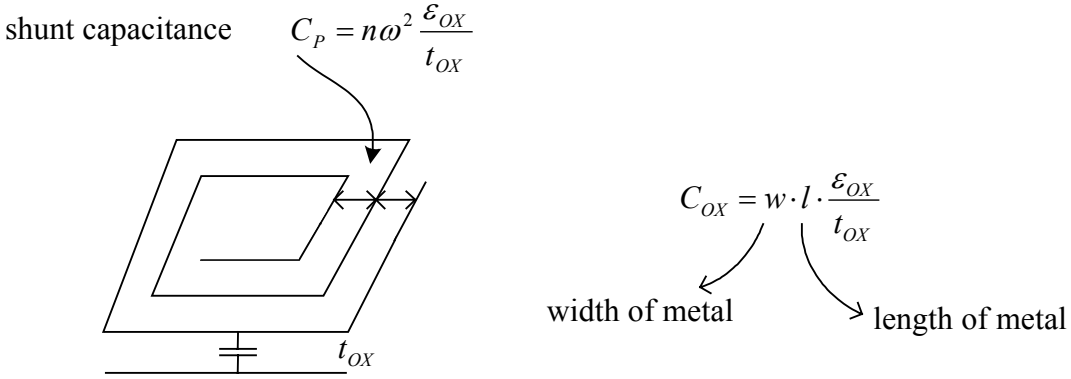
Inductor



- loss in dielectric (Si)
- interwire capacitance
- oxide capacitance







R_1 : shows the loss associated with current flow in the substrate

$$R_1 = \frac{2}{w \cdot l \cdot G_{sub}}$$ → fitting param (conductance/area)

$$C_1 = \frac{w \cdot l \cdot C_{sub}}{2}$$ → fitting parameter (capacitance/area)