Low Noise Amplifiers

Example

An NMOS transistor has been measured at 4 GHz under the bias condition $(V_{DS} = 2.5V \quad , \quad I_D = 4\,mA)$

measured S-parms

$$S_{11} = 0.552\angle 169°$$
$$S_{12} = 0.049\angle 23°$$
$$S_{21} = 1.681\angle 26°$$
$$S_{22} = 0.839\angle -67°$$

measured noise characteristics

$$F_{\min} = 2.5\,dB$$
$$\Gamma_{opt} = 0.475\angle 166°$$
$$R_n = 3.5\,\Omega$$

Design a low-noise amplifier with minimum noise figure

Step 1: determine the stability (we only have one point (4 GHz) ?)

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} = 1.01 \quad > 1$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.419\angle 111^\circ \quad < 1$$

→ transistor is unconditionally stable at 4 GHz

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(k - \sqrt{k^2-1}\right) = 14.7\,dB$$

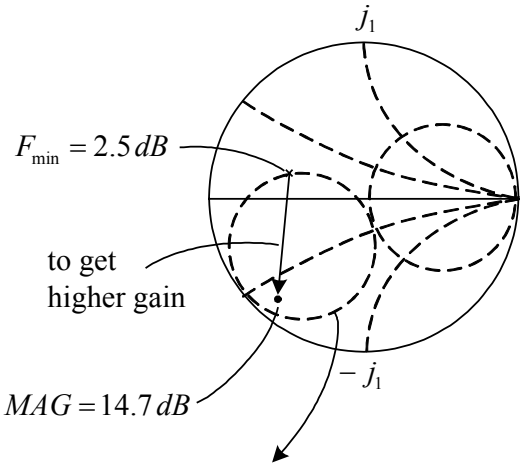
matching condition for achieving MAG

$$\Gamma_{S\,oft} = 0.94\angle -154^\circ \quad , \quad \Gamma_{L\,oft} = 0.98\angle 70^\circ$$

$\Gamma_{S\,oft}$: input matching to achieve highest possible gain

$\Gamma_{L\,oft}$: output matching to achieve highest possible gain

but F_{min} is obtained at $\Gamma_S = \Gamma_{opt} = 0.475\angle 166^\circ$



$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} = 0.844\angle -70°$$

substitute $\Gamma_S = \Gamma_{opt} = 0.475\angle 166^\circ$

↓

you can calculate G_A

$$G_A = 10.7\,dB$$

↓

4 dB gain degradation

Since R_n is small in this case, it could be better if you deviate from Γ_{opt} to get higher gain

never the less, let's stick to $\Gamma_S = \Gamma_{opt}$

now to get maximum gain you need $\Gamma_L = \Gamma_{out}^{\ *} = 0.844\angle 70°$

therefore $\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_\Gamma} = 0.744\angle 157°$

All you need to do is to design the matching network to show

$\Gamma_S = 0.475\angle 166^\circ$ at 4 GHz

$\Gamma_L = 0.844\angle 70^\circ$

either use transmission lines or passive components (L & C)

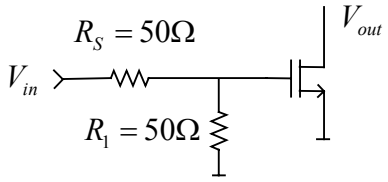
to design the matching network. Why?

1) → Because of stability concerns, you need to use narrowband approach ⟶ therefore L's and C's or transmission lines

2) → Adding resistors to the LNA basically adds up to the noise

example

consider the following circuit at 4 GHz



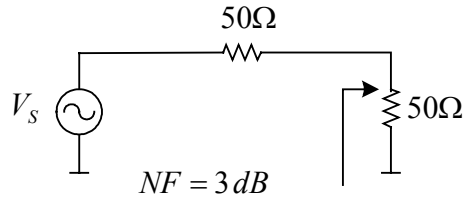
Advantage

Adding $R_1 = 50\Omega$ provides a very good match at input especially at low frequency (broadband match)

Disadvantages

① The power that goes to the transistor now has to pass a voltage divider
Therefore your total gain would be much less than the case without R_1

② R1 adds at least 3 dB noise figure to your circuit

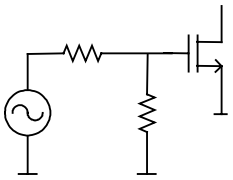


③ because of broadband match now you have problem with stability at frequencies < 4 GHz

Therefore never use resistors in LNA design unless

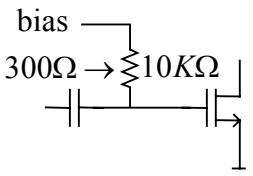
1. for broadband design → but understand that you can never achieve F_{min}

example ←



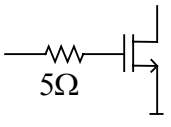
2. for biasing → high value shunt resistors can be used for biasing without much degradation in the noise performance

example ←



3. for stability → sometimes you need to sacrifice gain/noise figure for stability in this case you may have to use resistors

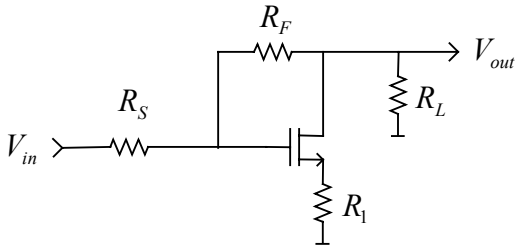
example ←



Broadband (wideband) low noise amplifier design

There is basically no good approach as your noise degrades by adding resistors

- one popular circuit is shunt-series amplifier



* Problem is Z_{opt} changes with frequency, so it is extremely difficult to get a match to Z_{opt} for a circle range of frequencies

2nd problem : R_F and R_1 introduce thermal noise

* change Z_{opt}

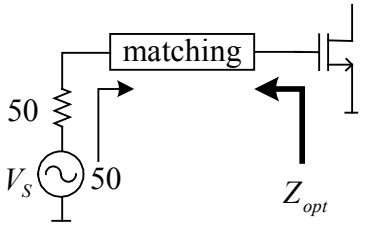
* increase F_{min} to values much higher than $F_{min}\big|_{transistor}$

Narrowband LNA design

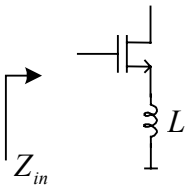
first lesson ⟶ do not use resistors !!?

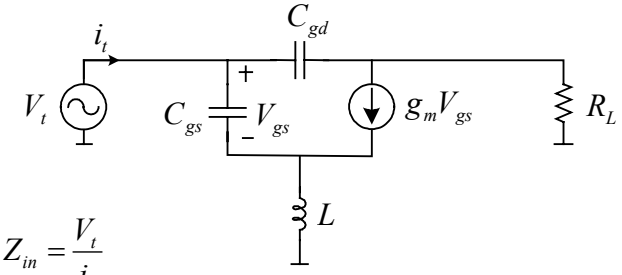
how? ⟶ if you have a $Z_{opt} = R_{opt} + j\,X_{opt}$, you can always match to X_{opt} using inductors + capacitors , but what about matching to R_{opt}

* impedance transformation



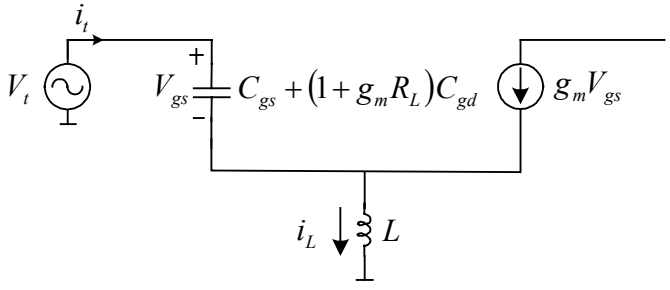
* use inductive degeneration





$$Z_{in} = \frac{V_t}{i_t}$$

$\approx$



$$i_L = \underbrace{V_{gs}\left(C_{gs} + (1 + g_m R_L) C_{gd}\right) \cdot j\omega}_{= i_t} + g_m V_{gs}$$

$$V_t = i_L \cdot j\omega L + V_{gs}$$

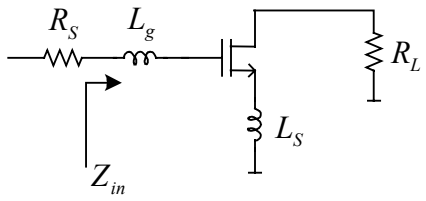
$$Z_{in} = \frac{V_t}{i_t} = \frac{V_{gs} + jL\omega\left(C_{gs} + C_{gd}\left(1 + g_m R_L\right) + j\omega V_{gs} + g_m V_{gs}\right)}{\left(C_{gs} + C_{gd}\left(1 + g_m R_L\right)\right) j\omega V_{gs}}$$

$$= \frac{1}{j\omega\left(C_{gs} + C_{gd}\left(1 + g_m R_L\right)\right)} + \frac{g_m L}{C_{gs} + C_{gd}\left(1 + g_m R_L\right)} + j\omega L$$

capacitive — resistive — inductive

you can use this to match the resistance to what you need but that would fix your inductive term

* need additional degree of freedom

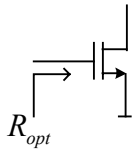


$$Z_{in} = \frac{1}{j\omega\left(C_{gs} + C_{gd}\left(1 + g_m R_L\right)\right)} + \frac{g_m L_S}{C_{gs} + C_{gd}\left(1 + g_m R_L\right)} + j\omega\left(L_S + L_g\right)$$

L_S ⟶ desired input resistance

L_g ⟶ desired inductance to tune out the capacitance at resonance

Remember



$$R_{opt} = \sqrt{r_g^2 + \frac{\delta}{\gamma}\frac{R_g}{g_m\left(1+\frac{C_{gs}}{C_{gd}}\right)^2}}$$ ← mos optimum source resistance (assumption → no noise correlation)

$$\frac{\delta}{\gamma} \approx 2$$

$$R_g = r_g + \frac{1}{5\,g_m}$$

by providing the right Ls you can get $R_{in} = R_{opt}$

$$\rightarrow \quad \frac{g_m L_S}{C_{gs} + C_{gd}\left(1 + g_m R_L\right)} = \sqrt{r_g^2 + \frac{2\left(r_g + 1/5\,g_m\right)}{g_m\left(1+\frac{C_{gs}}{C_{gd}}\right)^2}}$$

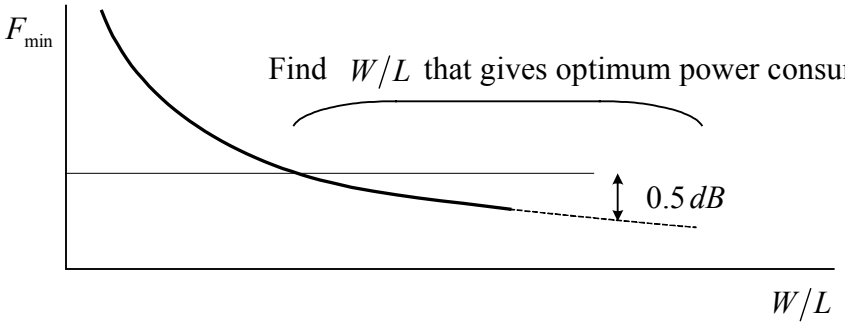
find Ls

but there is another parameter that you can very

↳ transistor size (W/L) ⟶ typically $\frac{W}{L}\uparrow$ ⟶ $F_{\min}\downarrow$

so to minimize F_{min} ⟶ you need very large size transistor

which means large power consumption



Since power consumption is important, you have to find W/L ratio that gives you lowest power consumption yet very good F_{min}, and gain

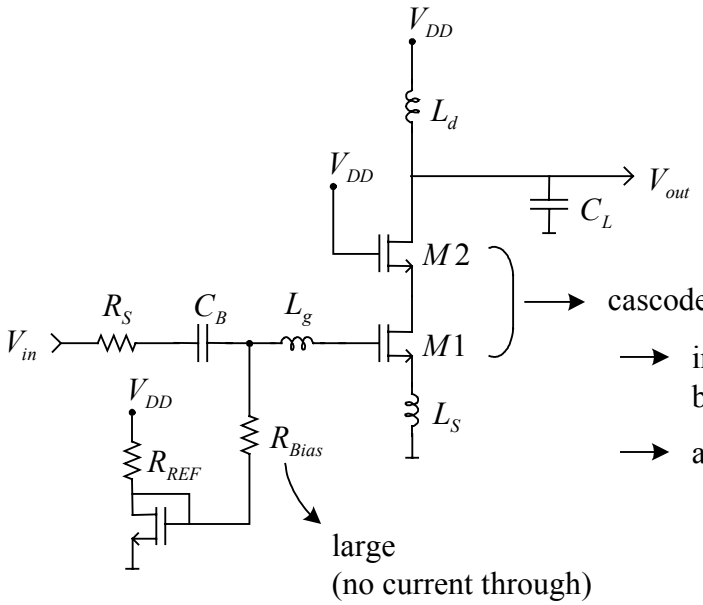
Turns out that there is a W/L ratio that will give you optimum power performance (high-gain) yet reasonable F_{min}

$$\left.\frac{W}{L}\right|_{opt,\,P} = \frac{1}{3\omega L^2 C_{OX} R_S}$$

the resistance you try to match to, typically $50\,\Omega$

⟶ LNA design

Single-ended LNA



cascode pair is used to reduce S_{12}

→ input and output matching become independent

→ also for better stability

$$R_L\Big|_{M1} = \frac{1}{g_{m2}} \approx \frac{1}{g_{m1}}$$

Resistance component for cascode

Optimum source matching

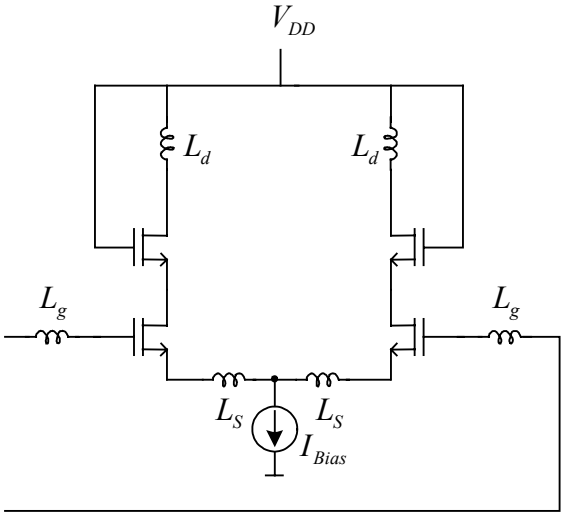
$$\frac{g_m L_S}{C_{gs} + 2C_{gd}} \approx \frac{\sqrt{2/5}}{g_m\left(1 + C_{gs}/C_{gd}\right)}$$

Assume $C_{gs} \approx 3C_{gd}$

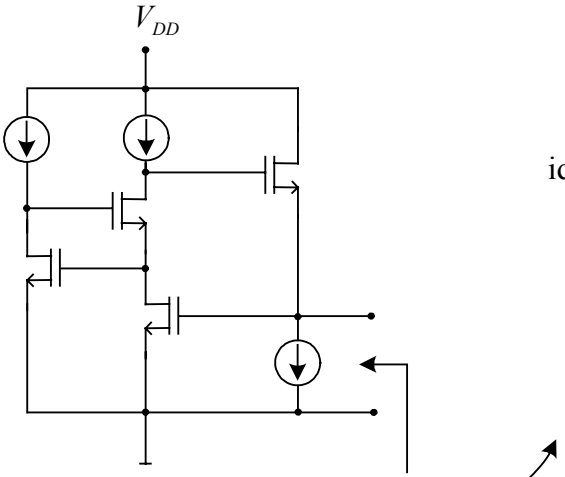
$$L_S = \frac{\sqrt{2/5}}{g_m^2} C_{gs} \times \frac{5}{12} \approx \frac{C_{gs}}{4g_m^2}$$

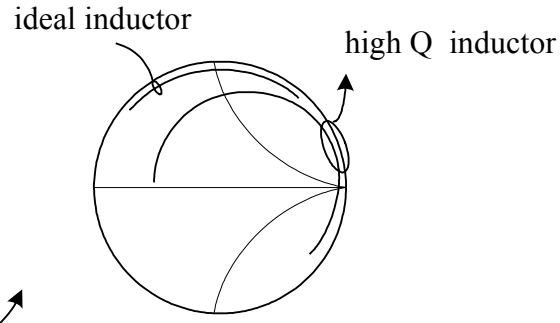
$$L_S \approx 14\,pH \qquad for \qquad \frac{W}{L} = \frac{100\,\mu}{0.18\,\mu}$$

Differential LNA



CMOS LNA's reported in literature





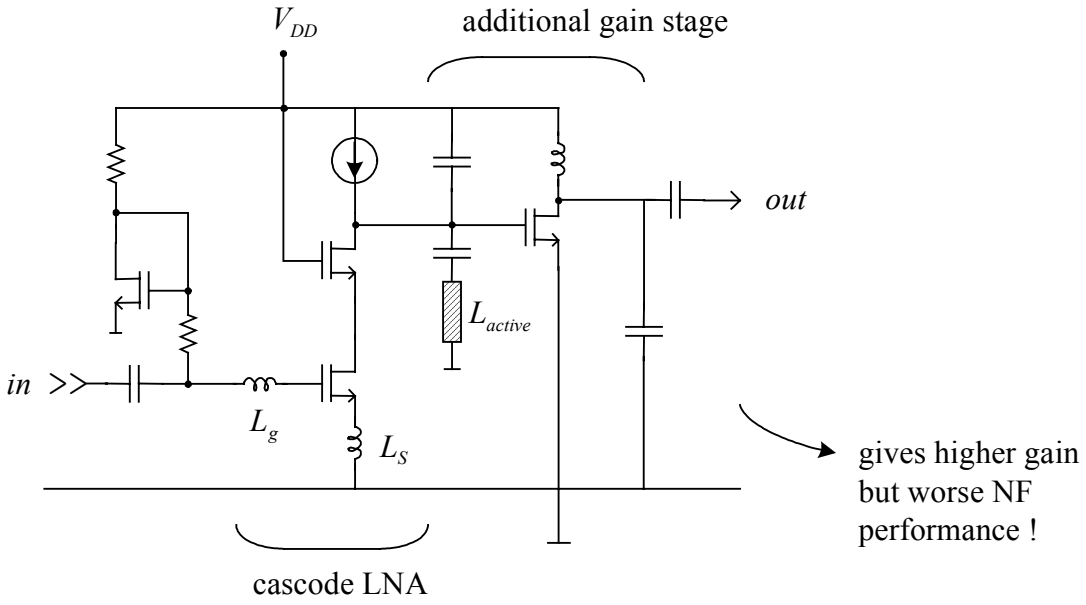
active inductor inductive

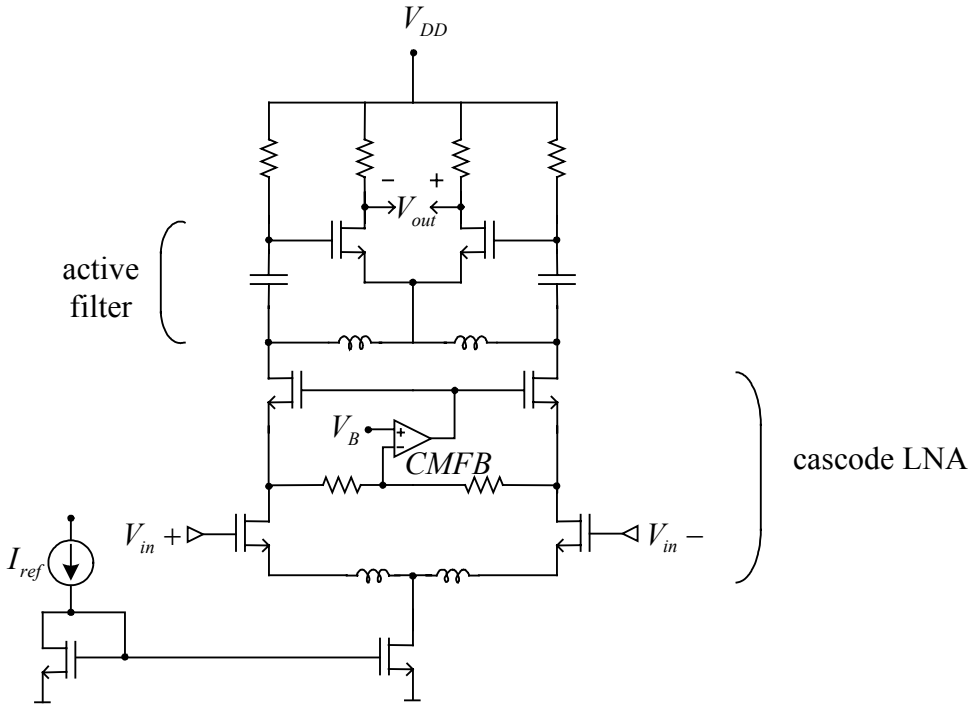
based on gyrator

$Q \sim 60$ $L \sim 10 \sim 90\,nH$!!

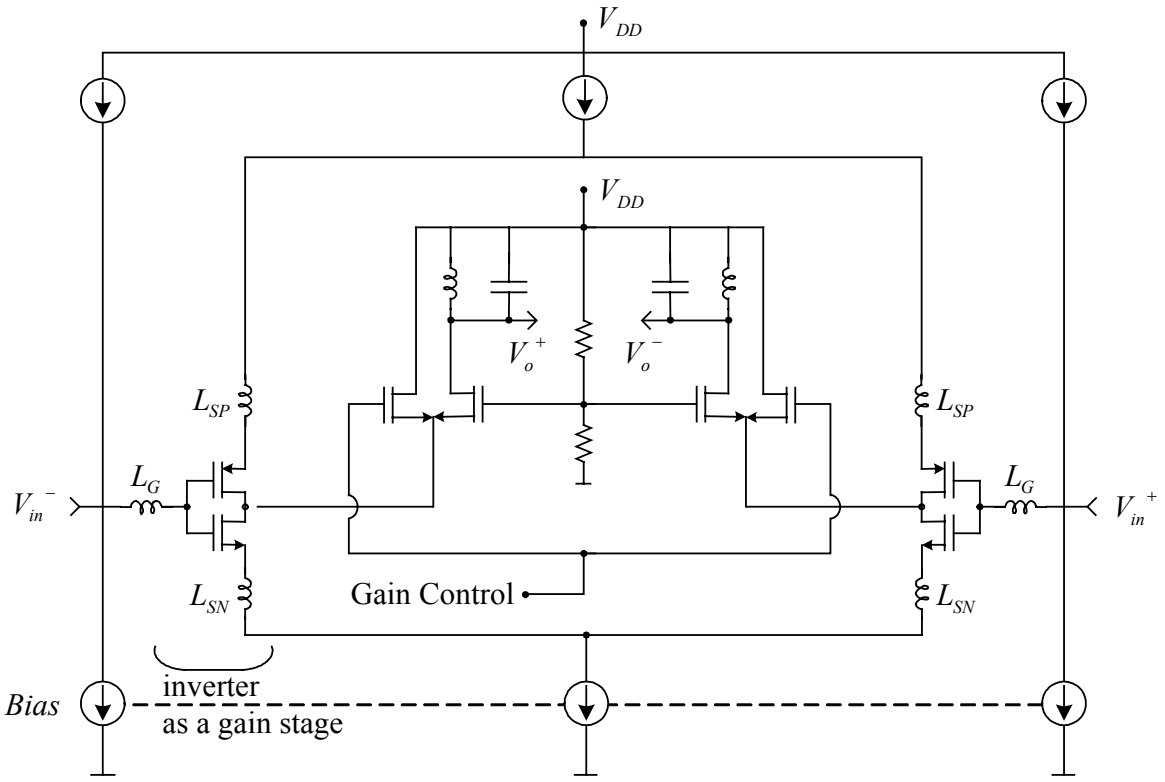
high Q , high inductor values, tunable

bad noise performance
consume power → 90% less die area!


V_{DD}
additional gain stage
out
L_{active}
in
L_g
L_S
gives higher gain
but worse NF
performance !
cascode LNA


V_{DD}
V_{out}
active
filter
V_B
CMFB
cascode LNA
$V_{in}+$
$V_{in}-$
I_{ref}

LNA-VGA
→ variable gain amplifier



Common-Gate LNA

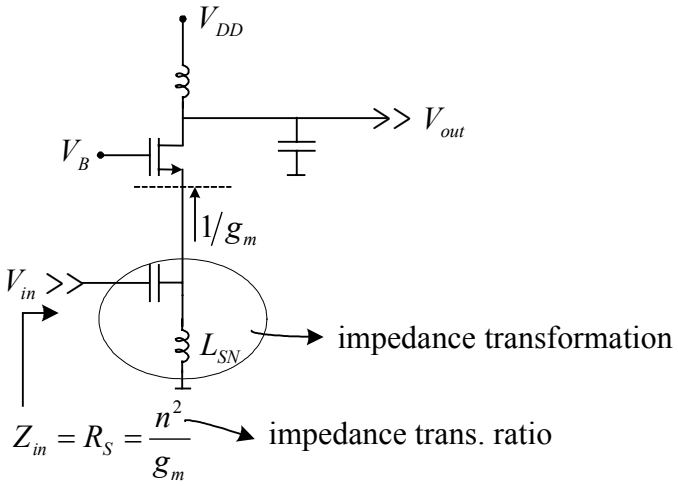
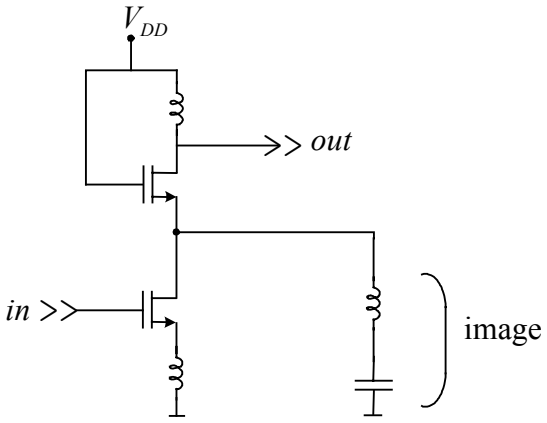
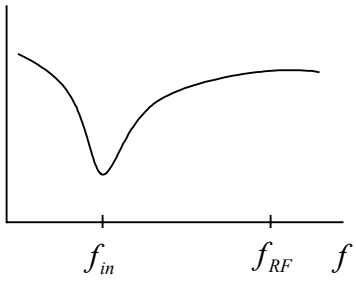
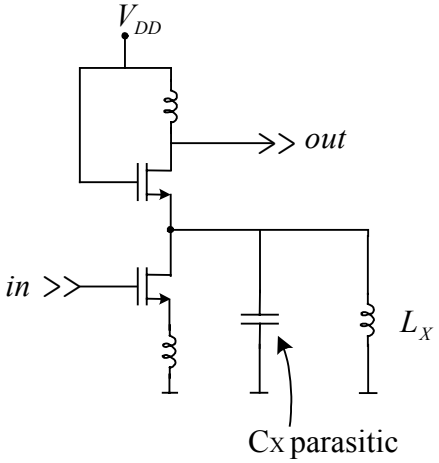


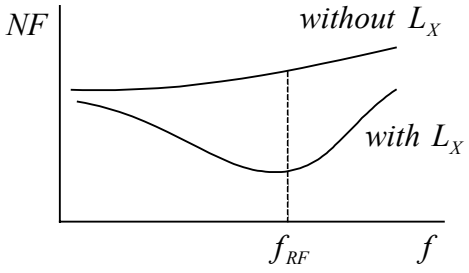
Image reject LNA





Improving NF of a standard LNA





Third-order filter

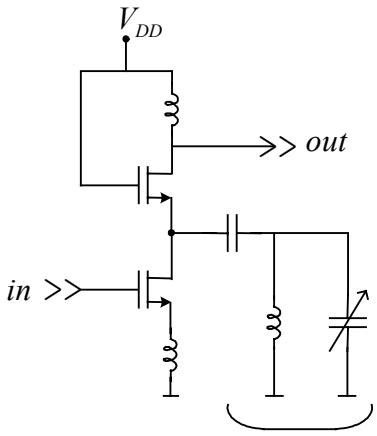


image rejection
+ improving NF in one shot

realization