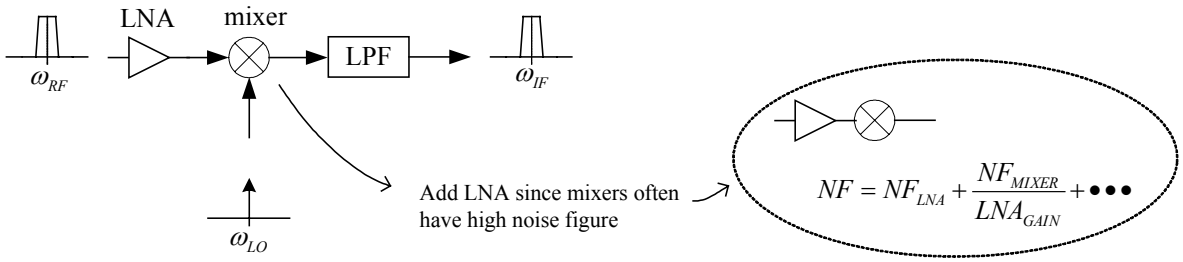
Transceiver Architectures

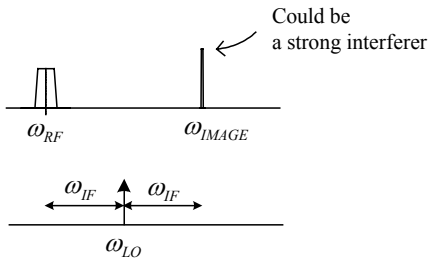
Receiver Architectures

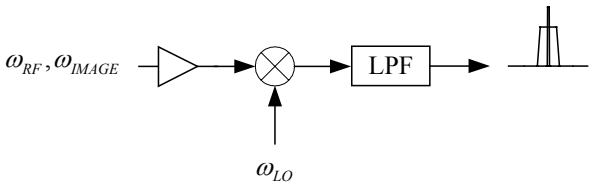
Heterodyne Receiver

→ Signal frequency is transferred to much lower frequency to relax the Q requirement for filter

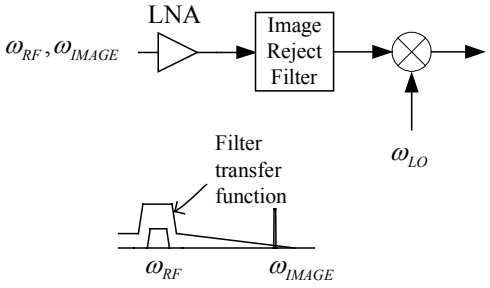


→ Problem of Image:
LO and IF are chosen by considering the image frequency





So the image frequency must be attenuated



If image is too close (Small IF) ⟶ realizing the filter (image-reject) would be difficult

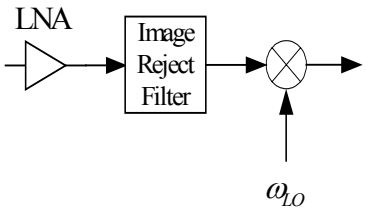
Large IF ⟶ Q of IF filter must be high $\left(\frac{channelBW}{IF} = \frac{1}{Q}\right)$

Channel selection becomes difficult

⟶ choice of IF is a trade-off among three parameters

- image noise
- spacing between desired band and the image
- loss of the image reject filter

Drawback of heterodyne ⟶ image reject filter is an external component

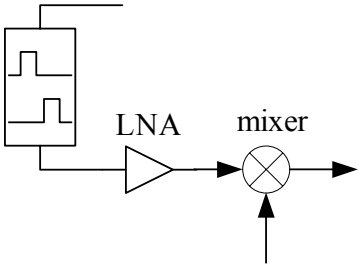


LNA must drive an external component (typically 50Ω)

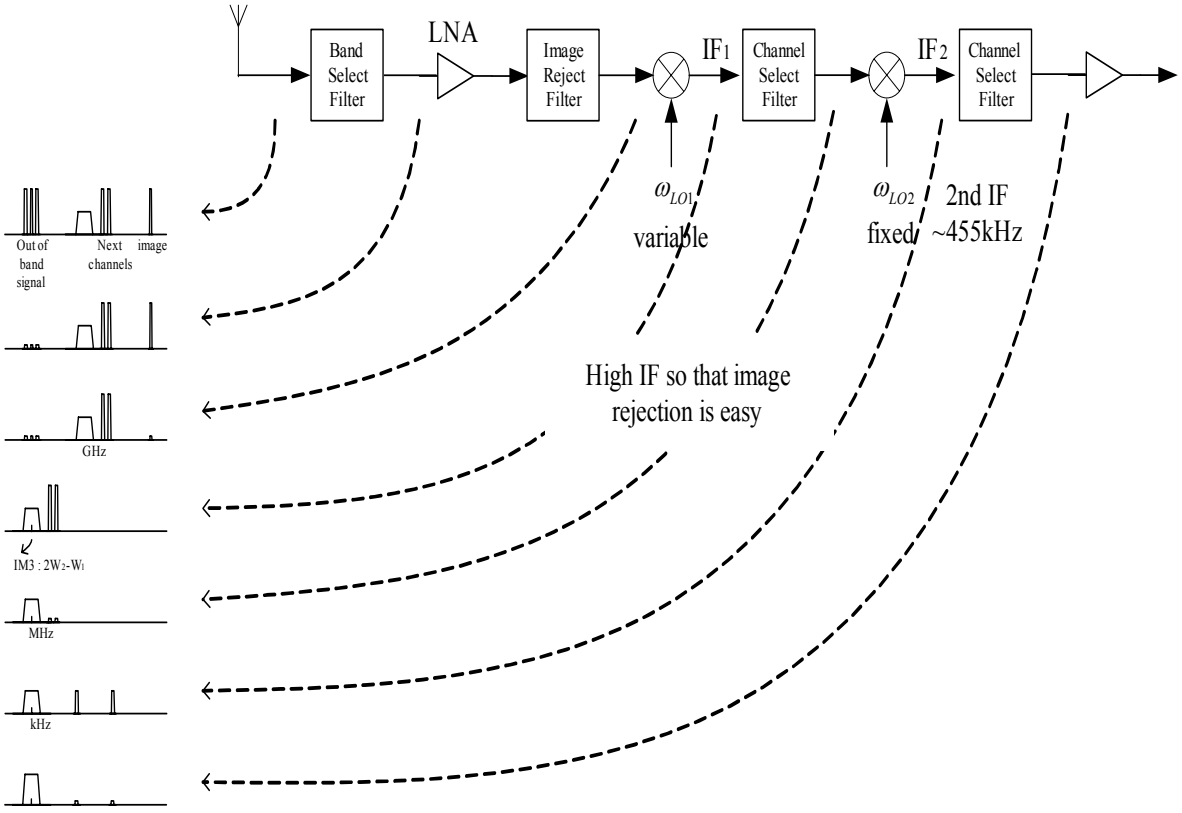
⟶
- lower gain
- higher noise figure
- stability problem
- higher power dissipation

In FDD system if IF is high enough

image can be removed using FDD filter ⟶ LNA can be connected directly to mixer



Use dual-IF topology to solve the problem of image



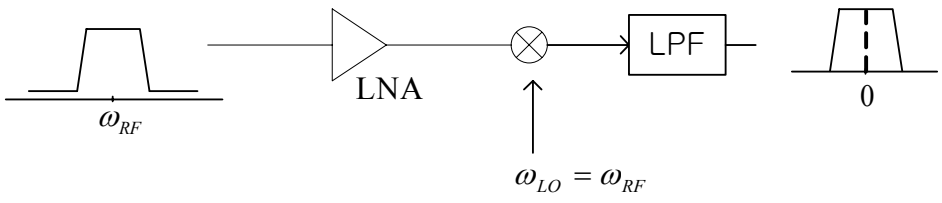
Homodyne Receiver (Zero-IF or Direct Conversion)

→ very simple (IF = 0)

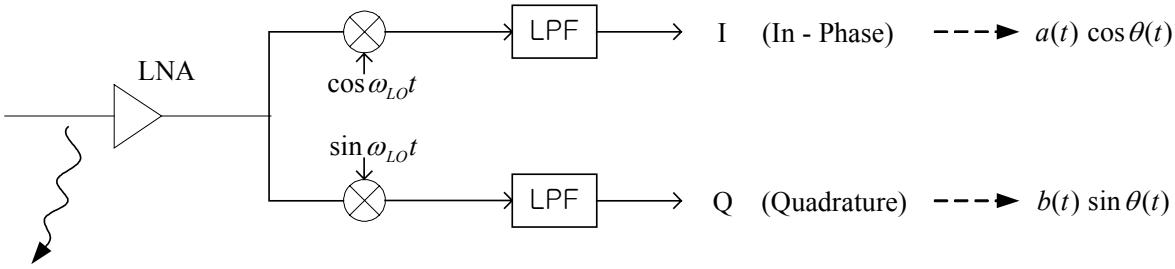
* There is no problem of the image frequency → Image filter is not needed

$\omega_{LO} = \omega_{RF}$

* No IF filtering is needed (need only low pass filters)

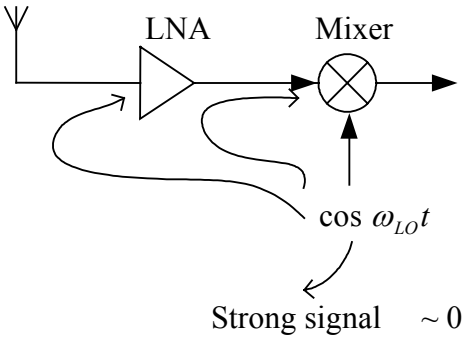


In case of phase or frequency modulation



$a(t)\cos(\omega_{RF}t+\theta(t))+b(t)\cos(\omega_{RF}t+\theta(t))$

<u>Problem with DC offset in zero-IF</u> → does not exceed in heterodyne as IF >> 0



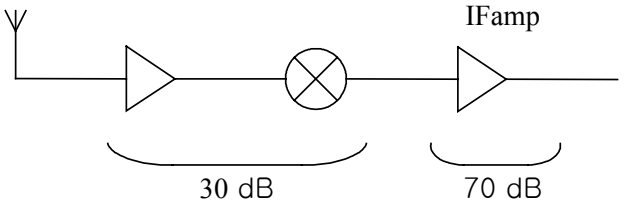
LO leakage to RF port causes
a DC offset term:

- Isolation between LO and RF ports of the mixer is not infinite
- Leakage from LO to antenna & input of the LNA (capacitive + substrate coupling)

- LO → 1mW (0 dBm) → on a 50Ω System: 0.63 V_{PP}
- LNA/Mixer gain ~ 30dB
- Isolation between LO and input of LNA ~ 60dB

→ generate ~ 10mV dc term

Signal level ~ 30μ Volt (rms)



→ With 70 dB more amplification the DC offset voltage saturates the receiver and de-sensities it to the RF signal

→ need DC offset cancellation: cannot use series capacitor to remove DC as usually there is a lot of information at DC

* for a 200 kHz GSM channel a high pass filter (series capacitor) with a cut-off of only 20 Hz increases the bit error rate (BER) to unacceptable level of 10^{-3}

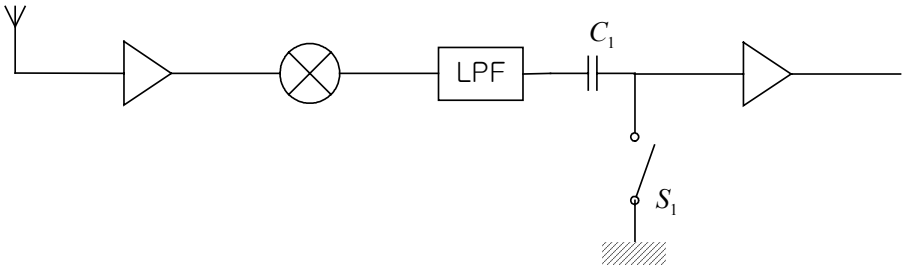
10^{-7} acceptible

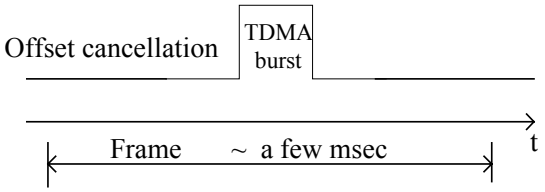
can be encoded signal so the spectrum is not at DC (called DC free coding)

* DC-free coding is suitable for wideband channels, for example DECT, a few kHz is insignificant

* often problem is as you drive, offset level varies with reflection from other cars etc → so it is not exactly DC offset

A better way is to use offset cancellation in digital wireless standard





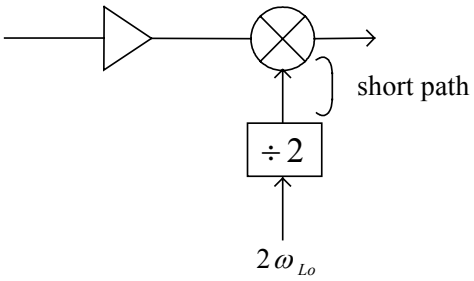
problems

C_1 ~ 200 PF (very large)

I/Q differential ckt
you need 4 of those

Interferes may be stored along with offset (interferers are present outside TDMA burst)

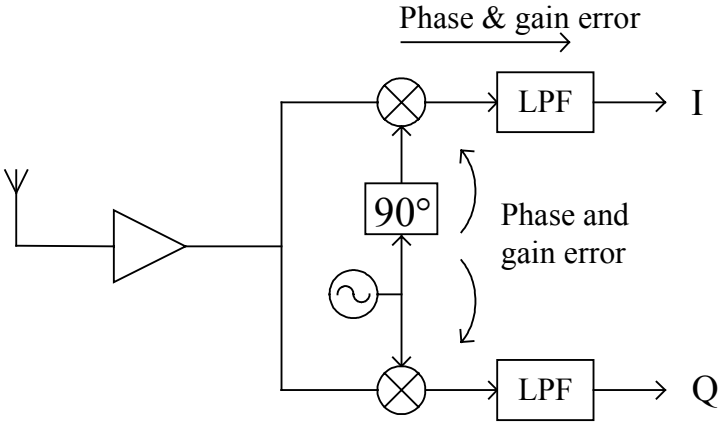
To reduce offset you can generate LO at double the frequency and then divide it locally



I/Q mis-match

→ need { gain error < 1dB
phase error < 5°

To do quadrature mixing



90° phase shift is achieved using an RC network
Loss/variation in R and C value results in both gain and phase error!

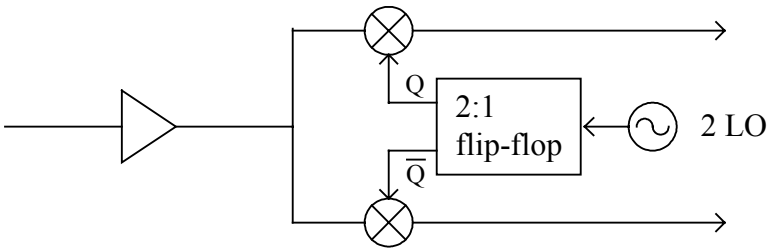
I/Q mismatch in heterodyne is not a problem → ① down conversion to I & Q occurs at IF and not RF

↓

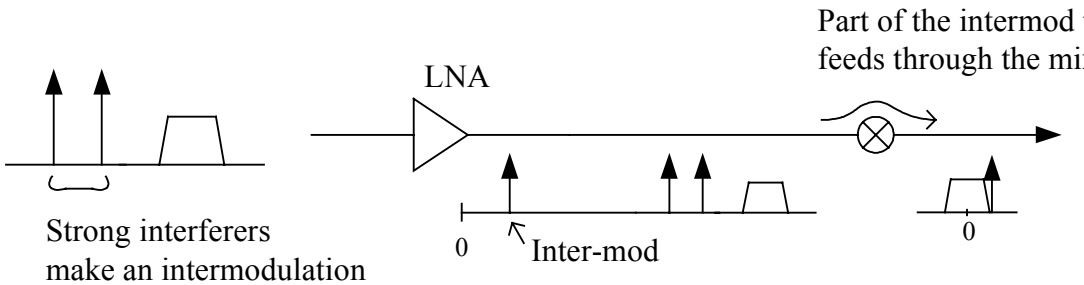
lower frequency → I/Q Paths are much less sensitive to mismatch
in IC design, lower frequency allows using longer devices that improves the matching in the I/Q parts

② in heterodyne signal is amplified by 50~60dB before I/Q separation
(one or two stage amplification afterwards)
in zero-IF signal needs another 50~60dB amplification 3~4 stages each increase the mismatch!
in monolithic integration I/Q mismatch is less device problem

Besides, instead of 90° phase amplifier use $2\omega_{LO}$ scheme



<u>Even-order distortion</u> : another problem of zero-IF



Strong interferers
make an intermodulation
term in the LNA due to its
non-linearity

→ You can use differential LNA and mixer to get rid of even-order term

↳ Problem: Antenna & duplexer are not differential

Because they must operate with single-ended power amplifier

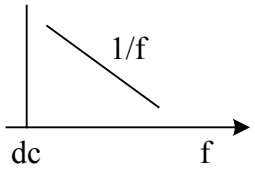
in the transmit path → Use transfomer

↳ extra loss of few ~dB

Differential LNA needs higher power to achieve comparable noise figure

Fliker Noise (1/f noise)

MOS devices often have large 1/f noise



To reduce flicker niose in stages subsequent to mixer

① → use large devices (low-frequency so you can do that)

② → periodic offset cancellation also lowers noise components below $1/T_C$ where T_C time b/w consecutive offset cancellation instances

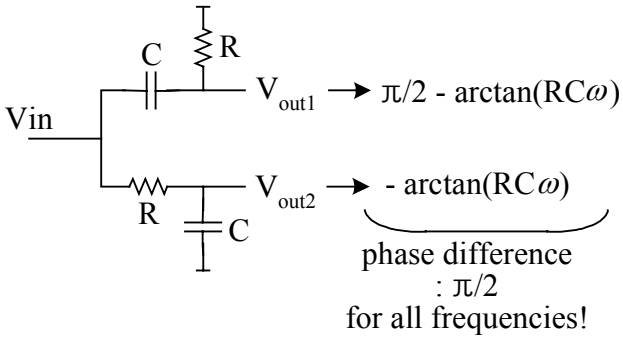
LO leakage

To antenna in bound LO radiation ~ -50 to -80 dBm

Direct conversion receiver is becoming more popular in new generation of wireless phones (it was the receiver of choice in pager systems)

Image Reject Receivers

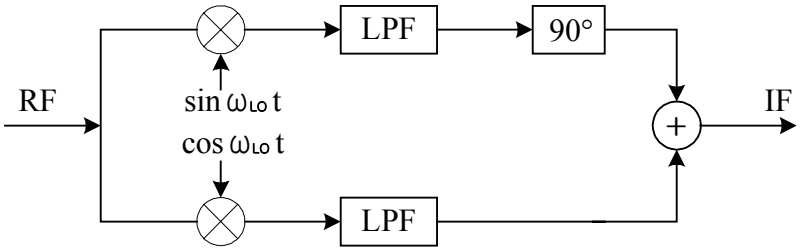
90˚ phase shift CKT:



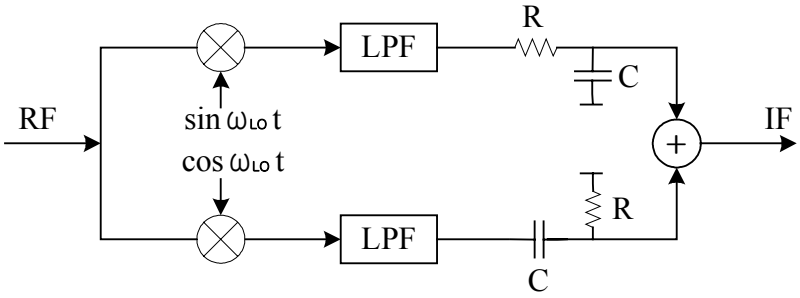
for sinusoidal input, phase shifts of V_{out1}, V_{out2} are equal to

idea is to process image frequency differently

Hartly Architecture



Using the 90˚ phase shift CKT:



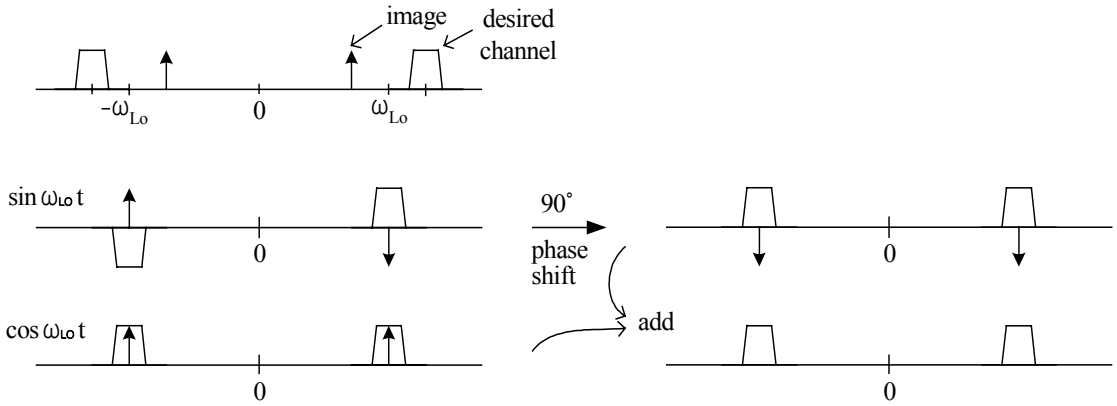


Image rejection is a function of relative gain and phase mismatch:

$$IRR = \frac{(\Delta A / A)^2 + \theta^2}{4}$$

Image Rejection Ratio

$\frac{\Delta A}{A}$ relative gain mismatch

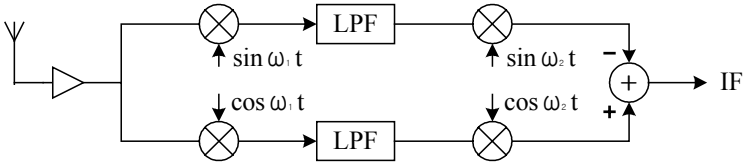
θ phase mismatch

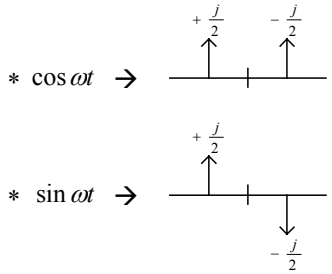
In Hartley architecture only at $\omega_{IF} = \frac{1}{RC}$ gains match!

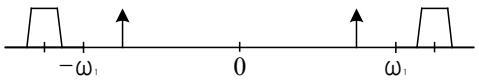
So deviation from ω_{IF} results in mis-match in gain paths

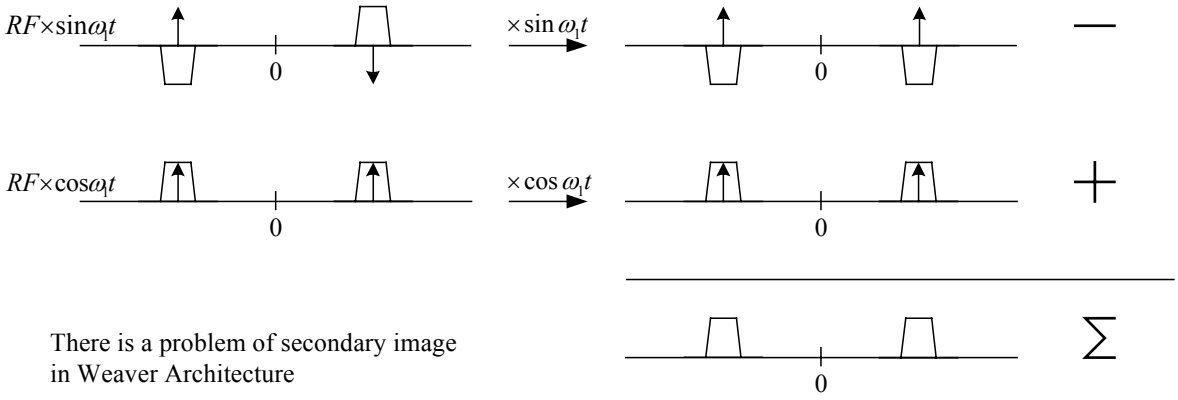
problems
- * → design is not easily integrable as you have RC omponents
- * → linearity of the adder imposes additional trade-off
- * → loss and noise of 90° phase shift is significent

Weaver Architecture

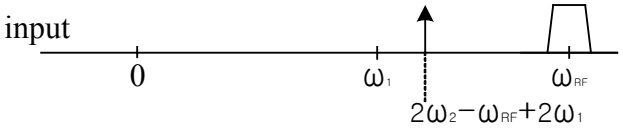


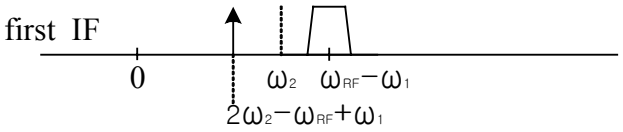


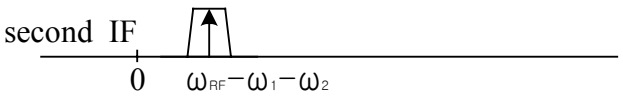




There is a problem of secondary image in Weaver Architecture

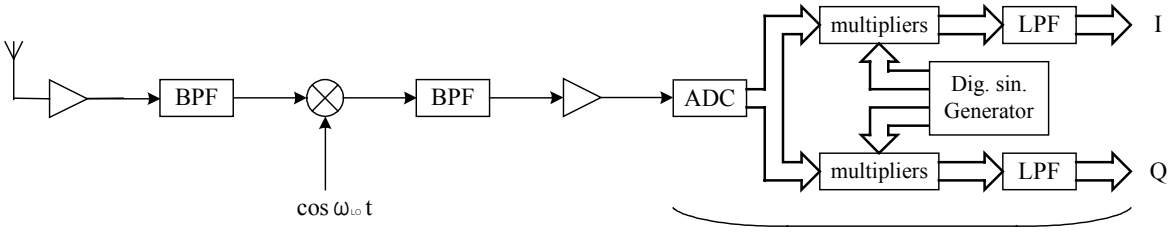






To solve the problem replace LPF with BPF(Band Pass Filter)

Digital IF Architecture



Digital Signal Processing

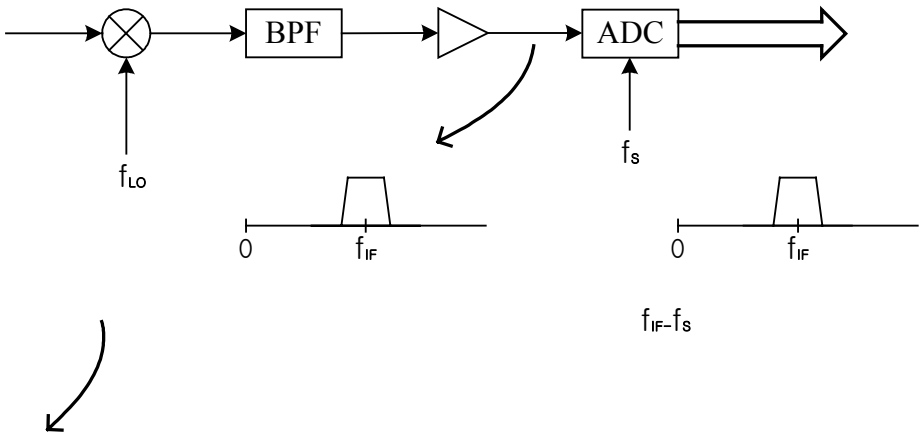
ADC dynamic range must be wide enough to accommodate variations in signal level due to path loss and multi-path fading

at ω_{IF} need 14dB resolution

difficult to realize

Most ADC do sample and hold ⟶ which is basically a down conversion

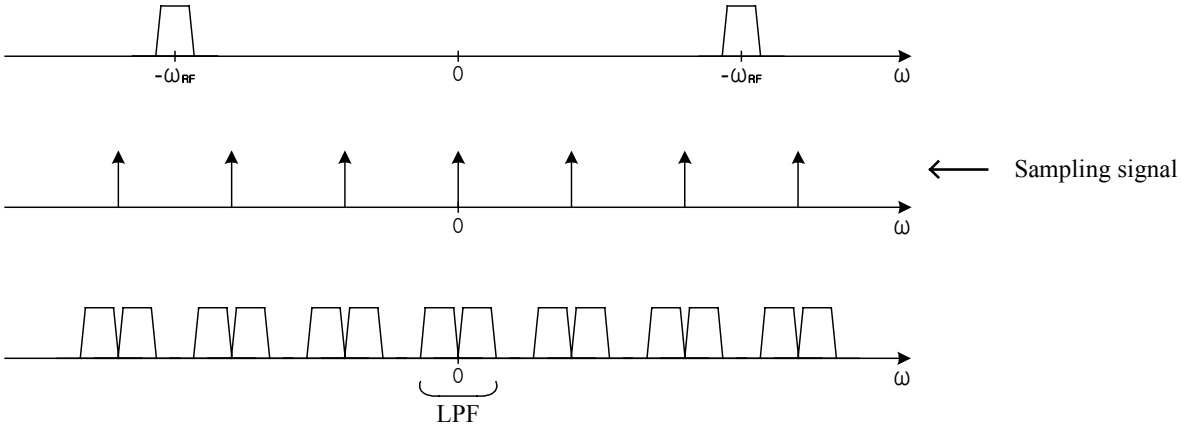
Sampling IF Architecture



Reduing sampling rate by a factor of ~2
but still need high (speed) / (high lilnearity)

Subsampling Receivers

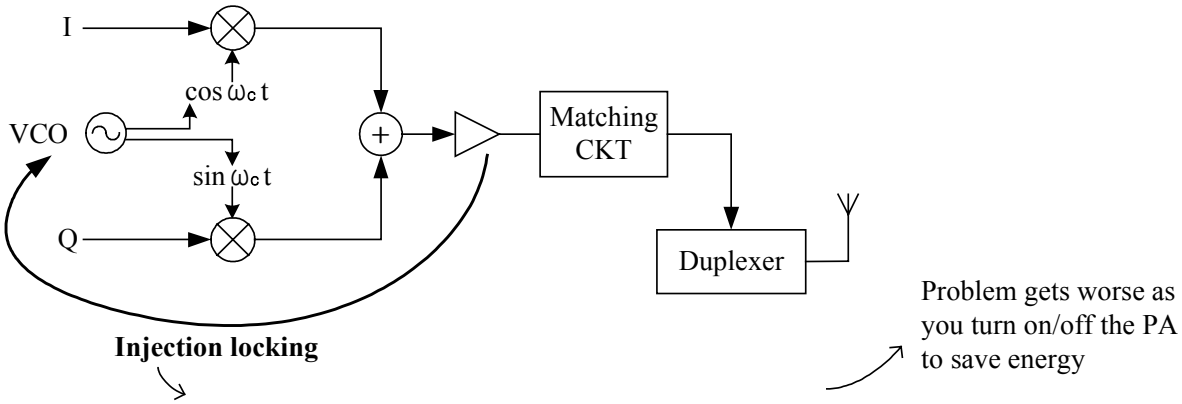
Sample the signal at a much lower rate
(since the RF is almost periodic sine signal with small variations)



Transmitter Architecture

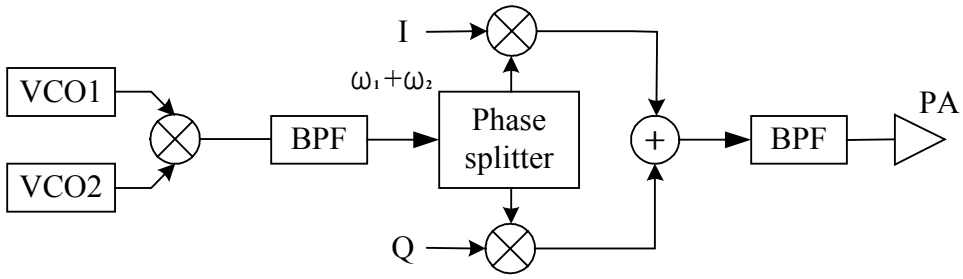
Direct Conversion Transmitter

→ modulation and up-conversion occur in the same circuit



Problem since spectrum of modulated signal at the output of Power Amplifier ruins VCO's clean signal

To solve the problem use mixing of two VCO signals



Direct conversion transmitter with offset LO

Another way to solve the problem of injection locking is to use two-step transmitter