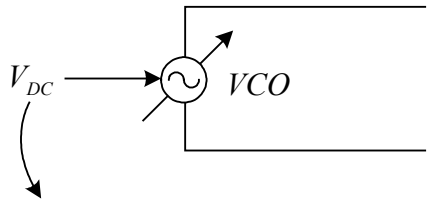
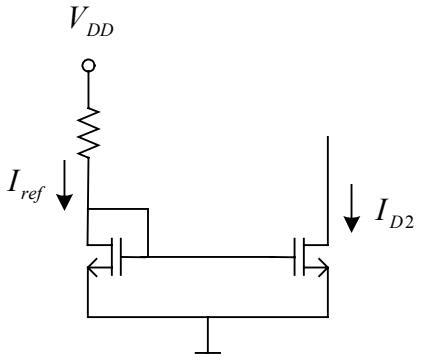
Current & Voltage References

why do we need voltage/current reference



if this V_{DC} varies as your power supply varies, you are in trouble

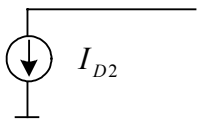
Current Sources



neglecting finite output resistance

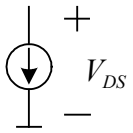
$$I_{D2} = I_{D1} = I_{ref}$$

since both transistors have same V_{GS}



→ what you need as a current reference is a current source

* I_D does not change with changing V_{DS2}
(infinite output resistance)
R_O



* I_D does not change with temperature

* There is always a gain error $\left(I_{D2} / I_{ref} = 1 \right)$

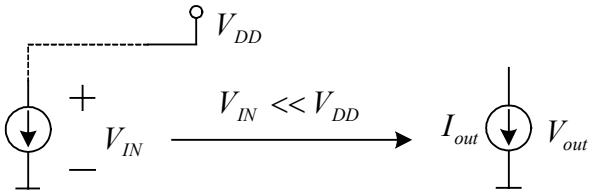
1) systematic gain error → you can calculate it as due to ckt topology you have slight gain error

2) random gain error

due to process variation → transistor mismatch in V_{Th}
→ can do only statistical analysis

* current sources always create a positive voltage drop (V_{IN})

→ we want to minimize V_{IN} especially for low-bias application

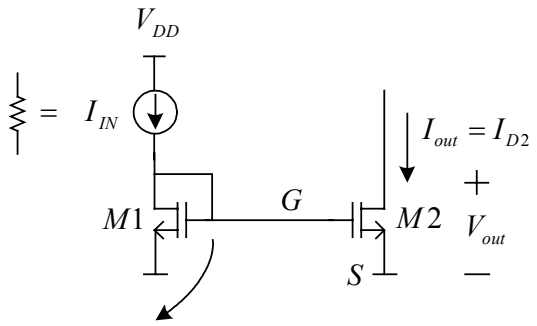


sometimes we use more than one input terminal
(cascode current mirror) to be able to operate
at low V_{DD}

* A positive output voltage V_{out} is needed such

that $I_D \sim I_{ref}$ → $V_{out\,\min} \downarrow$ → maximize range of output voltage
at which $R_0 \approx const$

Simple Current Mirror



$$V_{GS2} - V_{Th} = \sqrt{\frac{2I_{D2}}{k'\left(\frac{W}{L}\right)_2}}$$

often we say this is a diode connected transistor (while there is no diode when you short-ckt MOS drain to gate!)

k' : transconductance parameter $\sim \mu$

$\mu \downarrow$ *as* $T \uparrow$

so I_D is a function of temperature

$$V_{GS1} = V_{GS2} \quad \Rightarrow \quad V_{Th1} + \sqrt{\frac{2I_{D1}}{k_1'\left(\frac{W}{L}\right)_1}} = V_{Th2} + \sqrt{\frac{2I_{D2}}{k_2'\left(\frac{W}{L}\right)_2}}$$

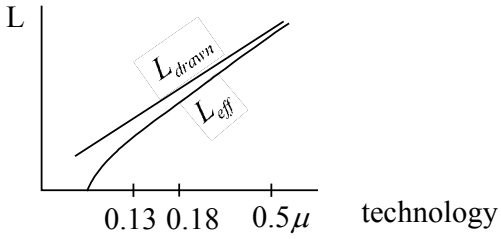
identical transistors : operating in active mode with infinite output resistance!

$$\left.\begin{array}{l} V_{Th1} = V_{Th2} \\ k_1' = k_2' \\ \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \end{array}\right\} \longrightarrow I_{D1} = I_{D2} \longrightarrow \boxed{I_{out} = I_{IN}}$$

In practice if devices are not identical

$$I_{out} = \frac{\left(W/L\right)_2}{\left(W/L\right)_1} I_{IN} \longrightarrow \text{transistors can be ratioed to get gain} \quad < \quad > \quad 1$$

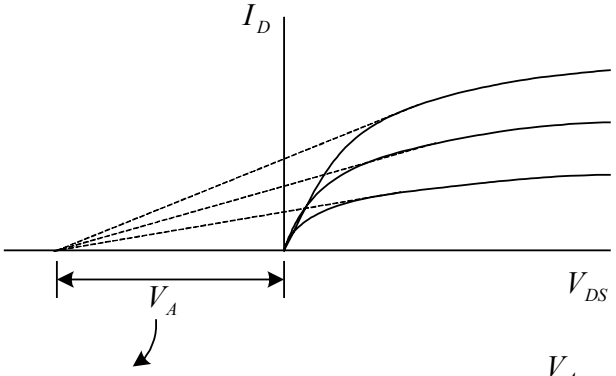
L'_S *as* L_{eff} *not* L_{drawn}



So far we assumed drain current is independent of drain-source voltage

In active region I_D increases as V_{DS} increases

this is characterized by output resistance



early voltage

$$R_O = \frac{V_A}{I_{D2}} = \frac{1}{\lambda\, I_{D2}}$$

we know this parm as channel length modulation factor

$$r_O = \frac{1}{\lambda\, I_D} = \frac{L_{eff}}{I_D}\left(\frac{dX_d}{dV_{DS}}\right)^{-1}$$

the good thing about MOS is that by increasing L (keeping W/L the same) you can improve output resistance

$$I_{out} = \frac{\left(W/L\right)_2}{\left(W/L\right)_1} I_{IN}\left(1 + \frac{V_{DS2} - V_{DS1}}{V_A}\right)$$

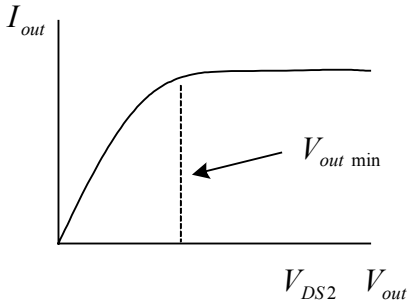
systematic gain error of a simple current mirror

$$\varepsilon = \frac{V_{DS} - V_{DS1}}{V_A}$$

The minimum output voltage needed to keep M_2 in saturation region

$$V_{DS2} > V_{GS2} - V_{Th} \quad \Rightarrow \quad V_{out\,\min} = \sqrt{\frac{2I_{out}}{k'\left(W/L\right)_2}}$$

$V_{out\,min}$ depends on transistor geometary



if you reduce $V_{GS2} - V_{Th}$

you can still keep I_{out} high enough by increasing $\left(W/L\right)_2$

⟶ but there is a limit as you enter weak inversion instead of strong inversion

transistor goes to subthreshold $V_{GS} \sim V_{Th}$

at weak inversion $V_{GS2} - V_{Th} \sim 2nV_T$ → thermal voltage

ideality factor

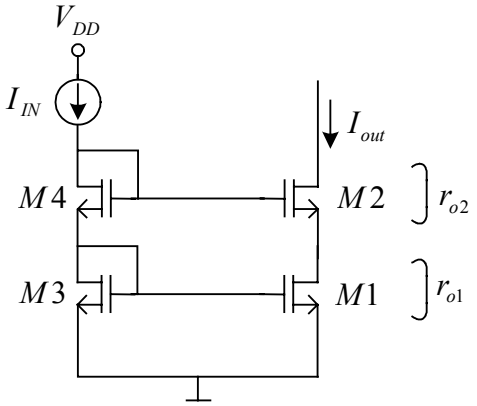
$n \approx 1.5$

$V_T = 26mV = \dfrac{KT}{q}$ ⟶ $V_{out\,\min} = 3V_T \approx 78mV$

6 *parms*

αV_{DD} , αT , r_o , V_{IN} , $V_{out\,\min}$, ε → systematic gain error

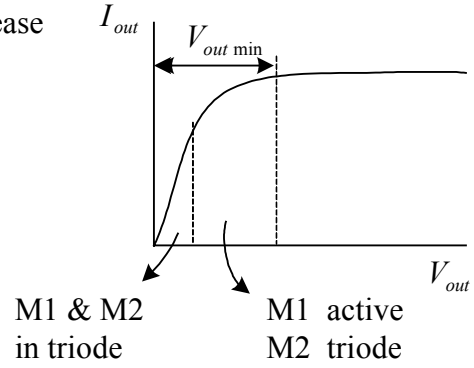
Cascode Current Mirror



output resistance increases as you go to cascode topology

$$R_o = r_{o2}\left(1 + g_{m2}\, r_{o1}\right) + r_{o1}$$

Problem: $V_{out\,min}$ increase



you can stack more transistors to get higher output resistance

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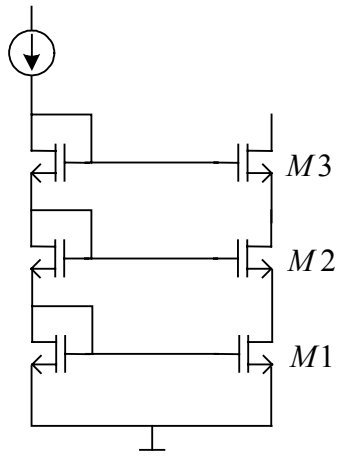


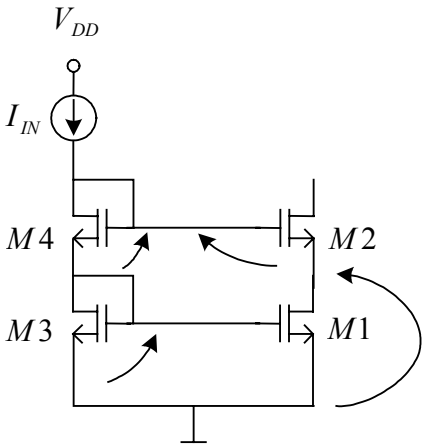
$$R_{o3} = r_{o3}\left(1 + g_{m3}\, R_{o2}\right) + R_{o2}$$

$$R_{o2} = r_{o2}\left(1 + g_{m2}\, r_{o1}\right) + r_{o1}$$

$$r_o = 1M\Omega$$
$$g_m\, r_o \sim 50$$

$$\longrightarrow \quad R_{o3} = \underbrace{r_{o3} g_{m3}}_{50}\ \underbrace{r_{o2} g_{m2}}_{50}\ \underbrace{r_{o1}}_{1M\Omega} = 2.5G\Omega$$

of course parasitic leakage path such as substrate leakage path is comparable to the output resistance



$V_{ds1} = V_{gs3} + V_{gs4} - V_{gs2}$

diode connected $M3$ $\quad V_{ds3} = V_{gs3}$

if $V_{GS2} = V_{GS4}$

$\downarrow$

$V_{DS1} = V_{DS3}$

M1 & M3 are identically biased

therefore systematic gain error $\quad \varepsilon = 0$

in practice $\quad V_{gs2} \neq V_{gs4}$ $\quad$ because of channel length modulation

$\longrightarrow \quad \varepsilon \sim 0$

* input voltage

$$V_{IN} = V_{gs3} + V_{gs4}$$

ignoring body effect and assuming transistors with identical overdrive $V_{GS} - V_{Th}$

$$V_{IN} = 2V_{Th} + 2\sqrt{\frac{2I_D}{k'\left(W/L\right)_3}}$$

body effect $\quad V_{SB} > 0 \longrightarrow V_{Th} \uparrow$

$\longrightarrow$ make it difficult to design input current source with low power supply

* for both M1 & M2 to operate in active region

$V_{DS1} \approx V_{DS3} = V_{gs3}$

M2 active $\longrightarrow$ $V_{DS2} > V_{gs2} - V_{Th} = \sqrt{\dfrac{2I_D}{k'\left(W/L\right)_2}}$

$V_{out\,\min} = V_{DS1} + V_{DS2\,\min} = V_{gs3} + \sqrt{\dfrac{2I_D}{k'\left(W/L\right)_2}}$

$V_{gs3} = V_{Th} + \sqrt{\dfrac{2I_D}{k'\left(W/L\right)_3}}$

$\longrightarrow$ $V_{out\,\min} = V_{Th} + 2\sqrt{\dfrac{2I_D}{k'\left(W/L\right)}}$

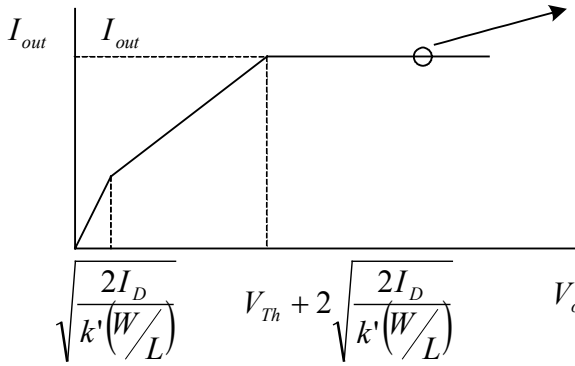
problem is now you have to at least have V_{Th} at your output

for simple current source

$$V_{out\,\min} = \sqrt{\frac{2I_D}{k'\left(W/L\right)}}$$

$V_{out} < V_{out\,\min}$ $\longrightarrow$ M2 in triode

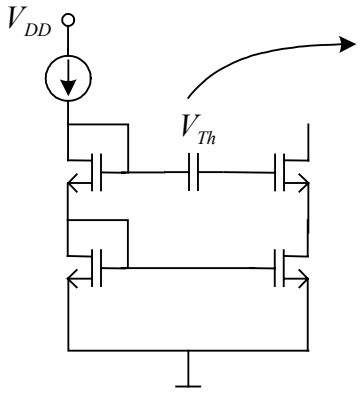
$V_{out} < \sqrt{\dfrac{2I_D}{k'\left(W/L\right)}}$ $\longrightarrow$ M1 in triode



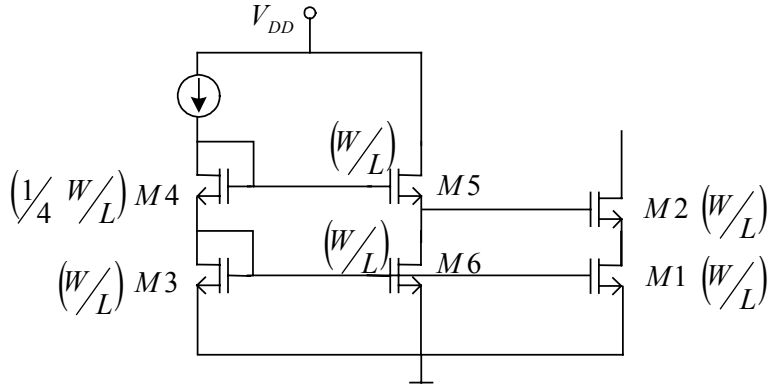
almost flat due to very high output impedance provided by cascode

$V_{out\,\min} = V_{Th} + 2\sqrt{\dfrac{2I_D}{k'\left(W/L\right)}}$ is too high for low power design

V_{Th} comes because $V_{DS1} = V_{DS3} = V_{gs3}$
if you could bias V_{DS1} at lower voltage (V_{Th} lower)
then M1 would be still in active region



this battery introduces a level shift
but we do not have battery
to get the level shift we use source-followers



$\longrightarrow \quad V_{out\ \min} = 2\sqrt{\dfrac{2I_D}{k'\left(W/L\right)}}$

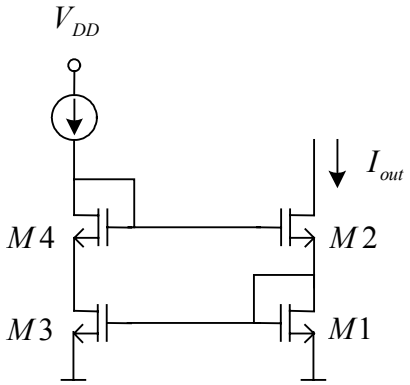
M5 source follower $\longrightarrow$ biased by M3, M6 simple current source

$V_{IN} = 2V_{Th} + 3\sqrt{\dfrac{2I_D}{k'\left(W/L\right)}}$ $\longrightarrow$ limits the minimum power supply you can use

systematic gain error $\varepsilon = \dfrac{V_{DS1} - V_{DS3}}{V_A} \approx \dfrac{-V_{Th}}{V_A}$

smaller W/L ratio selected due to body effect to ensure proper operation

Wilson Current Source



$$R_O = \frac{1}{g_{m1}} + r_{o2} + g_{m2}\, r_{o2}\left(1 + \frac{1}{g_{m1}\, r_{o3}}\right) r_{o3}$$
$$\approx (1 + g_{m2}\, r_{o3})\, r_{o2}$$

→ output resistance is as high as cascode

$\varepsilon = 0 \longrightarrow$ systematic gain error without M4

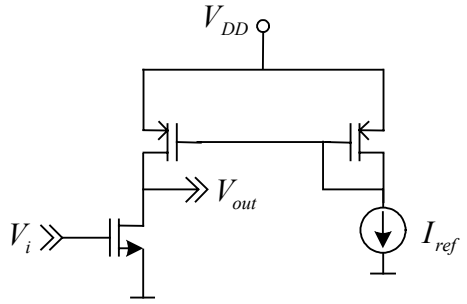
$$\varepsilon = \frac{V_{DS1} - V_{DS3}}{V_A} = \frac{-V_{GS2}}{V_A}$$

$$V_{out\,\min} = V_{gs1} + \sqrt{\frac{2I_D}{k'\left(W/L\right)_2}}$$
$$= V_{Th} + 2\sqrt{\frac{2I_D}{k'\left(W/L\right)}}$$

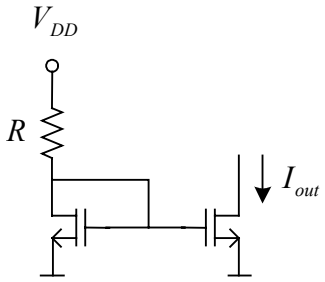
$$V_{IN} = V_{gs1} + V_{gs2} = 2V_{Th} + 2\sqrt{\frac{2I_D}{k'\left(W/L\right)}}$$

* you can use current source
- bias a transistor
- active load → much more compact than resistor
  give you high eq. res → high gain

example:
use PMOS
in a simple
current source



Sensitivity to Power Supply



definition of sensitivity $S_x^y = \lim_{\Delta x \to 0} \frac{\Delta y / y}{\Delta x / x} = \frac{x}{y}\frac{\partial y}{\partial x}$

$$I_{out} = I_{IN} = \frac{V_{DD} - V_{GS}}{R}$$

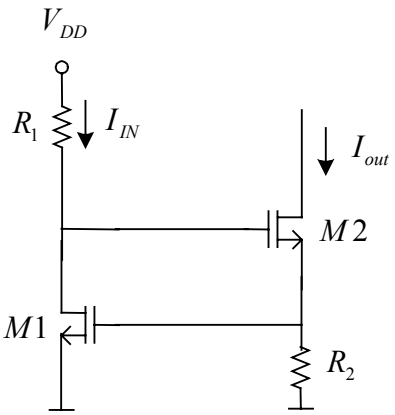
$$S_{V_{DD}}^{I_{out}} = \frac{V_{DD}}{I_{out}} \cdot \frac{\partial I_{out}}{\partial V_{DD}} = \frac{RV_{DD}}{V_{DD} - V_{GS}} \cdot \frac{1}{R} = \frac{V_{DD}}{V_{DD} - V_{GS}} \approx 1$$

how I_{out} varies as supply voltage varies slightly

assuming $V_{DD} >> V_{GS}$

Simple current source should not be used
if bias independent current source is desired

Another Example



Threshold referenced current source
(V_{Th} - referenced)

$$I_{out} = \frac{V_{GS1}}{R_2} = \frac{V_{Th} + \sqrt{\dfrac{2I_D}{k'\left(W/L\right)_1}}}{R_2}$$

by selecting sufficiently low input current and large $(W/L)_1$:

$$\sqrt{\frac{2I_D}{k'\left(W/L\right)_1}} \ll V_{Th}$$

⟶ output current becomes independent of power supply

$$S^{I_{out}}_{V_{DD}} = \frac{V_{DD}}{I_{out}} \cdot \frac{\partial I_{out}}{\partial V_{DD}} = \left(\frac{I_{IN}}{I_{out}} \cdot \frac{\partial I_{out}}{\partial I_{IN}}\right) \times \left(\frac{V_{DD}}{I_{IN}} \cdot \frac{\partial I_{IN}}{\partial V_{DD}}\right)$$

$$= S^{I_{out}}_{I_{IN}} \cdot S^{I_{IN}}_{V_{DD}}$$

$$S^{I_{out}}_{I_{IN}} = \frac{I_{IN}}{I_{out}} \cdot \frac{1}{R_2} \cdot \sqrt{\frac{2}{k'\left(W/L\right)_1}} \cdot \frac{1}{2}\left(I_{IN}\right)^{-1/2} = \frac{\sqrt{\dfrac{2I_{IN}}{k'\left(W/L\right)_1}}}{2R_2 I_{out}}$$

$$= \frac{\sqrt{\dfrac{2I_{IN}}{k'\left(W/L\right)_1}}}{2\left(V_{Th} + \sqrt{\dfrac{2I_{IN}}{k'\left(W/L\right)_1}}\right)} \qquad \Rightarrow \qquad S^{I_{out}}_{V_{DD}} = \frac{V_{GS1} - V_{Th}}{2V_{GS1}} \cdot S^{I_{IN}}_{V_{DD}}$$

$$I_{IN} = \frac{V_{DD} - V_{GS2} - V_{GS1}}{R_1} = \frac{V_{DD} - V_{Th2} - V_{Th1}}{R_1}$$

small current
large W/L ratios $\Rightarrow \quad S^{I_{IN}}_{V_{DD}} \approx 1$

Assuming $V_{DD} = 2.5V \longrightarrow$

$R_1 = 50K\Omega$

$V_{Th} = 0.7V$

$k' = 1.6\times10^{-4} \quad A/V^2$

$\left(\frac{W}{L}\right)_1 = 25$

$$I_{IN} \approx \frac{2.5 - 0.7 - 0.7}{50\times10^3} \approx \frac{1V}{50\times10^3} = 20\,\mu A$$

$$V_{GS1} = V_{Th} + \sqrt{\frac{2I_{IN}}{k'\left(W/L\right)_1}}$$

$$= 0.7 + \sqrt{\frac{40\times10^{-6}}{1.6\times10^{-4}\times25}}$$

$$= 0.7 + 0.1 = 0.8V$$

$$S^{I_{out}}_{V_{DD}} = \frac{0.8 - 0.7}{2\times0.8}\times1 = \frac{1}{16} = 6.6\%$$

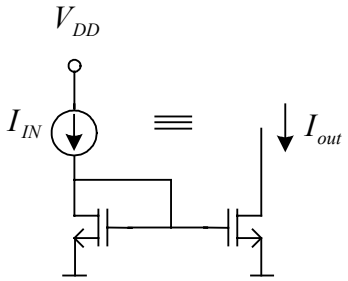
Still bias dependent but it is better than
simple current source where S=100 %

$$I_{out} = \frac{V_{GS1}}{R_2} = \frac{0.8V}{8K\Omega} = 100\,\mu A$$

$$\left(\frac{W}{L}\right)_2 = 125 \quad \rightarrow \quad V_{GS2} = 0.8V$$

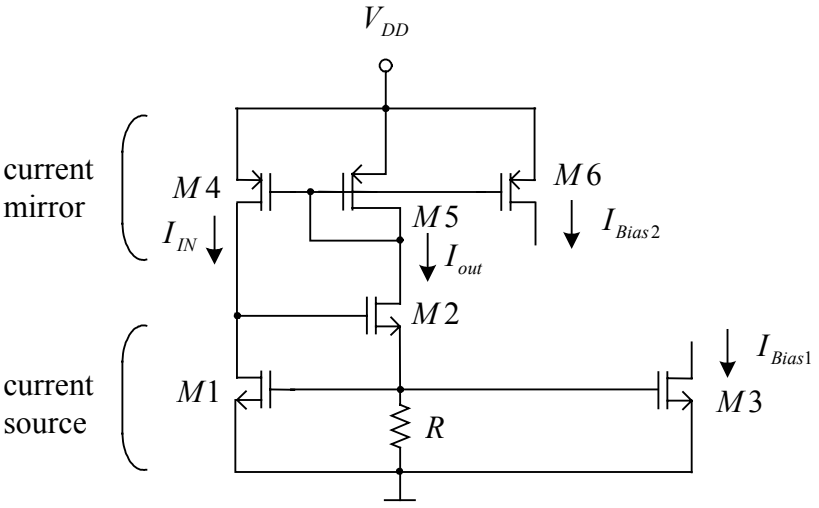
how to completely remove the sensitivity to power supply

→ use a technique called bootstrap bias = self bias

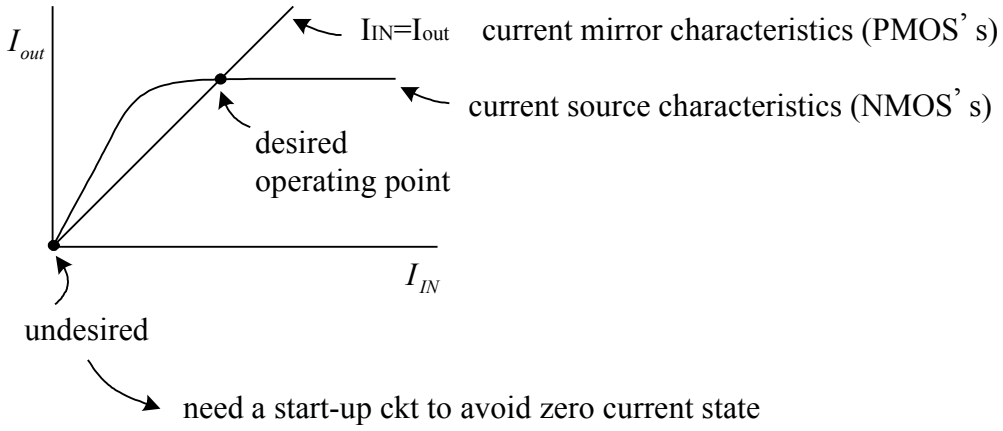


what if I_{IN} is a mirror of I_{out}

ckt
implementation

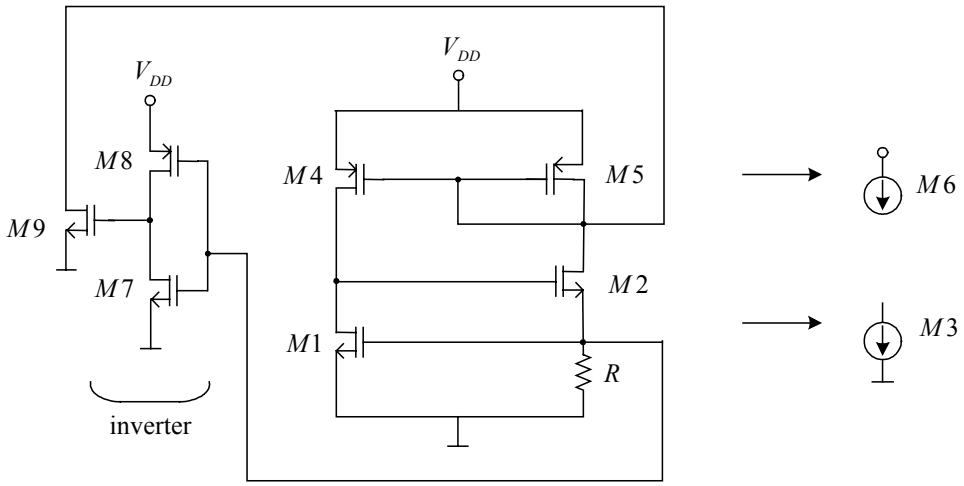


by adjusting M6 and M3 sizing you can get
any current you wish for Bias 2 & Bias 1

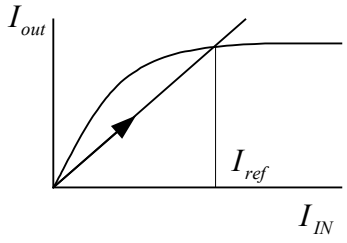


need a start-up ckt to avoid zero current state

self biasing
implementation
with start-up ckt



in case of zero state current, the voltage across R is zero
Then output of inverter M7 & M8 is V_{DD} which turns M9 on into saturation which turns on M5 to conduct → go to other stable solution



at $I_{IN}=I_{out}=I_{ref}$ the voltage I_{ref} R across R results in inverter output to be zero therefore turns off M9 but M5 current continue to pass through M2 and R

Now that we have made supply independent current sources, what about temperature sensitivity?

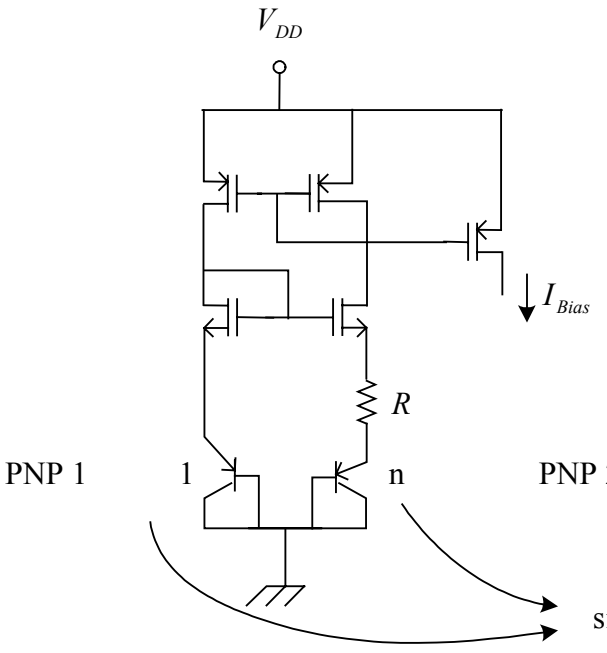
self-biased current source

$$I_{out} = \frac{V_{Th} + \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}}{R} \quad = I_{out}$$

unfortunately V_{Th} is a strong function of temperature

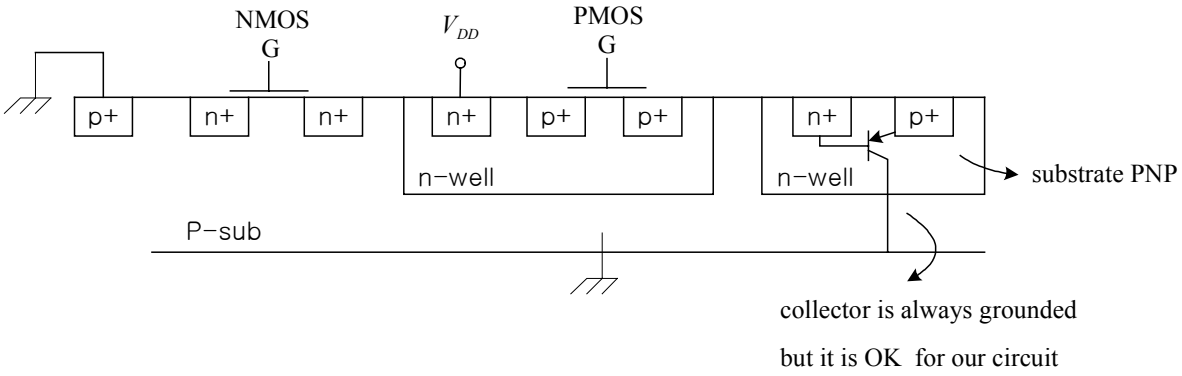
$$\frac{\Delta V_{Th}}{\Delta T} \approx \frac{-2mV}{C°}$$

There are other ways to make current sources such that I_{Bias} is not a function of V_{Th}



sinc ratio $\frac{n}{1}$ by sizing the emitter areas n:1

So far we only talked about CMOS
Here we are using bipolar pnp transistor
The good news is we can use parasitic pnp bipolar transistor in an only CMOS technology
How



current in bipolar transistors has
an exponential dependent to input voltage

$$I = J_O A_E \exp\left(\frac{V_{BE}}{V_T}\right) \quad \rightarrow \quad V_{BE} = V_T \ln\frac{I}{J_O A_E}$$

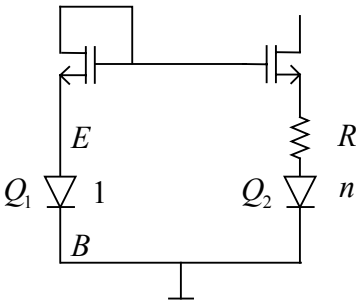
dark current density

emitter area

$$thermal\ voltage = \frac{kT}{q} = 26\,mV\ \ at\ \ room\ \ temp$$

do not confuse with threshold voltage

How does the ckt work



assuming identical MOS transistors

→ PMOS current mirrors

→ $I_{IN} = I_{out}$

$$V_{BE1} = R\,I_{out} + V_{BE2}$$

$$V_T \ln\frac{I_{IN}}{J_O A_E} = R\ I_{out} + V_T \ln\frac{I_{out}}{J_O n A_E}$$

$$R\,I_{out} = V_T \ln\left(n \cdot \frac{I_{IN}}{I_{out}}\right)$$

$$I_{out} = \frac{V_T}{R}\ln(n)$$

current mirror

again I_{out} is independent of bias (V_{DD}) but still a strong function of temperature

How to make temperature independent bias

Temperature Coefficient (TC) of I_{out}

$$\left.\begin{aligned} TC &= \frac{1}{I_{out}}\frac{\partial I_{out}}{\partial T} \\ I_{out} &= \frac{V_T}{R}\ln(n) \end{aligned}\right\} \longrightarrow \quad TC = \left(\frac{\partial I_{out}}{\partial R}\cdot\frac{\partial R}{\partial T} + \frac{\partial I_{out}}{\partial V_T}\cdot\frac{\partial V_T}{\partial T}\right)\frac{1}{I_{out}}$$

$$TC = \left(\frac{-I_{out}}{R}\cdot\frac{\partial R}{\partial T} + \frac{I_{out}}{V_T}\cdot\frac{\partial V_T}{\partial T}\right)\frac{1}{I_{out}}$$

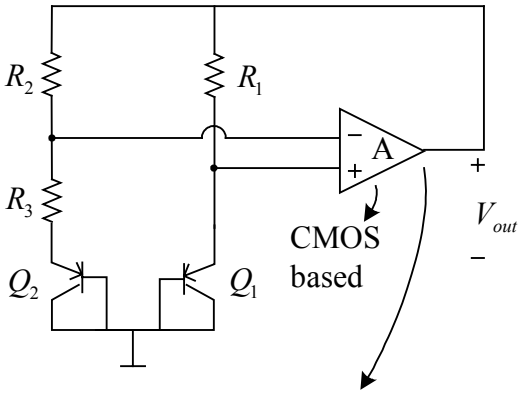
$$\left.\begin{aligned} TC &= \left(\frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T}\right) \\ V_T &= \frac{KT}{q} \quad \rightarrow \quad \frac{\partial V_T}{\partial T} = \frac{K}{q} = \frac{1}{T}\cdot V_T \end{aligned}\right\} \longrightarrow \quad TC = \frac{1}{T} - \frac{1}{R}\frac{\partial R}{\partial T}$$

assuming R with a temp coefficient of $+1500\ ppm/^{\circ}C$

$$\longrightarrow \quad TC_{\substack{Iout \\ at\ 300K}} = 3300\ ppm/^{\circ}C - 1500\ ppm/^{\circ}C = 1800\ ppm/^{\circ}C$$

positive temp coefficient of
the resistor slightly compensates
for temp coefficient of thermal
voltage but it is not enough

Temperature Independent Biasing



$$V_{out} = \left(\frac{R_2}{R_3} + 1\right)\left(V_{EB1} - V_{EB2}\right) + V_{EB2}$$

$\left(\frac{R_2}{R_3} + 1\right)\left(V_{EB1} - V_{EB2}\right)$ → $\propto V_T$, $+ve\ TC$

V_{EB2} → emitter base voltage, $TC \approx \frac{-2mV}{°C}$, $-ve\ TC$

cancel each other

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = V_T \ln\left(\frac{I_1}{I_2} \times \frac{I_{S2}}{I_{S1}}\right) = V_T \ln\left(\frac{I_1}{I_2} \times \frac{A_{E2}}{A_{E1}}\right)$$

dark current

to get a high ΔV_{EB} we force a small current into
a large transistor and a large current into a small transistor

Bandgap Reference Circuit