Chapter 6
Metal Semiconductor Field Effect Transistors (MESFETs)

GaAs MESFETs were first introduced in 1966. Because of simple fabrication technology and excellent microwave characteristics, for over 20 years, MESFETs was the device of choice for high speed, low noise and high power applications. Modern MESFETs are still used in power amplifiers, however their applications are limited by the advent of HBTs, HEMTs and nanoscale MOSFETs.

Basic Structure

GaAs MESFET takes advantage of velocity saturation under high electric field. Fig. 6.1 shows the cross section and the top view of GaAs MESFET devices. Gate is formed by a Schottky-barrier contact formed between Al metal and N-doped GaAs region. Source and drain are formed by putting AuGe contact metallization on N+ GaAs contact regions.

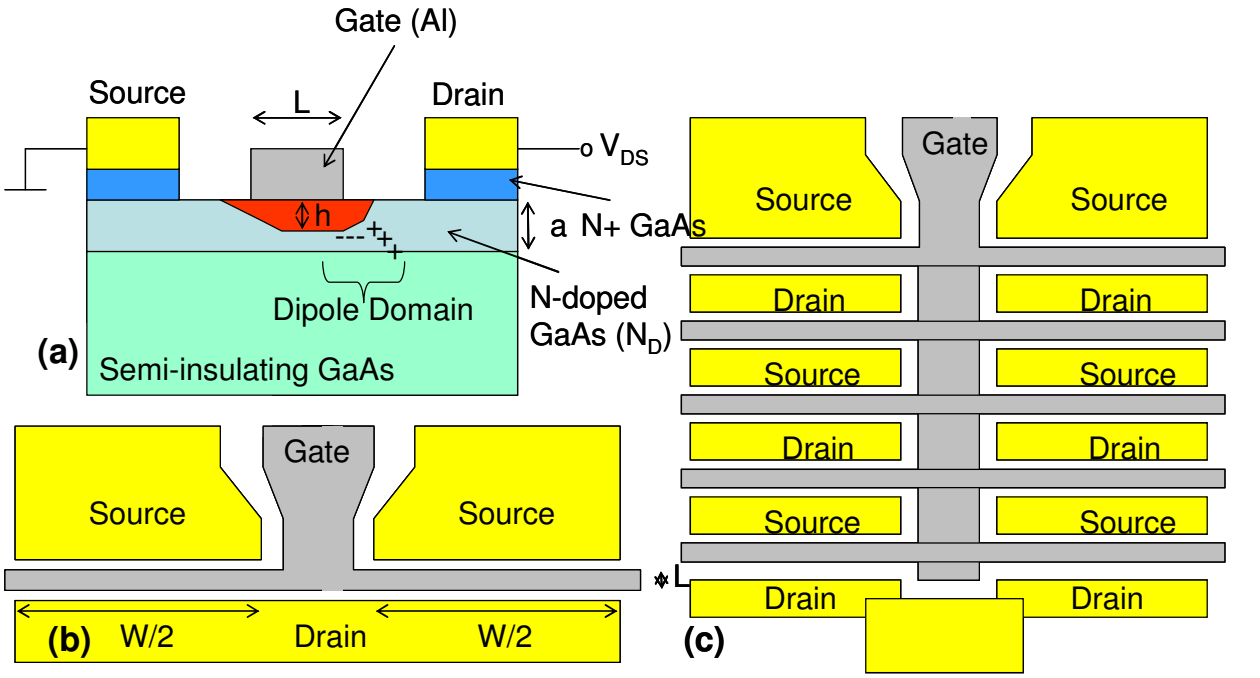


Fig. 6.1. (a) Cross section of a GaAs MESFET. (b) Top view of a two finger transistor. (c) Top view of a multi-finger transistor. Airbridge technology is used to connect all source and drain contacts.

An important rule of thumb for microwave FET design is that the distance from the gate feed point to the end of gate finger (W/2) be less than λ/16 where λ is the wavelength along the gate at the frequency of operation. The upper limits on W/2 range are 5mm for 1GHz operating frequency and 50μm for 100GHz operating frequency. For high power applications, many unit cells, each having a gate finger width less than λ/16 are placed close together and fed in parallel in a multi-finger power FET shown in Fig. 6.1(c). Non of the boundaries of this configuration may exceed λ/16. In addition to these size constraints, there are also impedance and thermal constraints on power FET designs. With common microwave techniques, it is difficult to match typical transmission line impedances (~50Ω) to FET input impedances that are below a few ohm. Because power FET impedance varies inversely with the number of cells connected in parallel, the impedance matching restriction may limit the number of fingers. The spacing between the fingers in a power FET may also have to be restricted to some minimum value to avoid excessive temperatures in each cell, thereby restricting the total number of fingers as well.

DC Characteristics and Basic Design

Typical DC characteristics of a GaAs MESFET are shown in Fig. 6.2. The pinch off voltage is defined as the voltage necessary to deplete the entire depth of the channel (a). Assuming a uniform doping N_D in the channel, one can calculate the pinch off voltage V_P according to

$$V_P = \frac{qN_D a^2}{2\varepsilon_s} \tag{6.1}$$

where ε_s is the dielectric constant of GaAs ($\varepsilon_s = 10.9\varepsilon_0$). The threshold voltage is defined according to

$$V_T = V_{bi} - V_P \tag{6.2}$$

where V_{bi} is Schottky-barrier built-in voltage. By reducing the doping level N_D in the channel and also introducing gate recess technology (etching the channel underneath the gate region), it is possible to develop normally off MESFETs (enhancement modes). Because of low doping in the channel and thinner channel, the resulting enhancement MESFETs typically have low current capabilities and therefore are not suitable for high power applications.

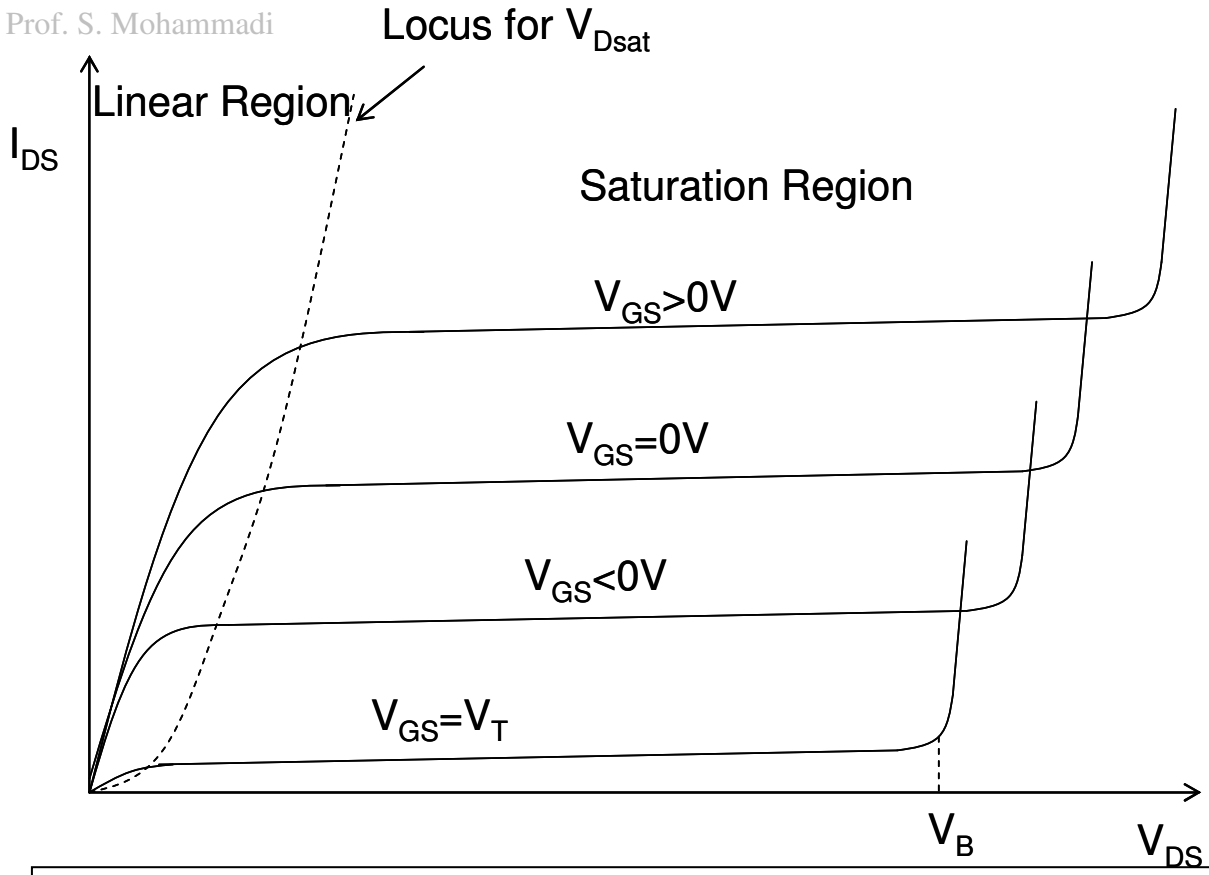


Fig. 6.2. Typical I-V characteristics of an N-channel depletion mode GaAs MESFET.

There are two distinct region known as linear region and saturation region. In the linear region, the velocity of electrons inside the channel has not reached the saturation velocity limit (v_s=1.2×10^{7}cm/sec for 1 to 2µm gate length and v_s=1.5×10^{7}cm/sec for 0.5µm gate length). As the drain source voltage is increased and through the formation of domains close to the drain side of the channel, electrons reach their drift velocity. As a result the current in the channel saturates. Drain source current can be written as

$$I_{DS} = qv_s WN_D(a-h) \tag{6.3}$$

Where W is the total width of the transistor. Substituting gate depletion with h from the Schottky barrier depletion equation, the current becomes

$$I_{DS} = qav_s WN_D\left[1-\left(\frac{V_{bi}-V_{GS}}{V_P}\right)^{1/2}\right] \tag{6.4}$$

where V_{bi} is a positive voltage. Differentiating the current I_{DS} with respect to gate voltage yields the intrinsic DC transconductance g_{mi}.

$$g_{mi} = \frac{v_s \varepsilon_s W}{a}\left(\frac{V_P}{V_{bi} - V_{GS}}\right)^{1/2} \tag{6.5}$$

For advanced MESFETs with gate lengths smaller than 0.5µm, the electrons transit through the high field region under the gate may be so fast that significant inter-valley transfer may not occur before the electrons reach the drain. In this case, electrons never experience velocity saturation as they move in the channel in a nearly ballistic fashion. IV characteristics of a 0.25µm MESFET is shown in Fig. 6.3. Note that there are two distinctive features in the IV characteristics. First, the current level never saturates as electrons inside the channel do not experience inter-valley transfer. Second, the current cannot be turned off even for gate voltages more negative than V_T due to as small separation between source and drain contact which results in finite dark current in the semi-insulating GaAs substrate. Electrons in MESFET channels with 0.25µm and smaller gate lengths gain energy as they travel from source to drain. Since they spend a short time in the channel, they will not slow down as a result of inter-valley transfer. Their velocity close to the drain ohmic region can reach values as high as 1×10^8cm/sec.

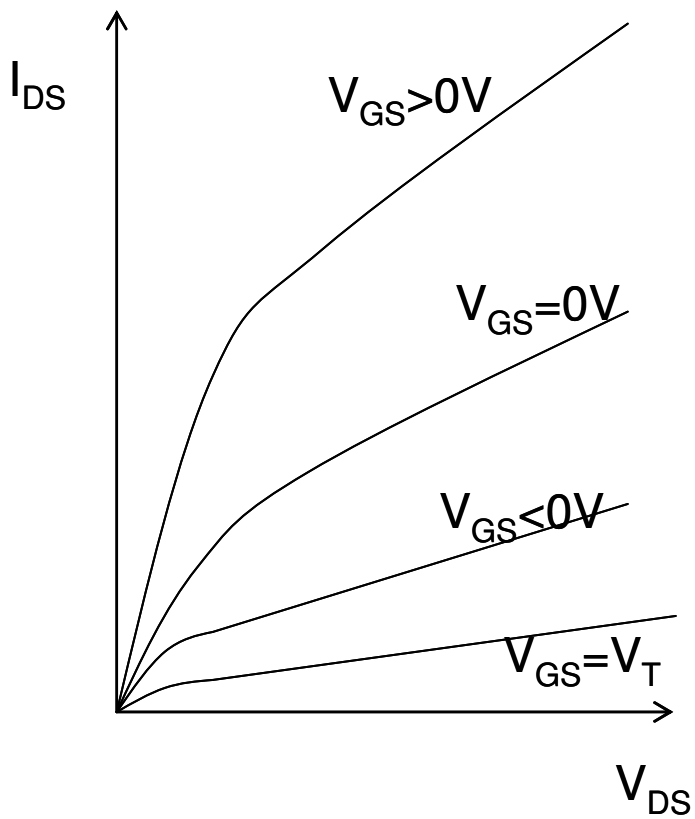


Fig. 6.3. I-V characteristics of a 0.25µm N-channel depletion mode GaAs MESFET.

Basic design of a GaAs MESFET is as following. First, the minimum gate length L is decided based on the cost of fabrication and availability of equipment. Obviously smaller gates are desired to improve the performance of the transistor (higher f_T and f_{max}), however, technologies with 0.25µm and smaller gate lengths become extremely expensive and may require electron

beam lithography for the fabrication. Once L is decided, the value of L/a of 4~5 is used for scaling. This value is a trade-off between transistor cut-off frequency f_T, parasitics and short channel effects. Large L/a ratios reduces current capacity (small a) too small L/a ratios result in high output conductance and enhanced short channel effects. Values of breakdown voltage, maximum drain current and output IV swing are important for high power MESFET devices. For these applications, once "a" is determined, an "N_D.a" value less than $2.3\times10^{12}cm^{-2}$ is chosen to maximize the gate-drain breakdown voltage to

$$V_{breakdown-GD} \approx \frac{5\times10^{13}}{N_D a} \tag{6.6}$$

This relationship takes into account the distribution of electric field across the dipole domain. If the "N_D.a" value is higher than $2.6\times10^{12}cm^{-2}$, the gate-drain breakdown voltage is equal to that of a Schottky barrier diode which is typically 3 times lower than the above value. In this case the break down can be calculated according to

$$V_{breakdown-GD} \approx 60\left(\frac{E_g}{1.1}\right)^{3/2}\left(\frac{10^{16}}{N_D}\right)^{3/4} \tag{6.7}$$

Note that the relation between the gate-drain breakdown voltage and maximum bias voltage VB shown in Fig. 6.2. is given by

$$V_B = V_{breakdown-GD} + V_T \tag{6.8}$$

Small Signal Operation

Small signal model of a FET is shown in Fig. 6.4. Note that C_{GS} is typically several times larger than other parasitic capacitances. R_i represents the resistance in the low-doped channel region that is not under the influence of gate. C_{DC} is the effective capacitance of the dipole domain. The extrinsic transconductance of the device g_m can be calculated from the intrinsic transconductance g_{mi} according to

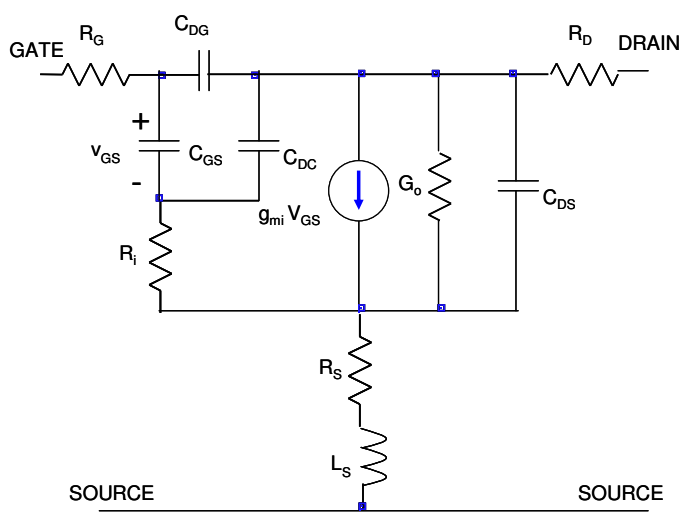


Fig. 6.4. Small Signal Model of a GaAs MESFET.

$$g_m = \frac{g_{mi}}{1 + R_S g_{mi}} \tag{6.9}$$

At high frequency, the parasitic inductance of the source contact LS also becomes a factor in reducing the intrinsic transconductance. According to this simple MESFET model, the small signal power fain of the device in the stable region (MAG) is assumed to roll off as $1/f^2$ or -6dB/octave. Plot of fT as a function of device gate length L is shown in Fig. 6.5. Note that dimensions smaller than 0.5µm, there is s sudden increase in the device cut-off frequency. This is due to velocity overshooting effect observed in MESFETs with gate lengths smaller than 0.25µm.

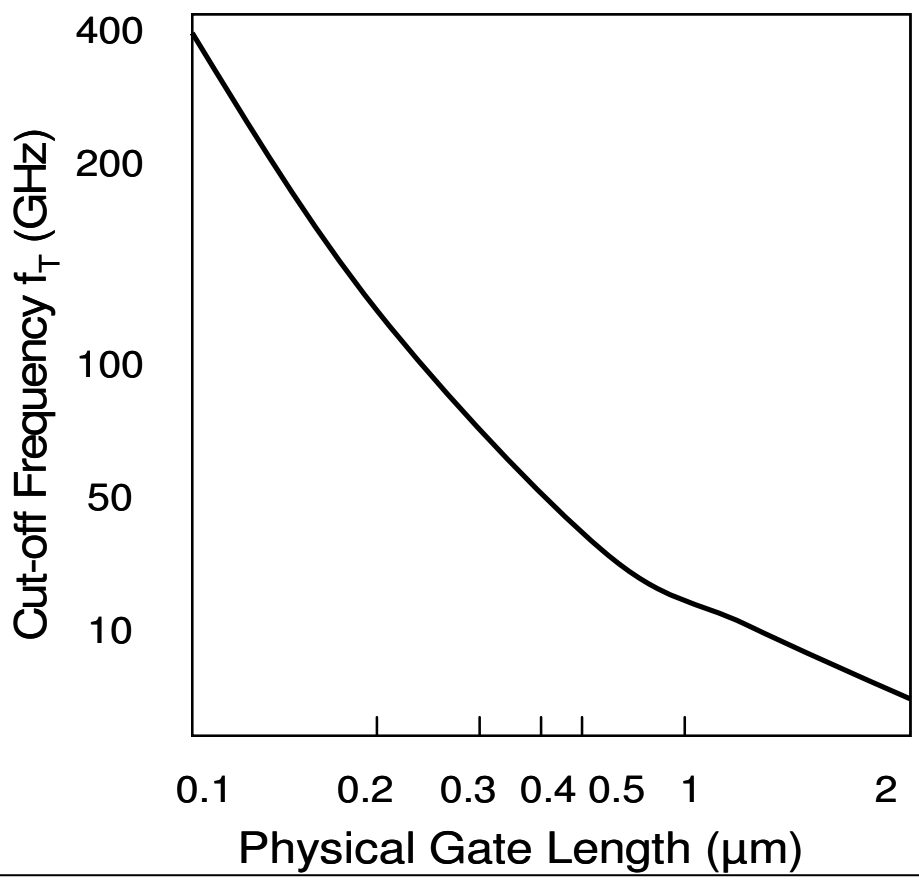


Fig. 6.5. Cut-off frequency of a GaAs MESFET as a function of gate length..

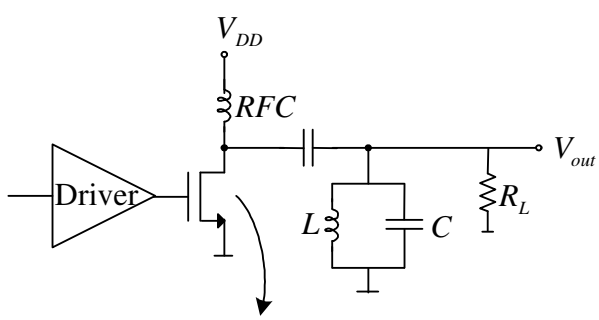
Large-Signal Operation

Various large signal classes of operation for a transistor in general (and a MESFET in particular) are Class A, AB, B and C for sinusoidal signals and Class D, E and F for pulse shape signals.

Typically MESFETs, HEMTs and GaAs HBTs are preferred over CMOS and SiGe HBTs due to higher breakdown voltage, higher frequency of operation and higher gain and higher efficiency.

efficiency
- drain efficiency or collector efficiency: $\eta = \frac{P_{O\,RF}}{P_{DC}}$
- power added efficiency: $PAE = \frac{P_{out} - P_{in}}{P_{DC}} \le \eta$

Typical Power Amp Ckt :



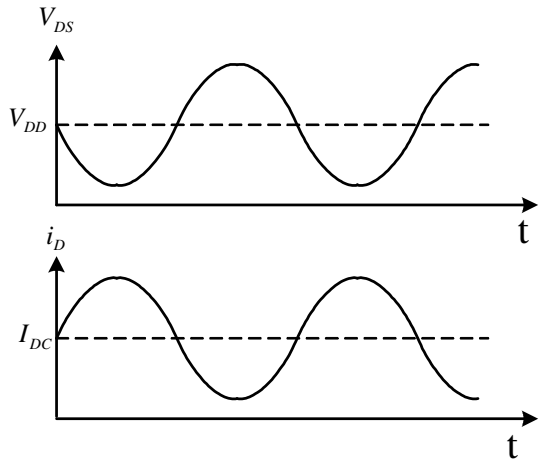
multi-finger : W ~ several mm

Different Classes of Power Amplifiers

Class A

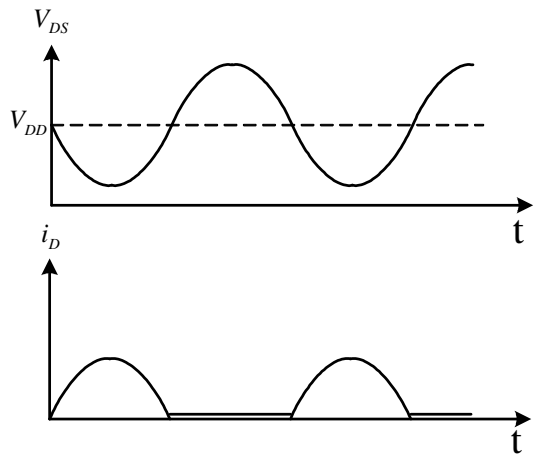
- linear
- low efficiency
- no clamping in V_{DS} , i_D

Class A



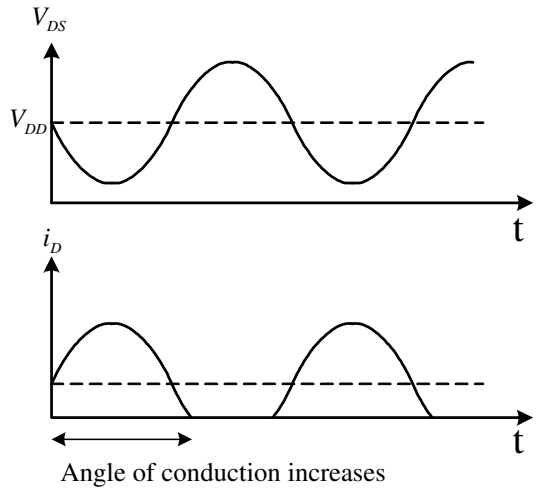
$\eta < 50\%$

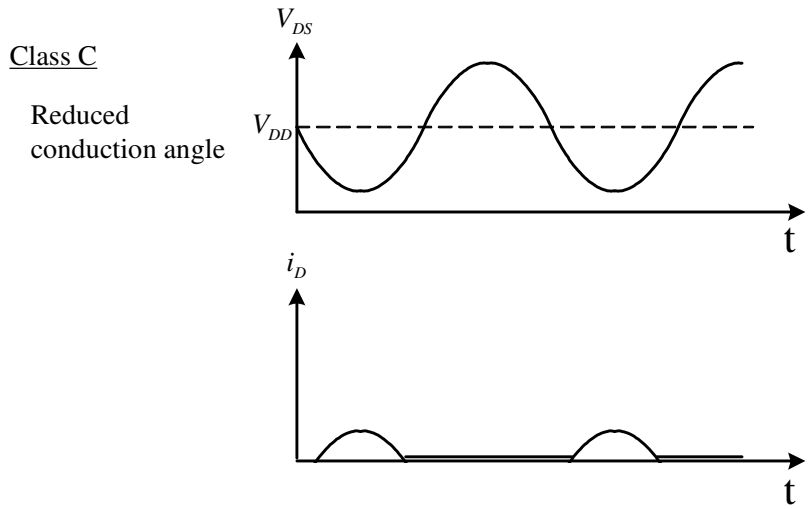
Class B



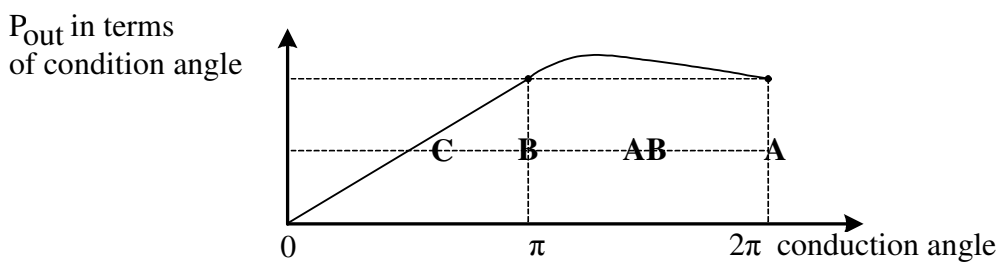
$\eta < \frac{\pi}{4} = 78\%$

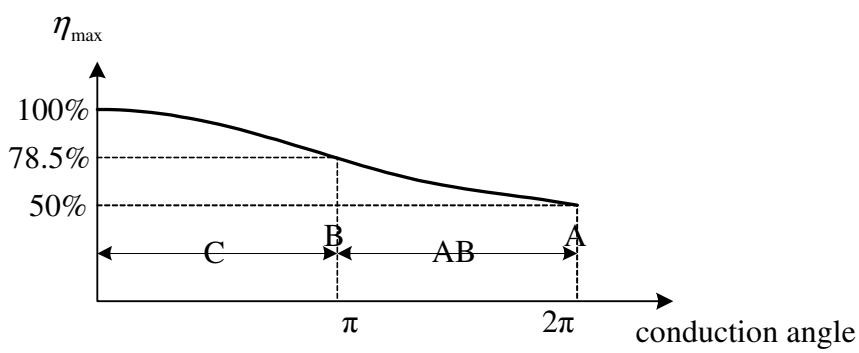
Class AB



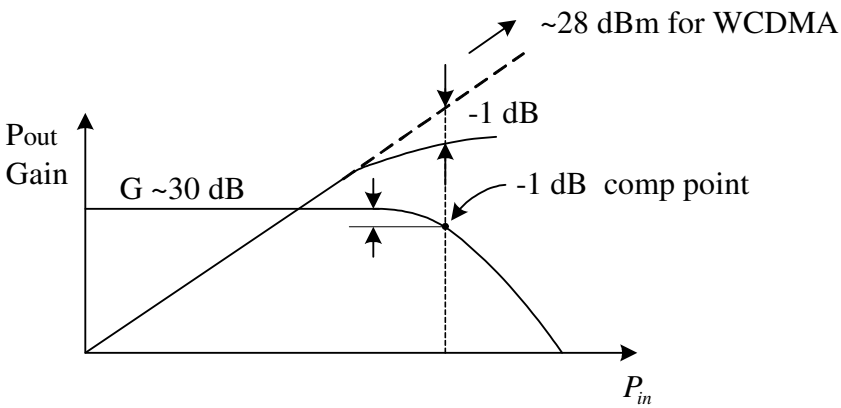


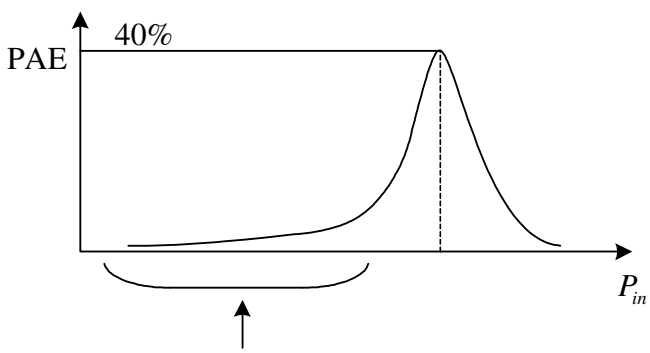
Conduction angle is smaller than π.





* what you typically observe





Problem is this range that your P_{out} (P_{in}) is low (urban areas) but your efficiency is also low

→ so you are still wasting a lot of DC power

→ to solve the problem use dynamic biasing or smart power Amp

There are higher classes of Amps (class E, F, S)

Problems * too non-linear

* often good for audio freq.

Advantages * very efficient $\eta \rightarrow 100\%$

Metrics for Power Amplifiers:

We have already defined Pout, Gain= P_{out}/P_{in} , drain efficiency and power added efficiency. For measuring the linearity of power amplifiers, we define the following metrics:

- 1dB compression point: where Pout degrades by 1dB below its linear (small signal) gain. Note that gain of class AB, B (and higher classes) first increases with input power (gain expansion) then degrades as input power is further increased (gain compression). See the following Fig.
- Input intercept point (defined for input (IIP3) or output (OIP3). It is measured using a two-tone technique. If we extrapolate IMD3 and linear gain, they meet each other at IP3 point according to the following figure.

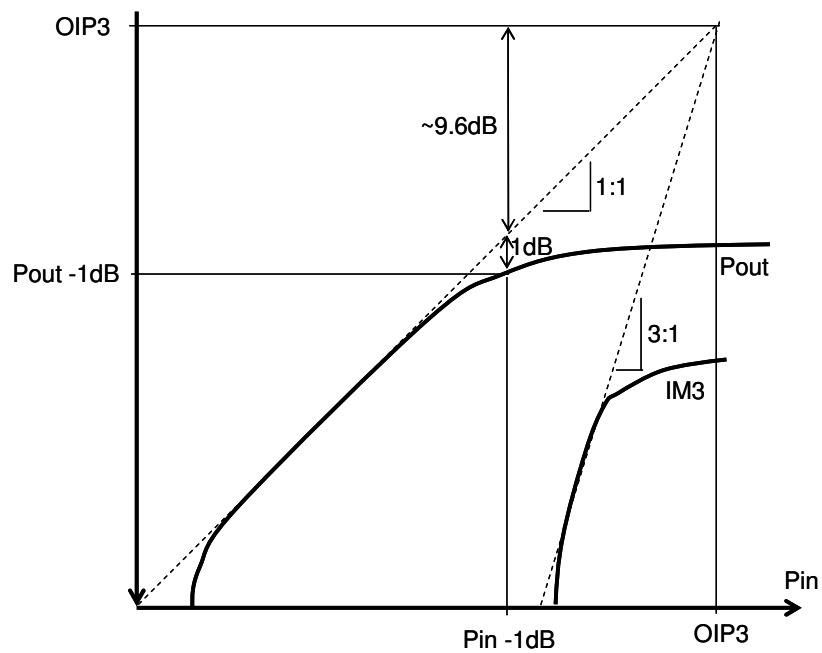


Fig. 6.6. 1dB compression point and third order intercept point definition

- Adjacent channel power ratio (ACPR): Instead of a non realistic 2-tone intermodulation measurement, it is better to measure distortion from spectral regrowth that appears in the sideband channel.

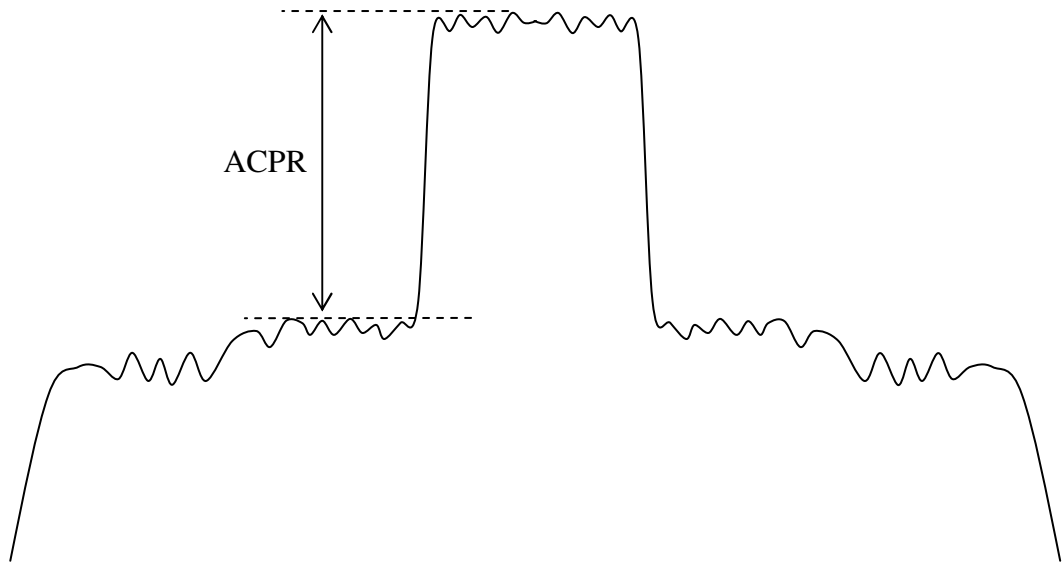


Fig. 6.7. ACPR definition

$$ACPR = \frac{Power\ spectral\ density\ in\ the\ main\ channel}{Power\ spectral\ density\ in\ the\ adjacent\ channel}$$

Let us now consider a MESFET class A amplifier. According to Fig. 6.8, the maximum power output in class A is given by:

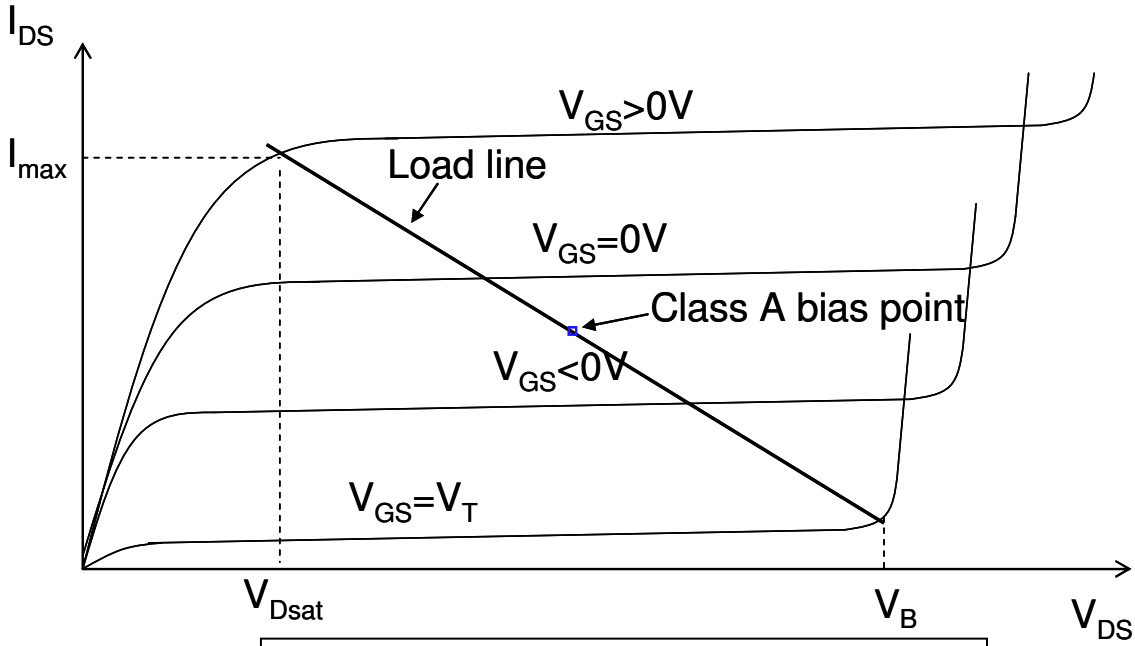


Fig. 6.8. Class A biasing of a MESFET power amplifier

$$P_{out-\max} = \frac{I_{\max}(V_B - V_{Dsat})}{8} \tag{6.10}$$

Here, it is assumed that the drain current varies from zero to a maximum of I_{max}, while the drain source voltage is between V_{Dsat} and V_B. The drain efficiency is then:

$$\eta_D = \frac{\eta_{\max}(V_B - V_{Dsat})}{(V_B + V_{Dsat})} \tag{6.11}$$

η_{max} is a function of dependence of g_m on V_{GS} and the class of operation. Assuming class A operation and constant g_m as a function of V_{GS}, η_{max} is 50% as calculated before. The power added efficiency is then:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta_D\left(1 - \frac{1}{G}\right) \tag{6.12}$$

where G is the gain of the MESFET at the specific frequency and input power.

Noise Performance of MESFETs

Noise behavior of a MESFET is explained by using small signal noise parameters. These four parameters describing the noise of any two port network relate to each other according to:

$$F = F_{\min} + \frac{4R_n\left|\Gamma_s - \Gamma_{opt}\right|^2}{Z_0\left(1 - \left|\Gamma_s\right|^2\right)\left|1 + \Gamma_{opt}\right|^2} = F_{\min} + \frac{\left|R_s + jX_s - Z_{opt}\right|^2}{R_n R_s} \tag{6.13}$$

In the above equation, noise parameters are minimum noise figure at the frequency of interest F_{min}, noise resistance R_n, and optimum source impedance for minimum noise (Z_{opt} or Γ_{opt}). Source reflection coefficient related to source impedance is defined as

$$\Gamma_s = \frac{R_s + jX_s - Z_0}{R_s + jX_s + Z_0} \tag{6.14}$$

where Z_0 = 50Ω is the reference impedance. The above R_s+jX_s is the input matching of the MESFET and should not be confused with R_S which is the MESFET source terminal access resistance in the equivalent model. The MESFET simplified noise equivalent circuit is shown in Fig. 6.9. As a first approximation, the gate noise source $\overline{i_g^2}$ and feedback capacitance C_{DG} are ignored. The drain noise source is expressed as

$$\overline{i_d^2} = 4kT\gamma g_{mi}\Delta f \tag{6.15}$$

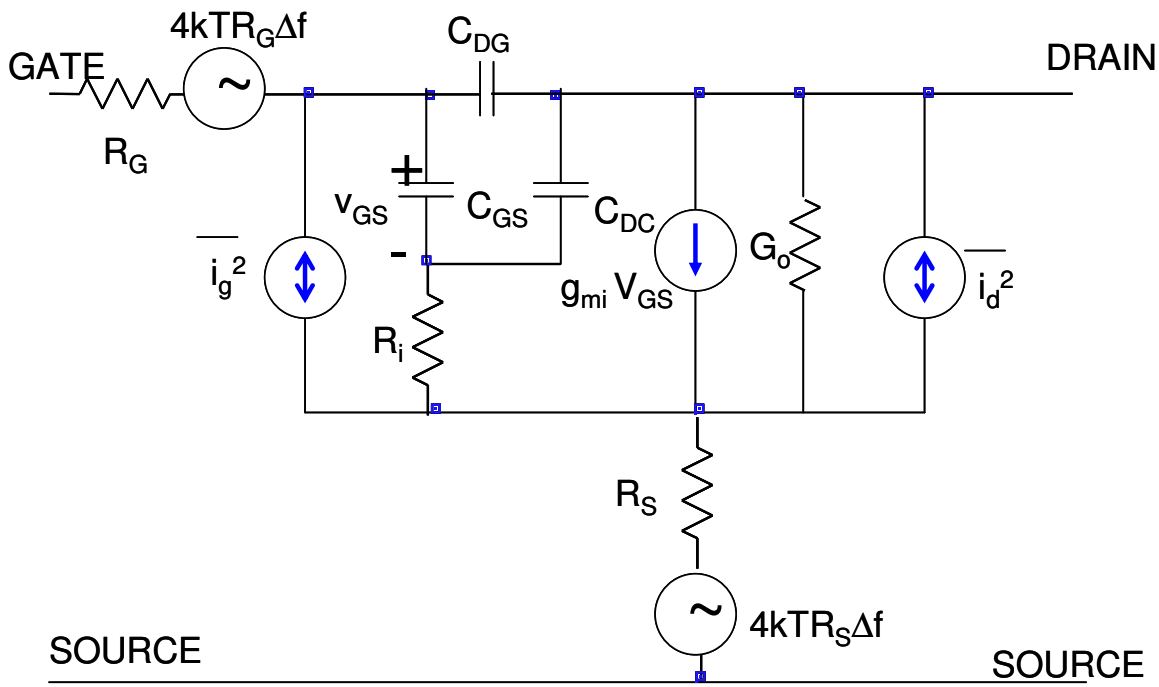


Fig. 6.9. Equivalent noise model of a GaAs MESFET

where γ is a dimensionless parameter ranging from 1~3 depending on the technological parameters and biasing conditions. Following a lengthy circuit analysis, the minimum noise figure can be calculated according to

$$F_{\min} = 1 + 2\sqrt{\gamma}\frac{f}{f_T}\sqrt{g_{mi}(R_S + R_g)} \tag{6.16}$$

Note that here f is the frequency of operation, R_S and R_g are respectively source and gate access resistance and f_T is the cut-off frequency of the transistor. The noise resistance is given by

$$R_n = \frac{f_T^2}{\gamma g_{mi} f^2} \tag{6.17}$$

The optimum source impedance for minimum noise is given by:

$$Z_{opt} = \sqrt{\frac{g_{mi}\left(R_S + R_g\right)}{\gamma}} \cdot \frac{1}{C_{GS}\omega} - j\frac{1}{C_{GS}\omega} \tag{6.18}$$

Paramater γ is estimated as

$$\gamma = \frac{I_{DS}}{L \cdot E_{field_critical} \cdot g_{mi}} \tag{6.19}$$

where L is the length of the transistor and $E_{field_critical}$ is the critical electric field in the material.

Unfortunately such oversimplification in the calculation of MESFET noise is not realistic. One needs to consider the effect of gate noise and its correlation to the drain noise. In the following analysis, we still ignore the effect of feedback capacitance C_{DG}. The gate noise can be expressed as

$$\overline{i_g^2} = \frac{4kT\delta C_{GS}^2\omega^2}{g_{mi}}\Delta f \tag{6.20}$$

where δ is a dimensionless noise parameter that depends on device technology and biasing conditions. After a lengthy circuit analysis, the calculation of minimum noise figure yields

$$F_{\min} = 1 + 2\sqrt{\gamma+\delta-2c\sqrt{\gamma\delta}}\cdot\frac{f}{f_T}\sqrt{g_{mi}\left(R_S+R_g\right)+\frac{\gamma\delta\left(1-c^2\right)}{\gamma+\delta-2c\sqrt{\gamma\delta}}} \tag{6.21}$$

In the above equation c is the correlation factor between gate and drain noise. Note that correlated gate noise is partially subtracted from overal noise due to the correlation. The noise resistance with the effct of correlated gate noise but excluding the effect of feedback resistance is given by

$$R_n = \frac{f_T^2}{g_{mi}\cdot f^2\cdot\sqrt{\gamma+\delta-2c\sqrt{\gamma\delta}}} \tag{6.22}$$

Finally optimum source impedance for minimum noise with the effect of correlated gate noise can be written as

$$Z_{opt} = \sqrt{\frac{g_{mi}\left(R_S+R_g\right)+\frac{\gamma\delta(1-c^2)}{\gamma+\delta-2c\sqrt{\gamma\delta}}}{\gamma+\delta-2c\sqrt{\gamma\delta}}}\cdot\frac{1}{C_{GS}\omega} - j\frac{1}{C_{GS}\omega}\cdot\left(\frac{\gamma-c\sqrt{\gamma\delta}}{\gamma+\delta-2c\sqrt{\gamma\delta}}\right) \tag{6.23}$$

Despite the fact that the gate noise is proportional to ω^2 according to equation 6.20, note that the gate noise influences the noise figure even at very low frequencies. Also note that the noise figure <u>increases linearly</u> with frequency. This is an important observation for MESFETs and HEMTs. As we shall see later on, the noise figure of bipolar transistors increases more rapidly with frequency. Another interesting observation is that even if R_S and R_g are negligible, there is still some intrinsic noise figure stemming from the correlated gate noise described by

$$F_{\min-\text{int}rinsic} = 1 + 2\frac{f}{f_T}\sqrt{\gamma\delta\left(1-c^2\right)} \tag{6.24}$$