Chapter 1. Introduction

Read Section 1.1(Historic) + 1.2(Cost) +1.3 (Quality Metrics)

So far you have been introduced to logic design(concept of 0s and 1s). Some of you know about electronic devices (transistors - - - -). This course is all about how to use transistors to make logic circuits and logic functions.

0 ⟹ 0.2 V

1 1.8 V

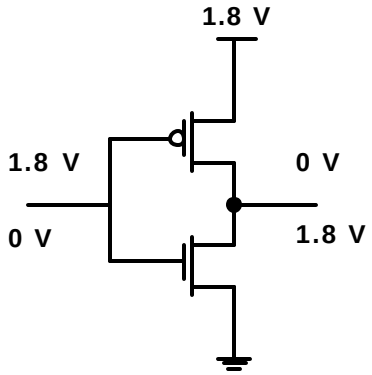
How to make sure we don't interpret the data wrong.

Logic 0 → reads logic 0

0.7 V → logic 0 ?

logic 1 ?

What causes the transistor to have 0.7 V ?

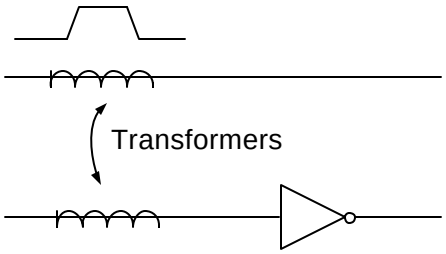


Noise in Digital Integrated Circuits

noise = unwanted coupling

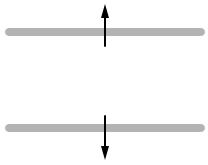
(In digital they call it noise because they don't know how to account for it !)

- Inductive Coupling



Can be reduced by

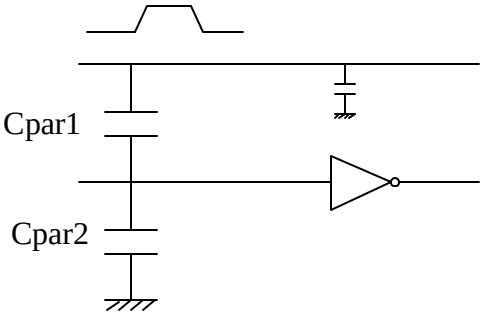
→ distancing interconnects



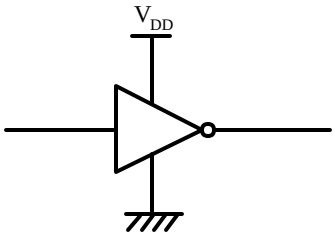
→ Add Ground Plane

→ Shortening interconnects

- Capacitance Coupling can be reduced by same.

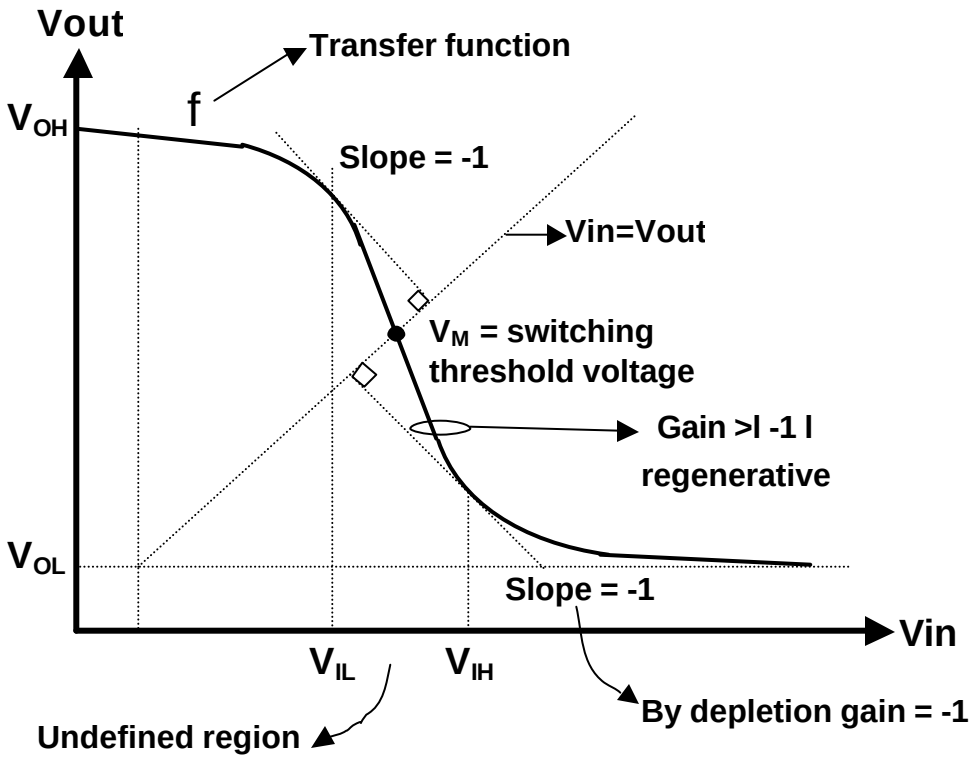


- Power and Gnd noise can be reduced by
  - widening Gnd & V_{DD} interconnect
  - Add capacitors if necessary / available



*How much noise is tolerated?

→ Voltage transfer characteristics of an Inverter

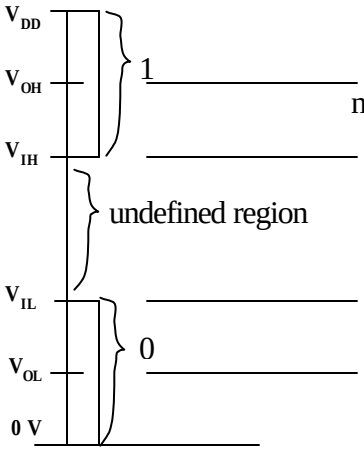


ideal case → $V_{OL} = f(V_{OH})$, $V_{OH} = f(V_{OL})$

but in reality the output signal deviates from the nominal value

*reason → noise, loading in the output of the inverter (Gate)

limits of acceptable region is V_{IL} , V_{IH}



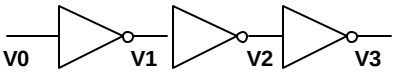
noise margin high NMH NMH = V_{OH} - V_{IH}

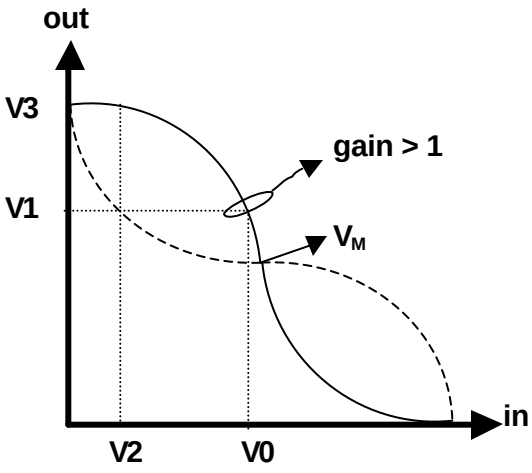
noise margin low NML NML = V_{IL} - V_{OL}

Regenerative vs. non-regenerative

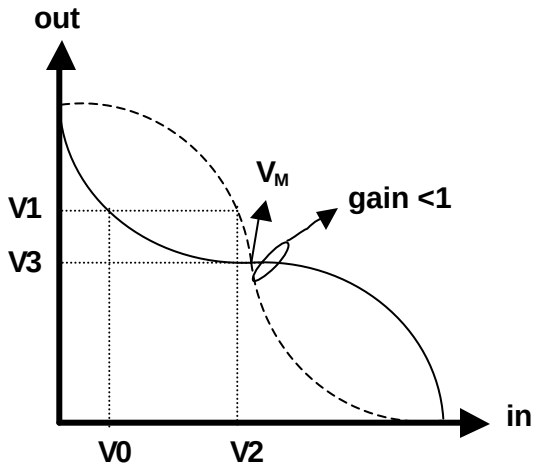
out = f(in)

in = finv(out)





Regenerative



Non-Regenerative

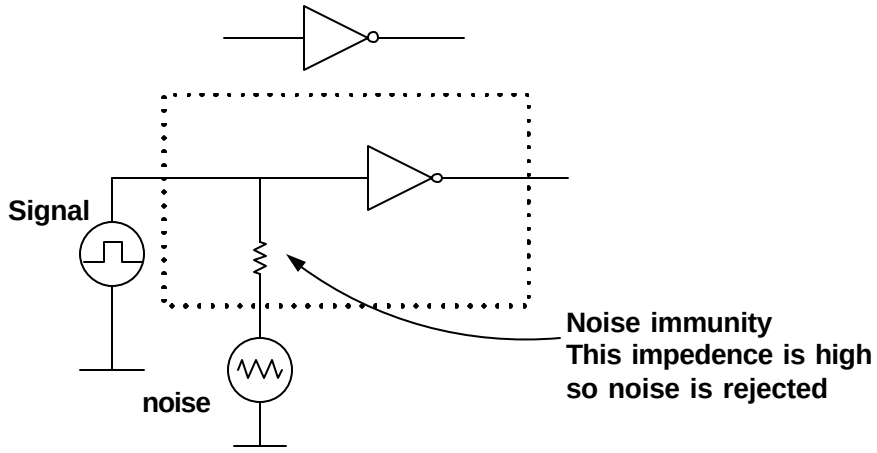
If transfer characteristics is regenerative → undefined input → a few gates, defined output

To be regenerative → gain in undefined region > 1

gain in two legal region < 1

Noise immunity

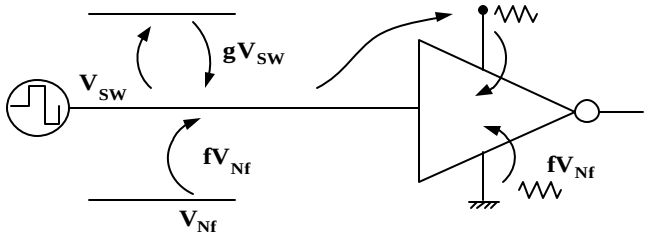
Noise margins may be low but still circuit can reject the noise source. This ability is so called noise immunity.



noise source → proportional to signal swing (strong signal → strong signal)

→ fixed

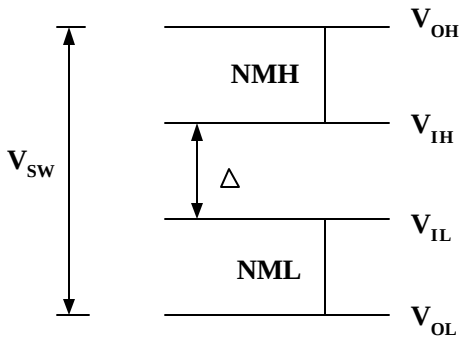
To operate correctly noise margin = Sum of the coupled noise values



$V_{NM} = ? \ f_i V_{Nfi} + ? \ g_j V_{SW}$

fixed proportional

to signal



$V_{SW} = ? + V_{NMH} + V_{NML}$

(assume $V_{NMH} = V_{NML}$)

$V_{SW} = 2 \ V_{NM}$

$\frac{V_{SW}}{2} = V_{NM} = ? \ f_i V_{Nfi} + ? \ g_j V_{SW}$

To operate safe, there is a min signal swing

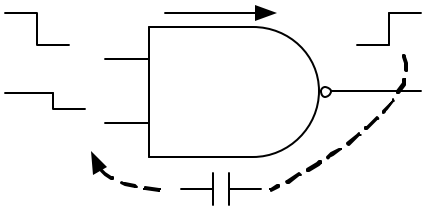
→ $V_{SW} = 2? \ f_i V_{Nfi} / (1 – 2 ? \ g_j)$

2 x Sum of fixed noise / (1 – 2 x Sum of prop.)

Directivity

Logic gate should be unidirectional

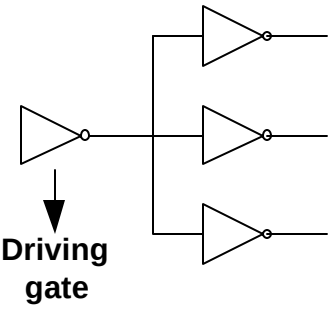
→ Output change should not affect at the input.



Capacitive coupling through

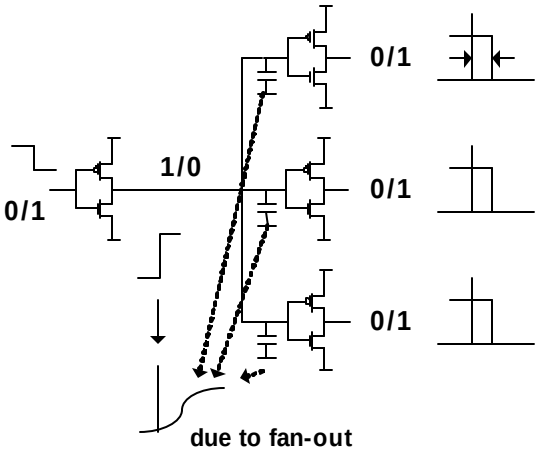
Fan-Out

Increasing fan-out can affect the logic out-put



CMOS logic → no problem in static

dynamically however there will be a limitation !



due to fan-out

Problems

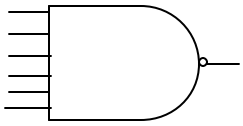
→ increased delay

increased dynamic power

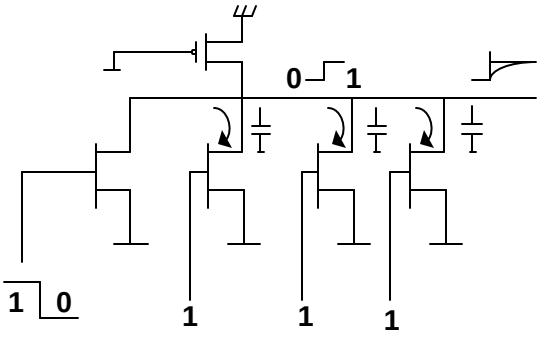
To increase fan-out, W/L of the driver transistor ? ? current drive will increase

? better transit performance

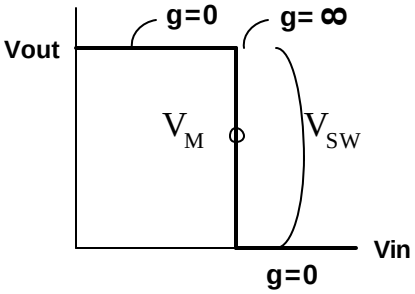
Fan-in



Fan-in ? ? complexity ? ? interior static & dynamic properties



Ideal gate (inverter)



$V_{NML} = V_{NMH} = V_{SW} / 2$

Input impedance ? 8

Output impedance ? 0

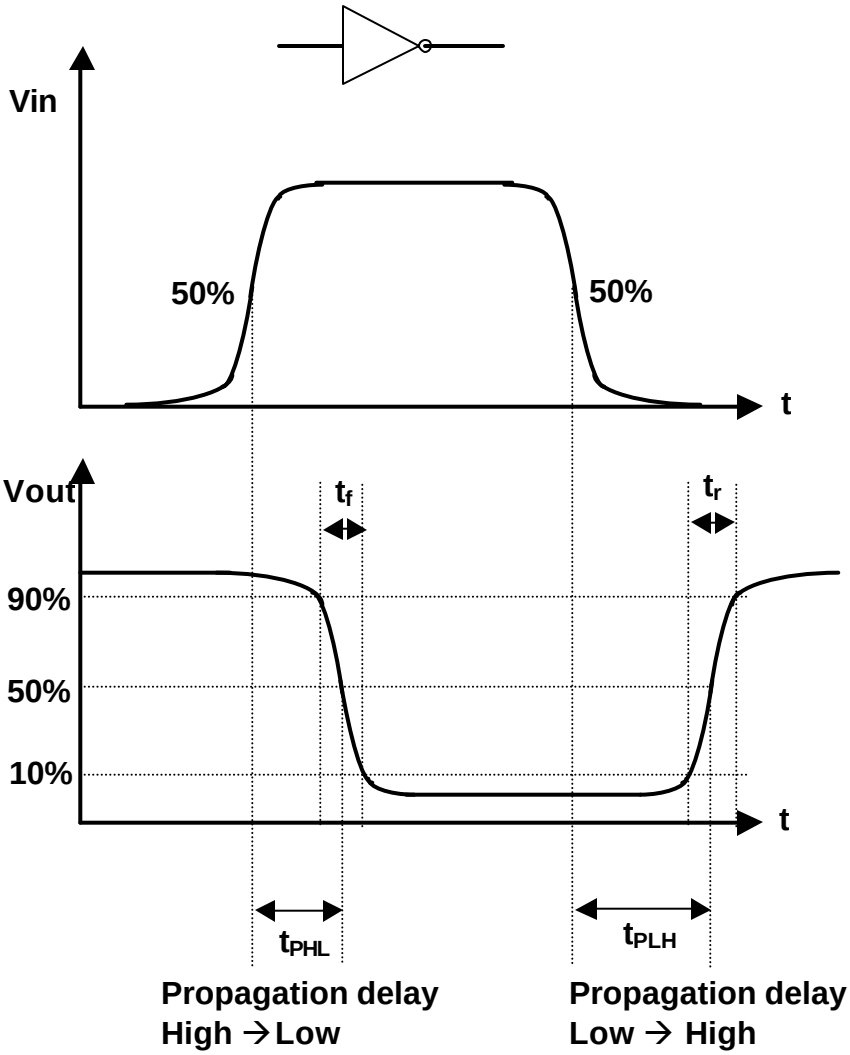
} Fan-out ?

Performance

Clock frequency of a logic circuit ? gate propagation time

? register read/write time

? uncertainty of clock arrival time



Propagation delay

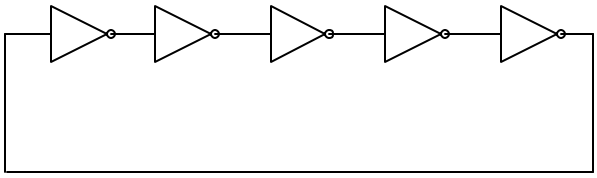
$t_p = (t_{PLH} + t_{PHL}) / 2$ (average response time of a gate)

t_r, t_f ? depend on strength of driver + load presented to it

Measuring t_p

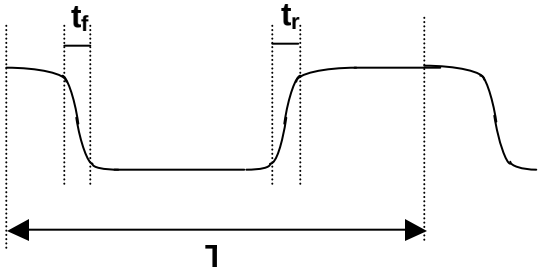
Uniform way of measuring t_p is by using a ring oscillator

Odd # inverters (at least 5)



Period of oscillation frequency, $T = 2 \times t_p \times N = N(t_{PLH} + t_{PHL})$

valid when $2Nt_p \gg t_f + t_r$, $T \gg t_f + t_r$



Ring oscillator frequency (5 inverters) 5GHz ? T = 200psec ? t_p = 20psec

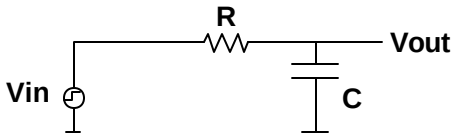
does not mean CICTS work up to 50 GHz

inverter ? no parasitics, no coupled gate, no extra interconnect, no fan-in/fan-out

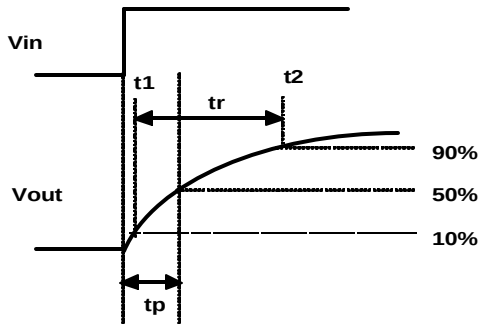
achievable clock frequency ~ 1/50 1/100 of 50GHz

careful optimized design could be better

t_r, t_f, t_p for RC network



$V_{out} = (1 - e^{-t/t}) V_{in}$, t = RC time constant



to calculate t_p

$V_{out} = V_{in}/2$? $e^{-t/t} = ½$? $-t/t = \ln ½$

$t_p = t \ln 2 = 0.69t$

to calculate t_r

$t_1 : V_{out} = 0.1 V_{in}$ $t_2 : V_{out} = 0.9 V_{in}$

$e^{-t/t} = 0.9$ $e^{-t/t} = 0.1$

$-t/t = \ln 0.9$ $-t/t = \ln 0.1$

$t_1 = t \ln 1.11$ $t_2 = t \ln 10$

$t_r = t_2 - t_1 = t(\ln 10 - \ln 1.11) = t \ln 9 = 2.2\,t$