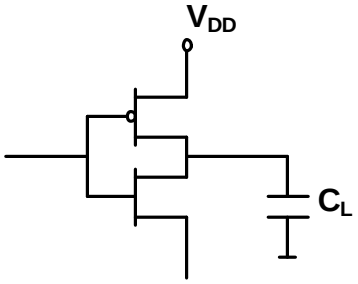
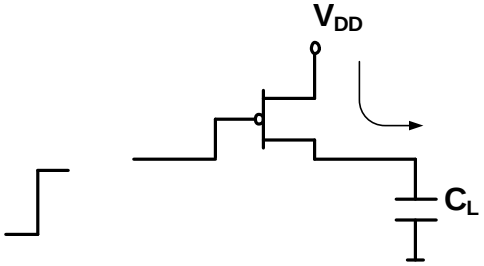
Power consumption in CMOS inverters

*Dynamic power



Assume zero rise and fall time

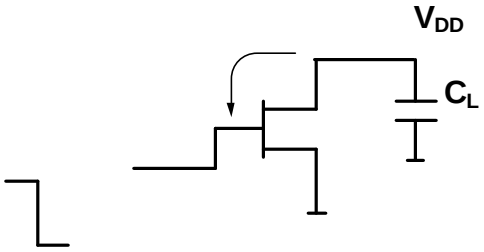


$E_{VDD} = C_L V_{DD}^2$ ½ energy stored in C_L

$E_C = \frac{C_L V_{DD}^2}{2}$ ½ energy consumed in PMOS

→ independent of $R_{transistor}$

but depends on size



$E_C = \frac{C_L V_{DD}^2}{2}$ consumed in PMOS

→ independent of of $R_{transistor}$

but depends on size

→ for each cycle $E_C = E_{VDD} = C_L V_{DD}$

$P_{dynamic} = E\, f_{0\to1} = C_L V_{DD}^2 f_{0\to1}$

*in a logic CKT → total load caps , $C_L = \sum C_L$

$P_{dynamic} = C_L V_{DD}^2 f_{0\to1}$ → but not all the gates activated together

$P_{dynamic} = C_L V_{DD}^2 f_{0\to1} = C_L V_{DD}^2 f P_{0\to1}$ P : probability of activation

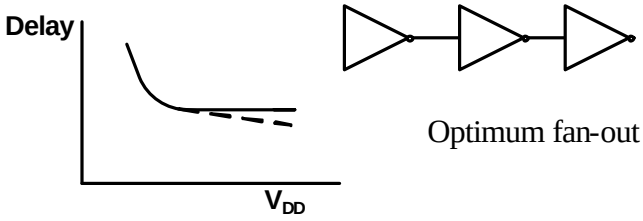
$= C_{eff} f V_{DD}^2$ effective capacitance $C_{eff} = C_L P_{0\to1}$ $P_{0\to1}$ may be 10% never 100%

To reduce P_{dyn} : VDD↓ power supply reduction

CL ↓ reduction of gate caps → use minimum size where possible

$P_{0\to1}$ ↓ reduction of switching activity

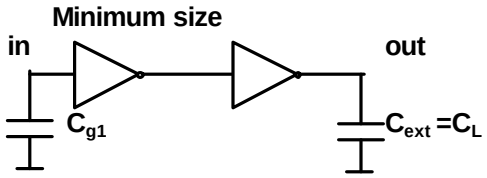
VDD/Transistor sizing for minimum power



Optimum fan-out = f=4

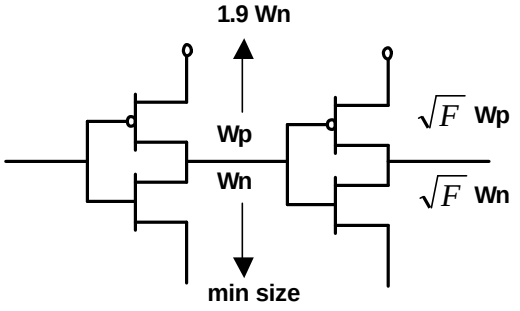
How about effect of VDD and transistor sizing on power?

Simple case : fixed # of stages = 2

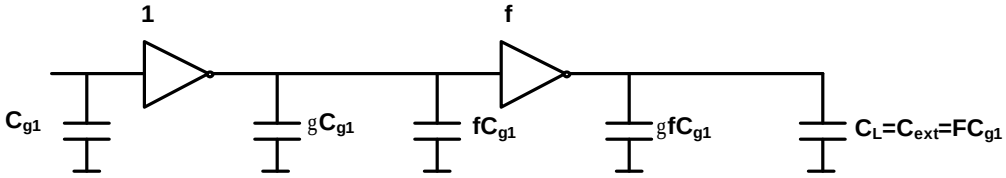


$$F = \frac{C_{ext}}{C_{g1}} \quad \text{for minimum delay} \quad f = \sqrt[2]{F}$$

to get min delay



$$t_p = t_{p0}\left[\underbrace{\left(1+\frac{f}{g}\right)}_{first\cdot inverter} + \underbrace{\left(1+\frac{F}{fg}\right)}_{second\cdot inverter}\right]$$

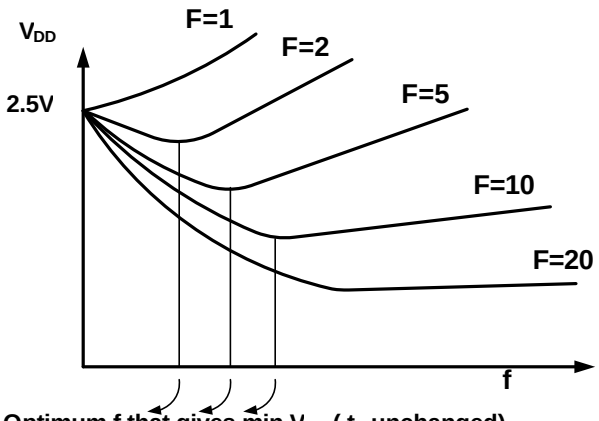


$$C_{tot} = C_{g1} + gC_{g1} + fC_{g1} + gfC_{g1} + C_{ext} = C_{g1}\left((1+g)(1+f)+F\right)$$

$$\rightarrow \; E_{tot} = V_{DD}{}^2 C_{tot} = V_{DD}{}^2 C_{g_1}\left((1+g)(1+f)+F\right)$$

$$t_{p0} \approx \frac{V_{DD}}{V_{DD} - V_T - \frac{V_{Dsat}}{2}}$$

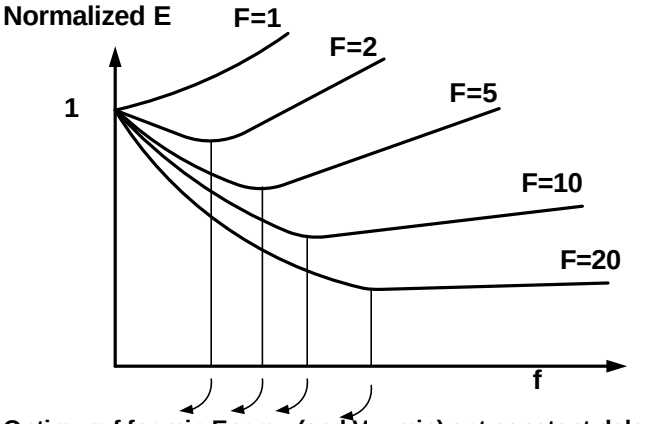
For a given effective fan-out (F), there is an optimum fan-out of each stage (f), that can give you a min V_{DD} while t_p is unchanged



(constant delay)

$$t_p = t_{p0}\left(2 + \frac{f}{g} + \frac{F}{fg}\right)$$

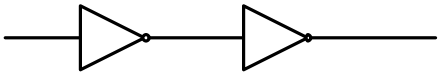
Optimum f that gives min V_{DD} (t_p unchanged)



Constant delay

Optimum f for min Energy (and V_{DD} min) get constant delay

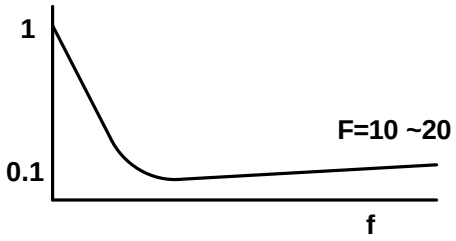
assume γ=1



F	f_{opt} for E_{min}	V_{DDmin} for E_{min}	Normalized E_{min}	f_{opt} for min delay	T_p min
1	1	2.5	1	1	$4t_{p0}$
2	1.3	2.22	~ 0.88	1.41	$4.82t_{p0}$
5	1.9	1.47	~ 0.44	2.26	$6.52t_{p0}$
10	2.5	~ 1.05	~ 0.24	3.17	
20	3.53	~ 0.77	~ 0.12	4.47	$10.94t_{p0}$

Conclusion of Power optimization

*device sizing + V_{DD} reduction can reduce energy consumption, especially for F↑



for F↓ still we get improvement

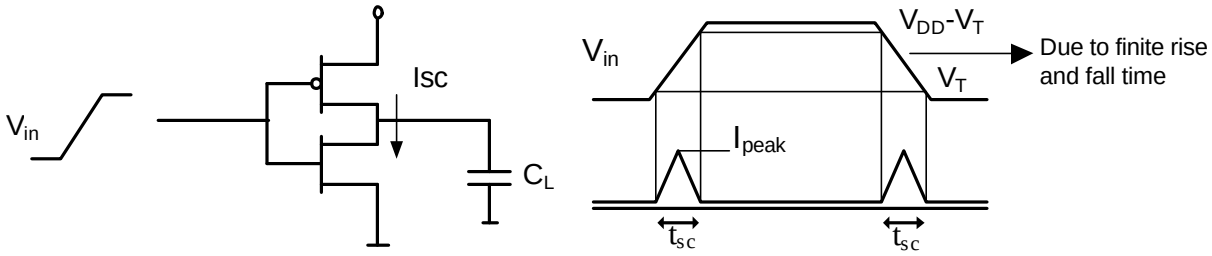
for F↑ → minimize size/V_{DD}=2.5 is the optimum

*oversizing transistor beyond optimum value

→ E↑↑

* optimum sizing for energy is smaller than for delay

Dissipation due to direct path current



$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

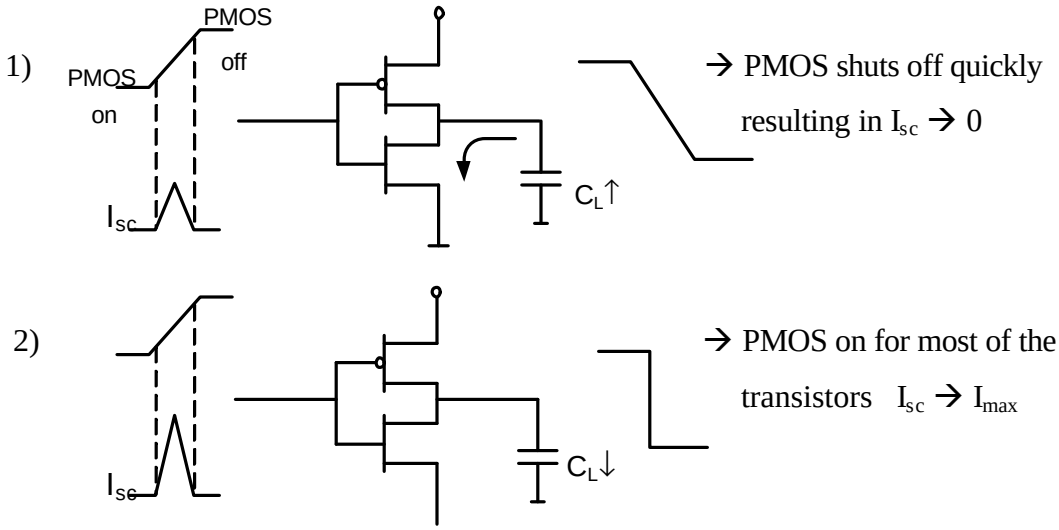
$$P_{dp} = \underbrace{t_{sc}\cdot V_{DD}\cdot I_{peak}}_{\text{Energy}} \cdot \underbrace{f_{0\to1}}_{\text{switching activity}}$$

$$t_{sc} = \frac{V_{DD} - 2V_T}{V_{DD}} \cdot \frac{t_{r(f)}}{0.8}$$

I_{peak} → depends on device size.

It is also a strong function of the ratio between input & output slopes

Consider 2-cases



→ make rise/fall time large to reduce direct path energy !

→ t_r, t_f ↑ → increased energy for the fan-out gate!!

Solution → optimum case for all the gates → $t_r, t_f \mid_{input} = t_r, t_f \mid_{output}$

→ effect of direct path current can be modulated by adding a load capacitance

$C_{sc} = \frac{t_{sc}I_{peak}}{V_{DD}}$ in parallel with C_L.

↳ (a function of transistor size, input/output slope ratio and V_{DD})

Static Power Consumption

$P_{stat} = I_{leakage} V_{DD}$

↓

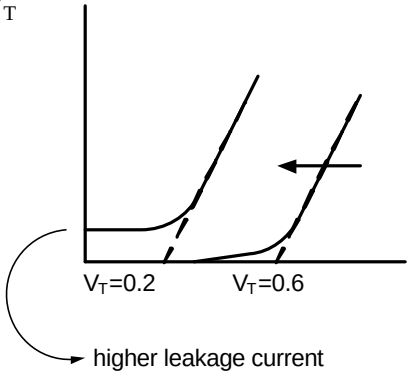
during no switching activity

$I_{leakage}$ = 10 ~ 100pA/μm^2 @ room temp

1 million gate each 0.5μm^2, V_{DD} = 2.5 V → P_{stat} ~ 0.125mW

@ 85?C → $I_{leakage}$ → 60X → P_{stat} = 7.5mW

Other problem → small V_T



$$P_{tot} = P_{dyn} + P_{dp} + P_{stat} = (C_L V_{DD}^{\ 2} + V_{DD} I_{peak} t_{sc}) f_{0\to 1} + V_{DD} I_{leakage}$$

Power-delay product : PDP = P_{av} t_p

ignoring P_{dp}, P_{stat} → $PDP = \frac{C_L V_{DD}^{\ 2}}{2}$

→ not a good measure since can be minimized by V_{DD} ↓

Energy delay product : $EDP = \frac{C_L V_{DD}^{\ 2}}{2} t_p$ → $V_{DDopt} = \frac{3}{2}\left(V_T + 2\frac{V_{Dsat}}{}\right) \approx 1.2V$