Devices

- Semiconductor Physics review
- Diode
- MOS transistor

Semiconductor Physics

Charge carriers in semiconductors : electrons, holes

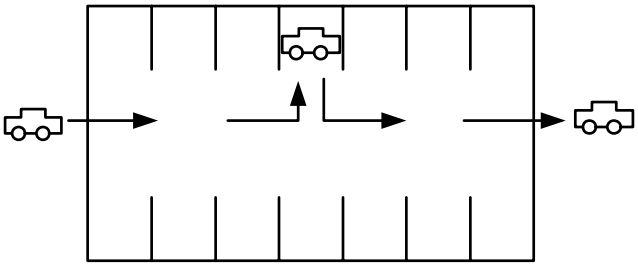
Why do we consider holes?

→ In metals, there are so many electrons that we don't really care about holes .

→ Metals are often conductor.

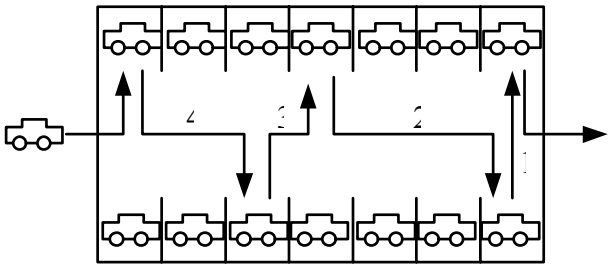
→ In semiconductor, number of free electrons may not be a lot but you will still see some condition which is due to holes.

Empty parking lot

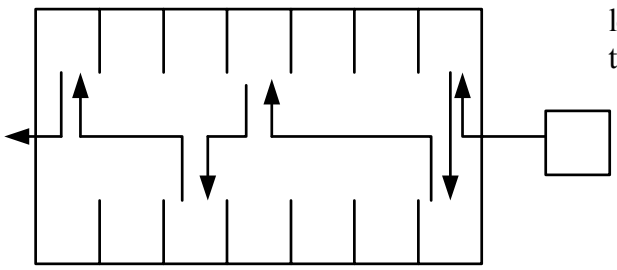


→Fast process

Full parking lot



→Much slower process



→If you look at the empty space it looks like empty space is moving in the other direction.

→ This is the concept of hole and why it is slower.

NMOS transistor → conduction using electrons, much faster devices

PMOS transistor → conduction using holes, slow devices

Semiconductors

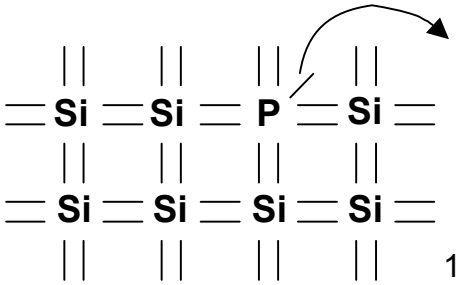
Intrinsic → # of holes ≈ # of electrons, pure semiconductors are intrinsic

N-type → # of electrons >> # of holes

P-type → # of electrons << # of holes

How to make n-type

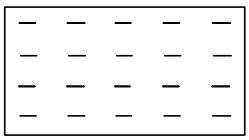
Add impurities that have an extra electron to give



Extra electron becomes a free electron with a very small energy received from thermal energy.

$10^{23}/cm^3$ Si atom

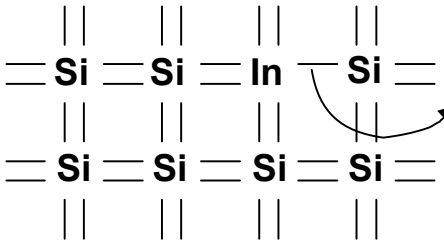
If you have $10^{19}/cm^3$ P you get a very good conductor.



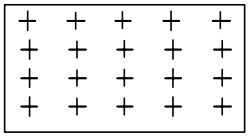
→ Material is neutral for every free electron

There is a positive charged ion (P).

How to make p-type



Empty space , a hole is generated.

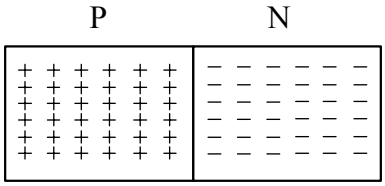


→ Material is neutral for every free holes

There is a negative charged ion (In).

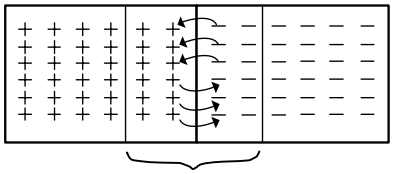
Diode

Diode is made when you connect an N-type and P-type semiconductors together.



What happens next?

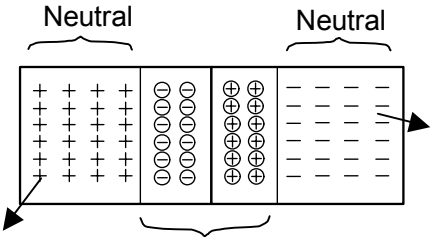
There will be a current flowing since positive and negative free charges attract each others and recombine. → Electron fills up the hole.



No free electron or hole but ions are there so material is charged

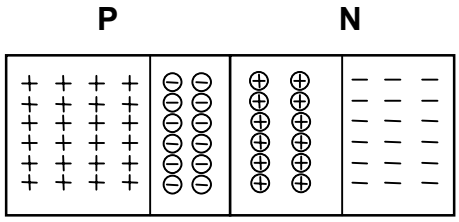
N_D : number of free electrons in N-type (Donor)
= number of charged ions
~ number of n- impurity

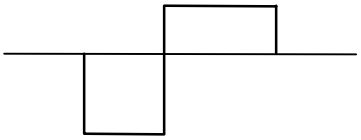
N_A : number of free holes in P-type (Acceptor)
= number of charged ions
~ number of p- impurity



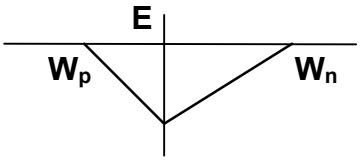
→ There is an electric field in the depletion region. → Generates a potential

Now electron and holes cannot go to the opposite side unless give them enough potential to go through the depletion region.



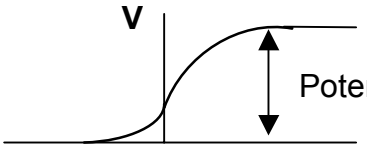


Uniform charge

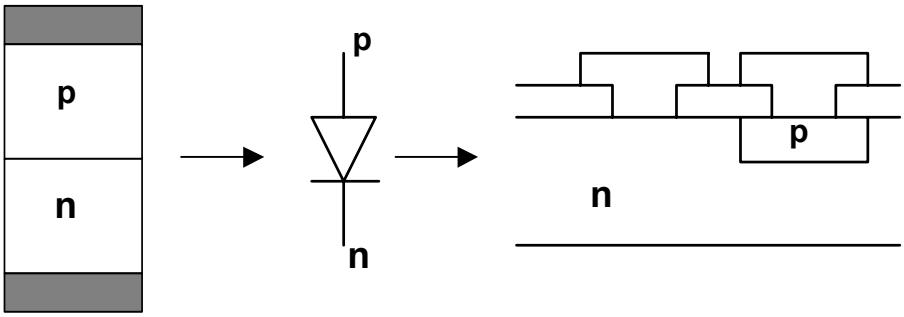


Linear e-field

integrate

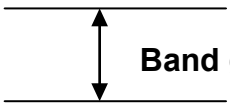


Potential difference



Potential : $\phi_0 = \frac{kT}{q} \ln(\frac{N_A N_D}{n_i^2})$

n_i : intrinsic # of carriers, depends on temperature and Bandgap

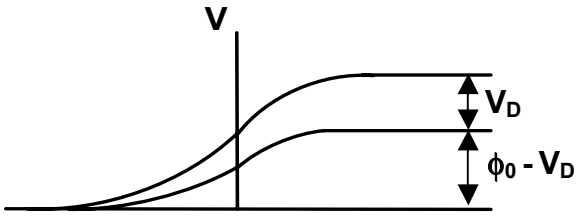


$n_i \propto T, \quad \propto 1/\text{Bandgap}$

For Si $n_i = 1.5 \times 10^{10}\ cm^{-3}$ @300k $\frac{kT}{q} = 26$ mV

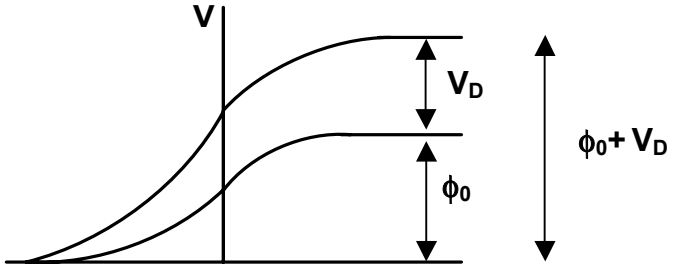
Apply external voltage V_D

If it lowers ϕ →



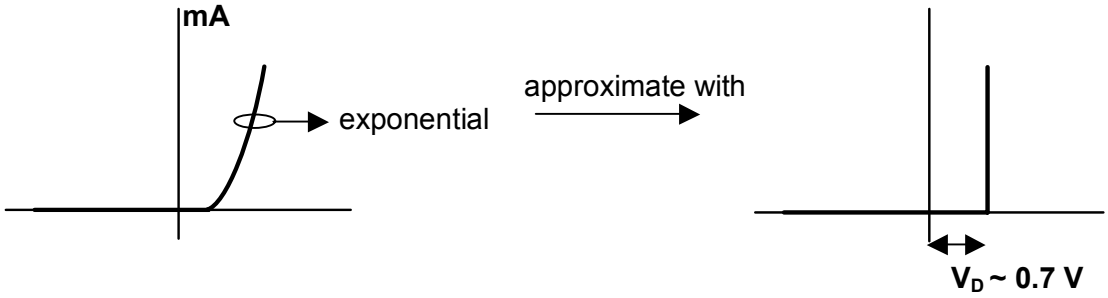
→ depletion layer shrinks → diode starts to conduct.

If it increases ϕ →



→ depletion layer increases → diode does not conduct.

Diode current $= I_D = Is\ (e^{qv/kT} - 1)$



In reality there is also voltage drop due to resistances of diode

$I_D = Is\ (e^{qv/nkT} - 1)$ current is smaller than ideal case

n : emission factor (ideality factor), $n > 1$

Dynamic behavior of diode

Diode capacitance $C_j = \varepsilon_{si} \frac{A}{Wj}$

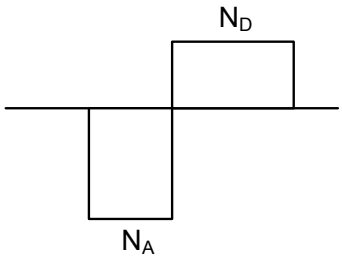
ε_{si} : Si dielectric constant, A : diode area

W_j : depletion region(W_N+W_P) , $W_j = \sqrt{\frac{2\varepsilon}{q}(\frac{1}{N_A}+\frac{1}{N_D})(\phi_0 - V_D)}$

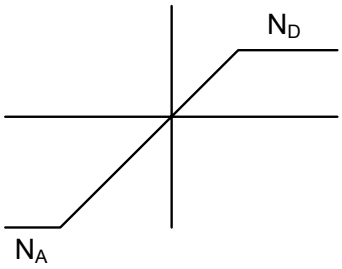
$C_{j0} = A\sqrt{\frac{\varepsilon q}{2}(\frac{N_A N_D}{N_A + N_D})\frac{1}{\phi_0}}$ → potential capacitance, V_D=0

$C_j = \frac{C_{j0}}{(1-\frac{V_D}{\phi_0})^m}$ m : grading coefficient

m=1/2 abrupt junction



m=1/3 graded junction



abrupt → usually with epitaxial layer

graded junction → achieved by diffusion

Large signal equivalent capacitance

$C_{eq} = \frac{\Delta Q}{\Delta V_D} = K_{eq} \cdot C_{j0}$

K_{eq} = look at the formula in the book

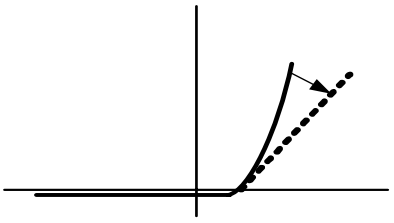
$C_{jhigh} = \frac{C_{j0}}{(1-\frac{V_{high}}{\phi_0})^m}$, $Q_{high} = \text{const} \cdot (\phi_0 - V_{high})^{1/m}$

$C_{jlow} = \frac{C_{j0}}{(1-\frac{V_{low}}{\phi_0})^m}$, $Q_{low} = \text{const} \cdot (\phi_0 - V_{low})^{1/m}$

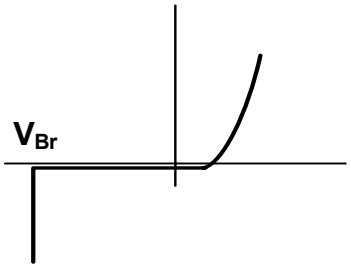
C_{j0} → $Q = \text{const} \cdot \phi_0^{1/m}$

Actual diode

→ resistivity of neutral zones



→ Break down voltage



→Temperature variation : kT/q ~ , Is ~

Spice diode model

IS : Saturation current

N : Emission factor(ideality factor)

RS : Series resistance

TT : Transit time → $C_D = \frac{C_{j0}}{(1-\frac{V_D}{\phi_0})^m} + \frac{\tau_T I_s e^{\frac{qVD}{nkT}}}{\frac{kT}{q}}$

↳ forward bias cap due to minority charging

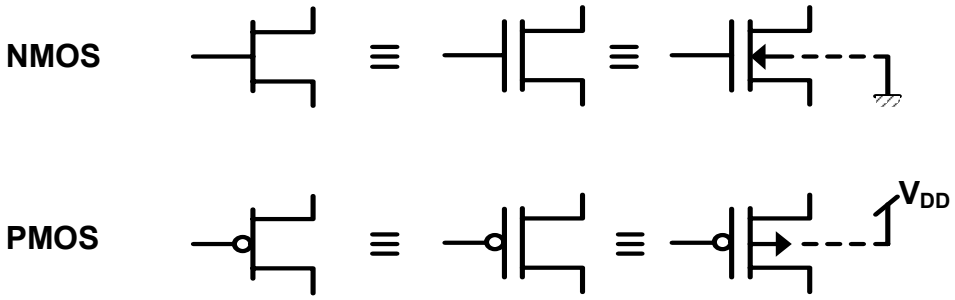
CJ0 : zero bias cap

M : Grading coefficient

VJ : (ϕ_0) junction potential

MOS (Metal-Oxide-Semiconductor)

MOSFET(MOS Field Effect Transistor)

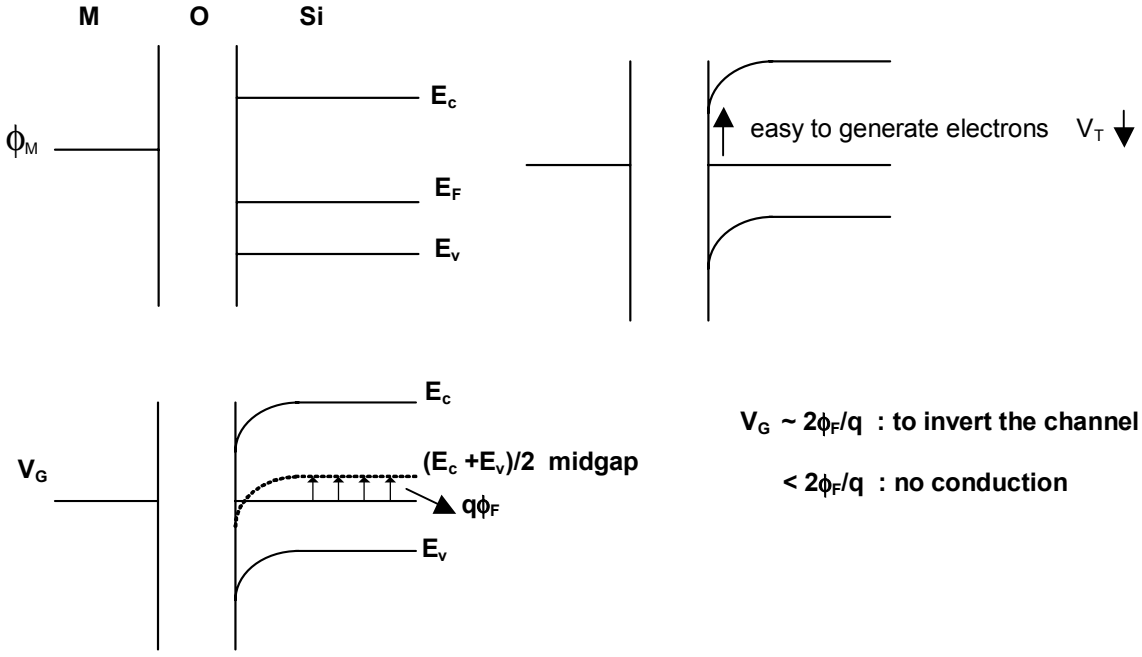


MOS are unipolar transistor : Only one carrier of charge exists

Hole → PMOS

Electron → NMOS

Technology that has both PMOS + NMOS = CMOS (Complementary MOS)



Thickness of induced charges , Wd = $\sqrt{\frac{2\varepsilon\phi}{qN_A}}$ Total charge, Q = $\sqrt{2qN_A\varepsilon\phi}$

ϕ : potential at Si-SiO_2 interface

Inversion layer

Fixed charge $Q_{B0} = \sqrt{2qN_A\varepsilon|2\phi_F|}$

If the body is not grounded V_{SB}, $|2\phi_F| \rightarrow |-2\phi_F + V_{SB}|$

V_{GS} needed to reach strong inversion is called Threshold Voltage.

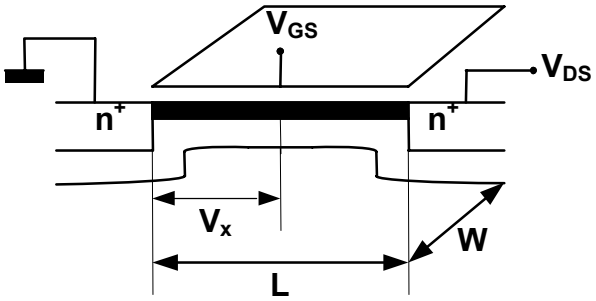
$V_T = V_{GS}$ (@ strong inversion)

$V_T = V_{T0} + \gamma\sqrt{|-2\phi_F + V_{SB}| - |2\phi_F|}$, γ : body-effect coefficient

V_{TO} : related to the process how Fermi level and material work function are aligned

→ Threshold voltage varies with substrate bias !

Small V_{DS} (V_D << , V_{GS} >> V_T) → Resistive operation



Induced charge, $Q_i(x) = -C_{ox}$ ($V_{GS} - V_x - V_T$), $Cox = \frac{\varepsilon_{ox}}{t_{ox}}$

$I_D = -v_n(x)\, Q_i(x) W$, $v_n(x)$: electron velocity at x,

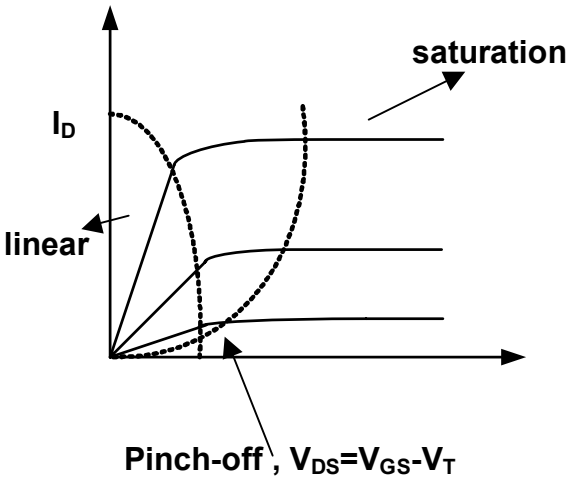
$v_n = \mu_n \frac{dV}{dx}$, μ_n: electron mobility

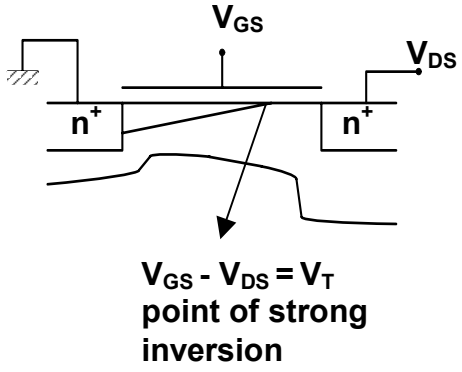
$Q_i(x)$: mobile charge, W : width of the channel

$$\int_0^L I_D dx = \int_0^{V_{DS}} \mu_n C_{ox} W (V_{GS} - V - V_T) dV$$

$$I_D = k'_n \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$ k'_n : transconductance factor

$$I_D = k_n\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$ gain factor $k_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$





In saturation, $V_{DS} = V_{GS} - V_T$, $I_D = \frac{k'n}{2}\frac{W}{L}(V_{GS} - V_T)^2$

$I_D \rightarrow$ constant (not a function of V_{DS} to first degree approximation)

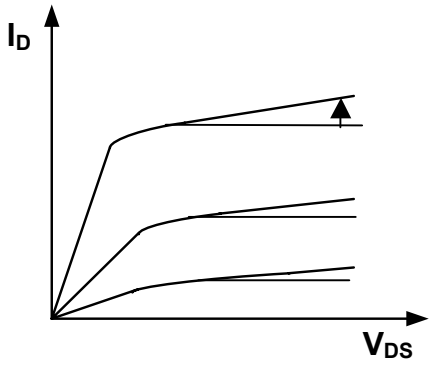
Why current at pinch-off stays constant?

$I_D \downarrow \rightarrow$ pinch-off disappears $\rightarrow I_D \uparrow$

$I_D \uparrow \rightarrow$ more depletion $\rightarrow I_D \downarrow$

Small size transistor

$V_{DS} \uparrow \rightarrow$ depletion region at drain $\uparrow \rightarrow L_{eff}$ changes

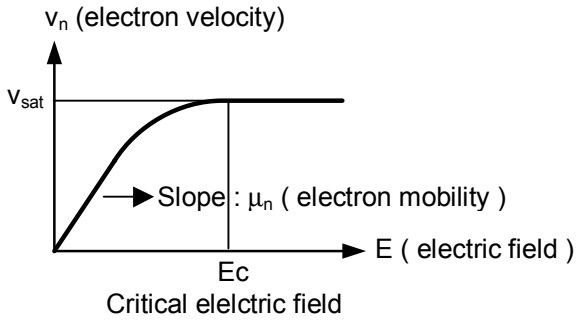


$I_D = I_D' (1 + \lambda V_{DS})$

λ: channel length modulation

There are other problems with small size transistors.

Velocity saturation



In small size (sub-micron) devices, electric field can be very large $E = \frac{V_{DS}}{L}$

→ crude approximation since E distribution is not uniform.

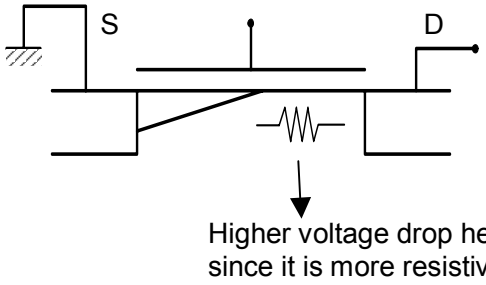
$I_D = I_D' \cdot k(V_{DS})$ I_D' : current that we calculate before

$k(V_{DS}) \leq 1$ shows degree of velocity saturation

For short-channel devices $k(V_{DS}) < 1$

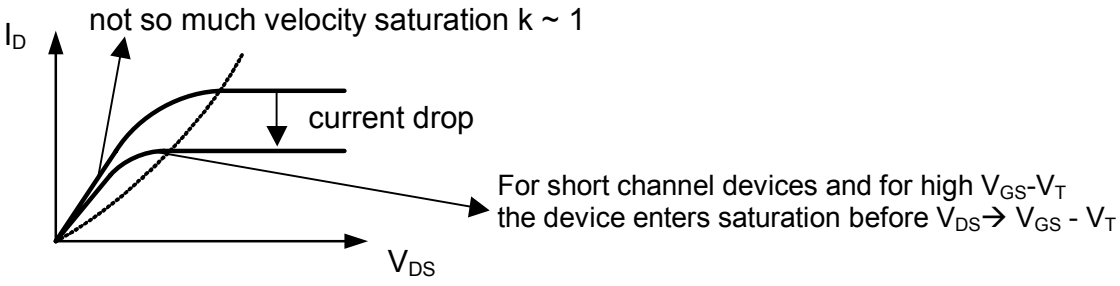
→ current is smaller but overall for very small $V_{DS} \approx 1$ and $I_D \rightarrow I_D'$.

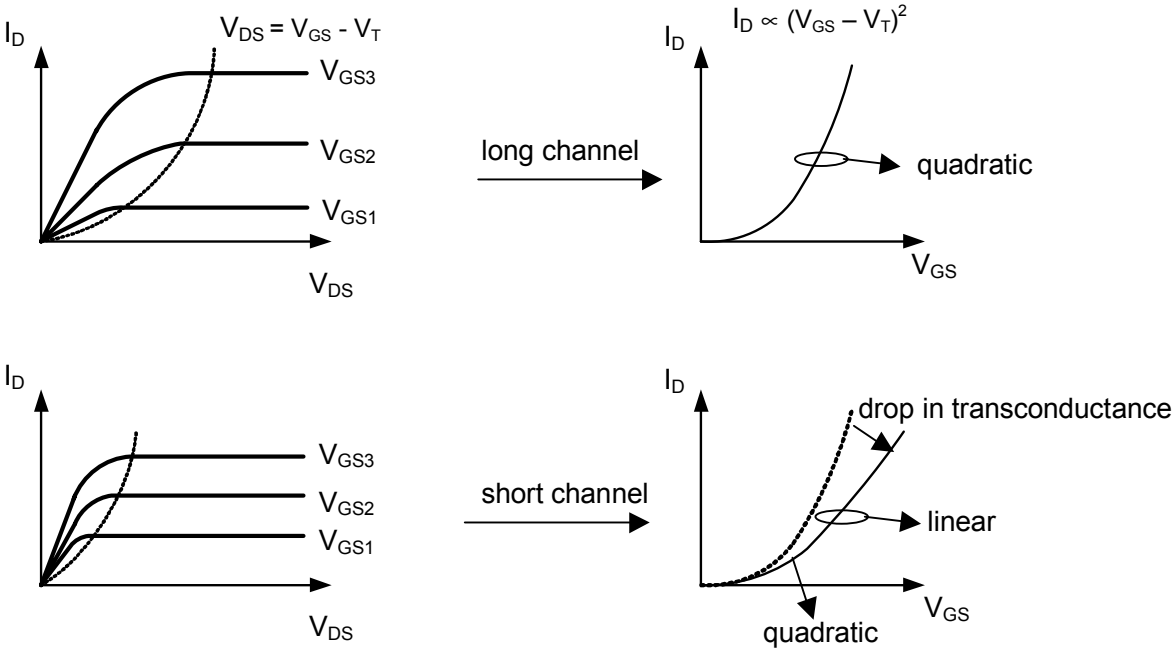
Velocity saturation first starts at drain part since there is higher electric field.



$$\rightarrow V_{DS} = V_{Dsat} \rightarrow I_{Dsat} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \cdot k(V_{Dsat})$$

I_{Dsat} is not a function of V_D so current is saturated once we hit velocity saturation limit.

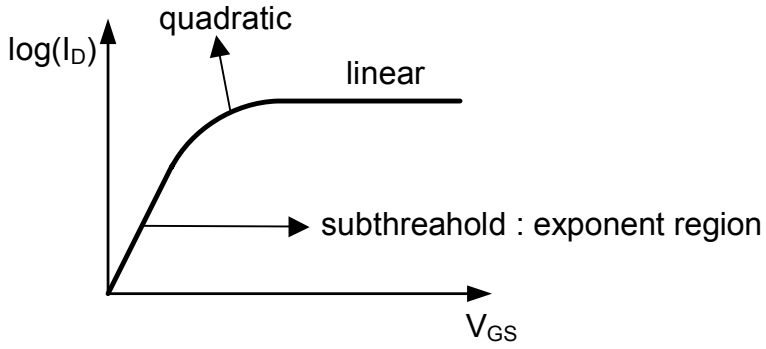




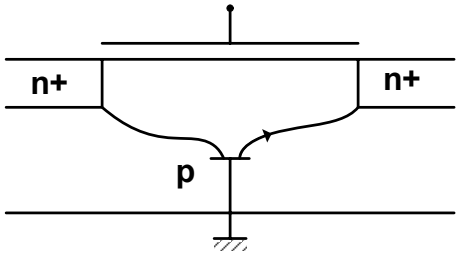
Subthreshold condition

In digital circuits it is undesired → means leakage (not such a good switch)

→ additional power consumption.



Subthreahold → no conducting channel



subthreshold slope

$$S = n\frac{kT}{q}\ln 10$$

n : ideality factor of

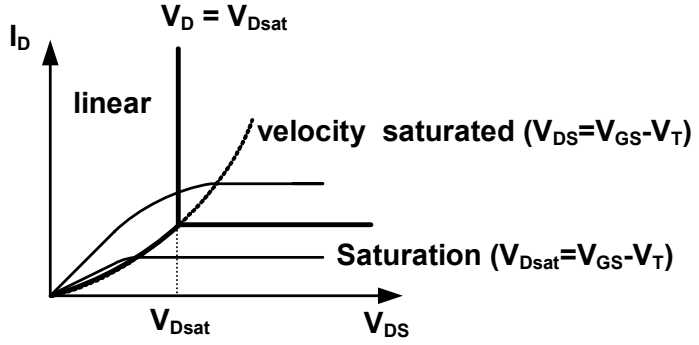
the parasitic bipolar transistor

Unified MOS Model

$I_D = 0$ for $V_{GS} - V_T < 0$ → zero subthreshold conduction

$$I_D = k'_n \frac{W}{L}\left[(V_{GS} - V_T)V_{min} - \frac{V_{min}^{\ 2}}{2}\right](1 + \lambda V_{DS}) \qquad \text{for } V_{GS} - V_T > 0$$

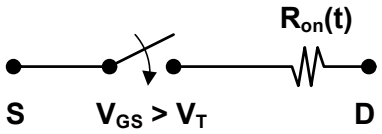
$$V_{min} = \min(V_{GS} - V_T, V_{DS}, V_{Dsat})$$



$$V_T = V_{T0} + \gamma\left(\sqrt{|1 - 2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right), \quad \gamma : \text{body-effect coefficient}$$

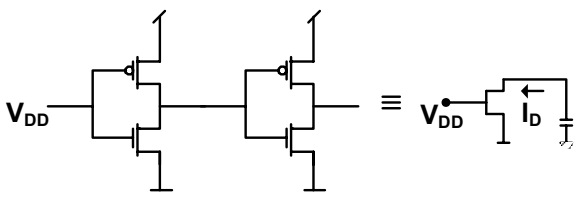
live parameter : V_{T0}, γ, V_{Dsat}, k', λ

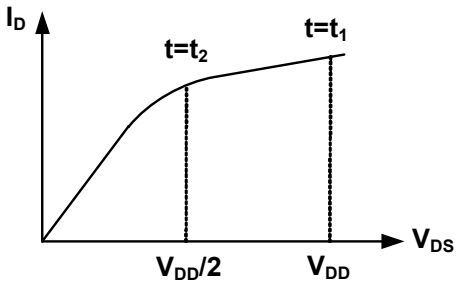
MOS model as a switch



Problem is that Ron is time varying, non-linear and bias dependent.

Finding R_{eq} from $R_{on}(t)$ $\qquad R_{eq} = \dfrac{1}{(t_2 - t_1)}\displaystyle\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)} dt$





$$R_{eq} = \frac{1}{(t_2 - t_1)} \int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)} dt$$ assuming velocity saturation from $V_{DD} \rightarrow V_{DD}/2$

changing variable from t to V

$$R_{eq} = \frac{1}{(V_{DD}/2 - V_{DD})} \int_{V_{DD}}^{V_{DD}/2} \frac{V_D}{I_{DS}(1-\lambda V)} dV$$

$$I_D = k'_n \frac{W}{L}\left[(V_{DD} - V_T)V_{Dsat} - \frac{{V_{Dsat}}^2}{2}\right](1 + \lambda V) = I_{DS}(1+\lambda V)$$

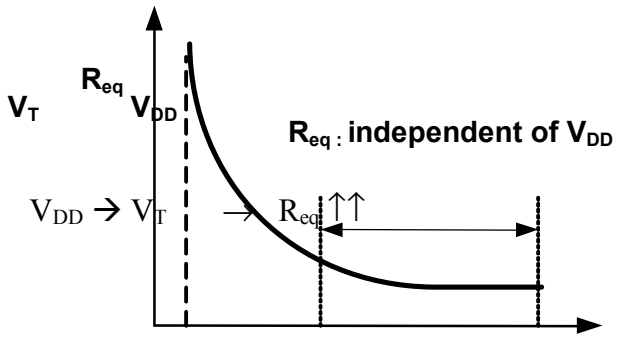
For small λ $\quad \frac{1}{1+\lambda V} = 1 - \lambda V$

$$R_{eq} = \frac{-2}{(V_{DD} I_{DS})} \int_{V_{DD}}^{V_{DD}/2} V(1-\lambda V) dV = \frac{-2}{V_{DD} I_{DS}} \left(\frac{V^2}{2} - \lambda \frac{V^3}{3}\right)\Bigg|_{V_{DD}}^{V_{DD}/2}$$

$$= \frac{-2}{V_{DD} I_{DS}} \left[\frac{\frac{{V_{DD}}^2}{4} - {V_{DD}}^2}{2} - \lambda \frac{\frac{{V_{DD}}^3}{8} - {V_{DD}}^3}{3}\right] = \frac{2}{I_{DS}} \left(\frac{3V_{DD}}{8} - \frac{7}{24}\lambda {V_{DD}}^2\right)$$

$$= \frac{3}{4} \frac{V_{DD}}{I_{DS}} \left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

$$R_{eq} \propto \frac{1}{I_D} \propto \frac{1}{W/L}$$ increase W/L $\rightarrow$ $R_{eq} \downarrow$


R_{eq}
V_T
V_{DD}
R_{eq} : independent of V_{DD}
$V_{DD} \rightarrow V_T$
$\rightarrow$ $R_{eq} \uparrow\uparrow$