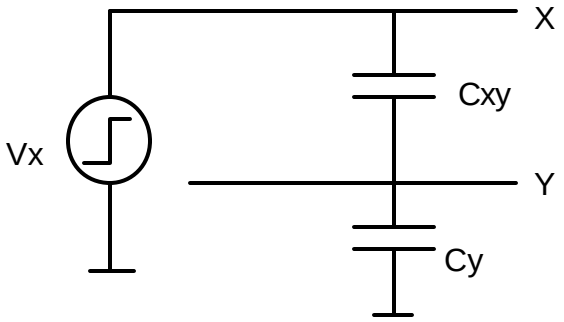
Interconnect:

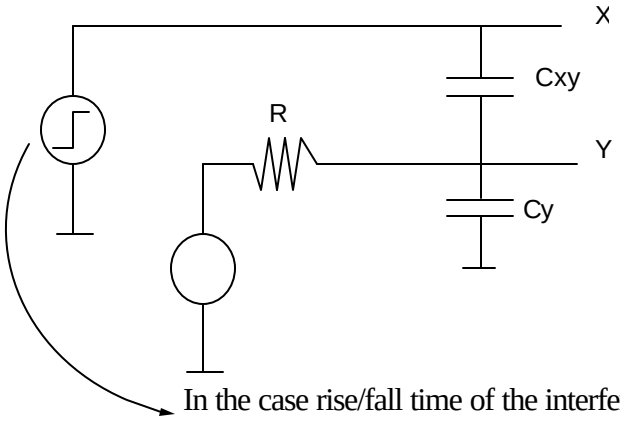
Capacitive Crosstalk

→ important for high impedance nodes

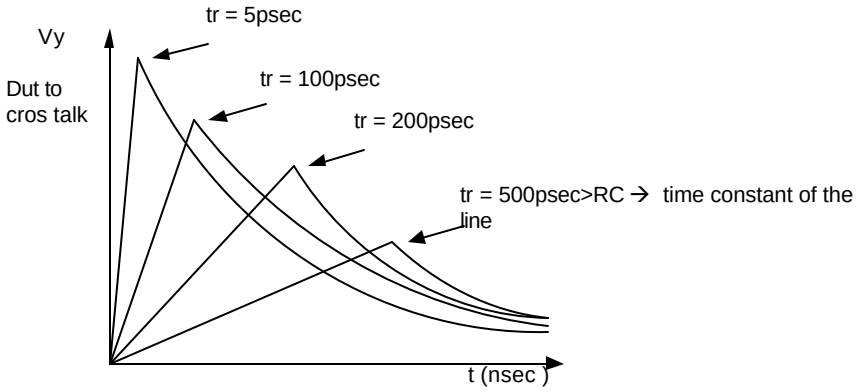


$$\Delta Vy = \frac{Cxy}{Cy + Cxy}\Delta Vx$$

but usually line y is driven with a finite resistance R



In the case rise/fall time of the interfering signal is important and you want slow rise/fall time



So if maximum speed is not required, rise time and fall time can be increased to decrease the effect of cross-talk → higher rise/fall time → higher power consumption (direct path)

Design techniques to reduce cross-talk

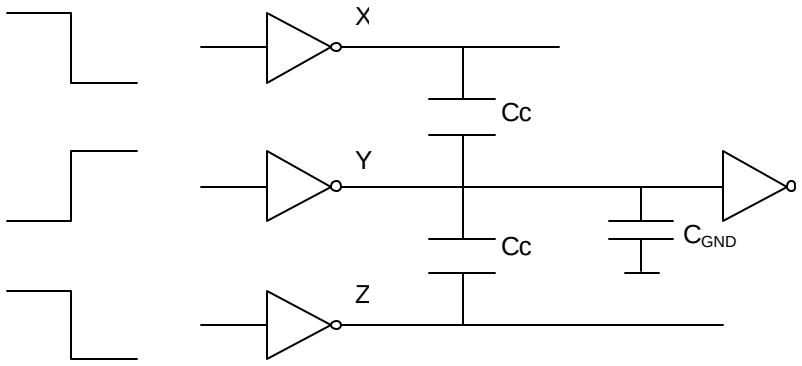
1. avoid floating nodes
2. separate high impedance nodes from full-swing signals
3. increase rise/fall time subject to timing constant and direct path power
4. use differential signaling in sensitive low-swing wiring network
   → cross-talk is common signal and will be rejected
5. do not allow high cap. between two signal wires
   (layout technique : have the wires run on different metallization)
6. provide shielding wire (GND,V_{DD}) between two signal lines

Effect of cross-talk on performance

Cross-talk affects the timing performance of the circuit and is not just unwanted coupling(noise)

Example

Exactly at the same time



Worst case : signal at Y is in opposite phase with X and Y

→ Due to miller effect, the capacitance seen by point Y is

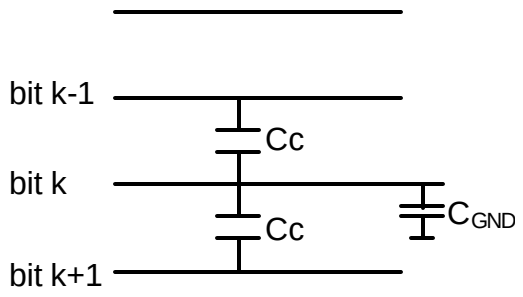
$$C_L = C_{GND}+2C_c+2C_c = C_{GND}+4C_c \leftarrow \text{worst case}$$

If X,Y,Z are stationary or even for signals with same phase coming at the same time

$$C_L = C_{GND} \leftarrow \text{beat case}$$

→ $C_{GND} < C_L < C_{GND}+4C_c$ → so cross-talk can change the propagation delay of signal

Imagine a bus



$$r = \frac{Cc}{C_{GND}}$$

k-1	k	K+1	Delay factor(g)
^	^	^	1
^	^	-	1+r
^	^	v	1+2r
-	^	-	1+2r
-	^	v	1+3r
v	^	v	1+4r

Propagation delay (Elmore delay)

$t_{p,k} = gC_{GND}(0.38R_w+0.69R_D)$

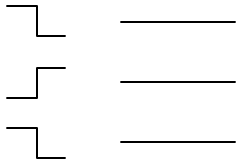
g represents the slow-down due to cross-talk

C_{GND} : wire cap to GND R_w: total wire resistance

R_D: driver resistance

Design techniques to reduce the effect of cross-talk on propagation delay

1. Evaluate and improve → find the bottlenecks from parasitic extraction and adjust the layout to decrease cross-talk (most often used)
2. Constructive layout generation → routing program should understand and avoid large cross-talks → ideal but difficult to implement
3. Predictable structures → use V_{DD},GND shield, Run adjustment wires orthogonal to each other
4. Avoid worst-case pattern



→ use encoder/decoder such that this pattern does not happen

→ delay of encoder/decoder should not exceed the worst-case delay

Capacitive load

Driving capacitive load

* use adequate transistor sizing (driven)

* partitioning driver (gradually increasing buffer)

Multistage buffer

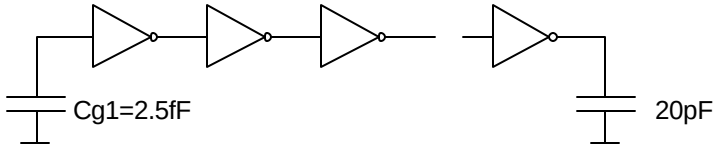
* delay should be divided equally over all stage

* optimum fan-out = 4/stage

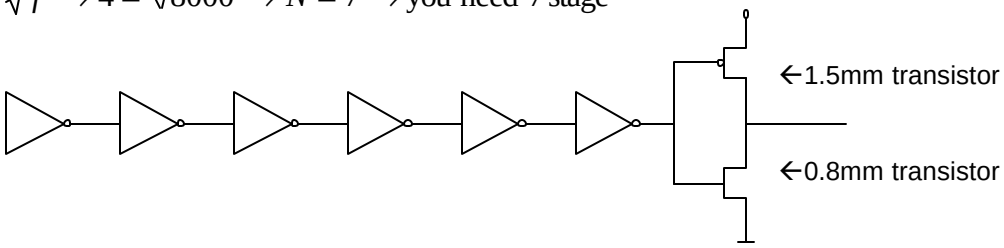
but sometimes the capacitive load is huge (off-chip capacitive load(Pads+long bus wire))

CL → 50pF !!!

$$F = \frac{20\,pF}{2.5\,fF} = 8000$$



$$f = \sqrt[N]{f} \rightarrow 4 = \sqrt[N]{8000} \rightarrow N = 7 \rightarrow \text{you need 7 stage}$$



The size of last stage is too big ! (1.5mm!)

Energy + area ? to achieve high speed

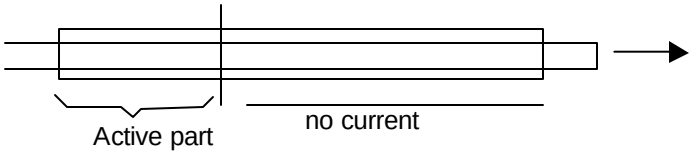
But most often you can trade-off speed for smaller area + lower energy especially because I/O does not have to be very fast.

Now find N/transistor sizing for a given maximum propagation delay time allowed. $t_{p,\max} = t_{p0} \times N \times F^{1/N}$ → find N using numerical techniques

to gat → 2. 5 times slower response in the previous example (7 stage) you only need 3 stage (largest transistor, 284 um)

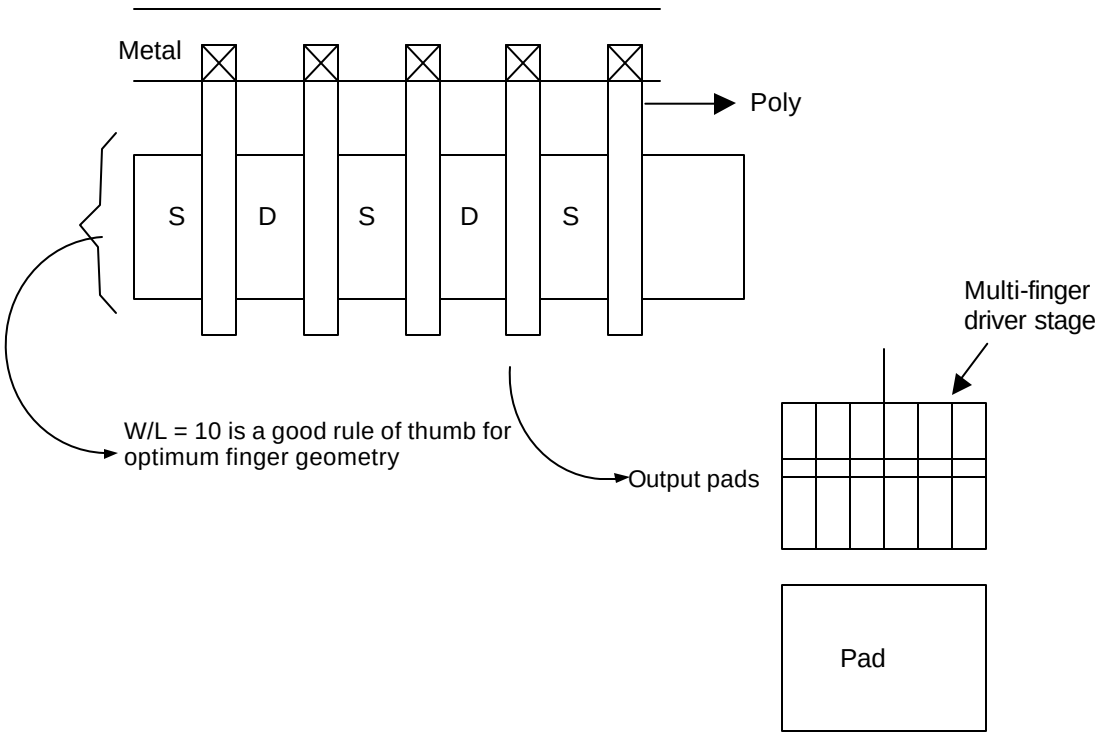
→ design the circuit for right speed NOT the maximum speed

Implementing wide transistor

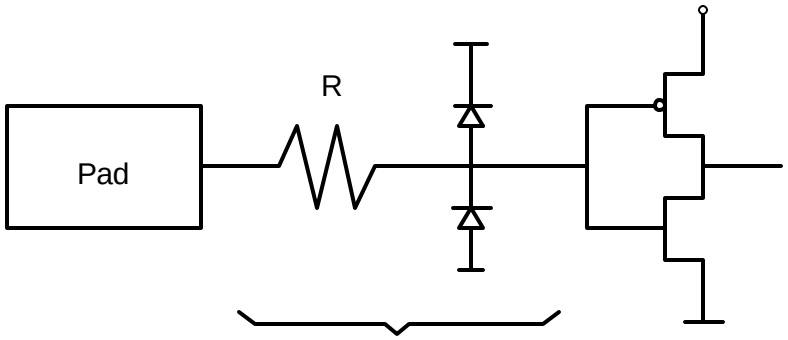


Not a good idea since poly-gate is very resistive and most of the current flow in the small part of transistor

→ use multi-finger



For input pad you need to add ESD protection circuit (Electro-Static Discharge)

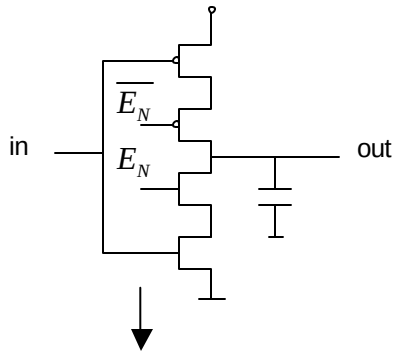


ESD protection slow-downs the circuit

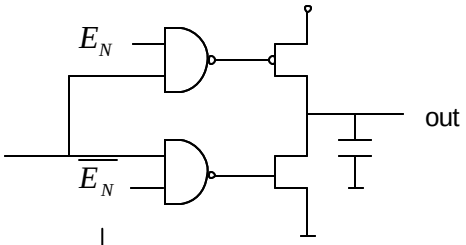
To make sure high voltages dur to electrostatic discharging do not damage the circuit

Tri-State buffer

A lot of time busses are shared among many devices. Therefore the one that is not being need should be in high impedance mode.



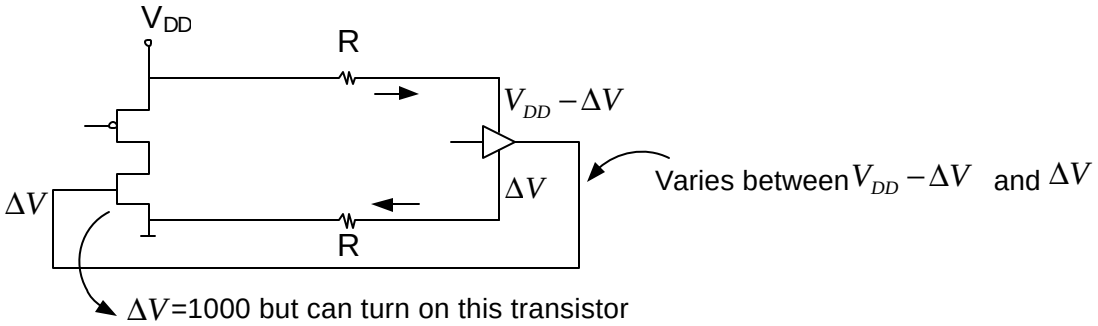
Similar C^2MOS



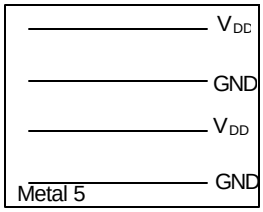
Preferred because output atage uses only 2 transistors(less area!)

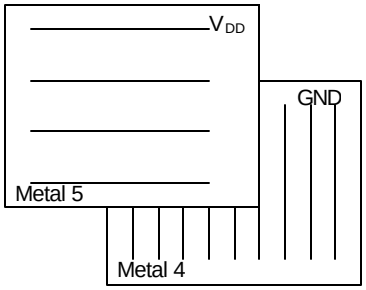
Resistive Parasitics

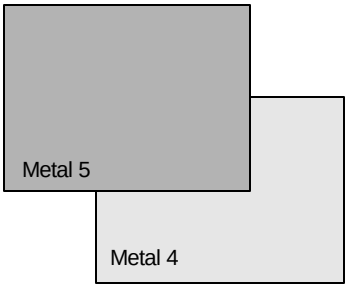
Ohmic drop can reduce noise margin



To avoid the problem distribute V_{DD}, GND







Electromigration

Long-term reliability problem

If in V_{DD} and GND path current is more than 1mA/um width over the line metal ions move → increase resistance → eventually open ckts.

→ This problem does not exist for signal path as current goes in both directions.

→ Cu instead of Al : has much better long term reliability

→ use wide V_{DD}/GND line such that current < 1mA/um

RC delay

→ sometimes you have to use long poly line (dense memories)

→ reduce access resistance by running a parallel metal to poly and connect it every IC cell

to reduce RC delay → shorten the interconnect

→ use 45 degree line → length of line in average 20% shorter