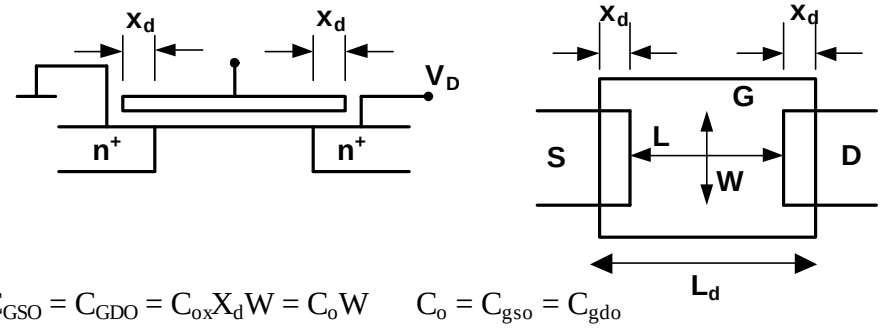
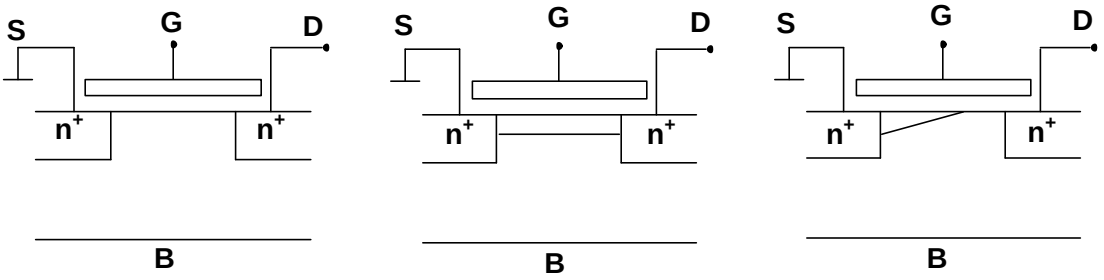
Dynamic Behavior (determined by various capacitors)

Overlap capacitance



$C_{GSO} = C_{GDO} = C_{ox}X_dW = C_oW$ $C_o = C_{gso} = C_{gdo}$

Channel Capacitance

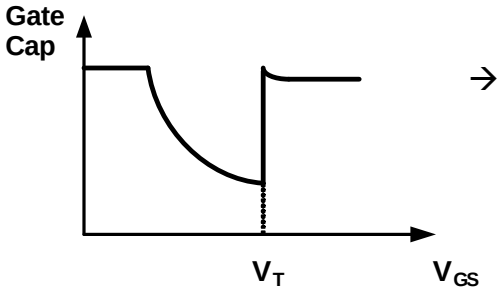


cut-off
$C_{GC} = C_{GB}$
gate gate
channel body

resistive
$C_{GB} = 0$
$C_{GC} = C_{GCS}+C_{GCD}$
uniform channel

saturation
$C_{GC} = C_{GCS}$
$C_{GCD}=0$, $C_{GCB}=0$

	C_{GB}	C_{GCS}	C_{GCD}	C_{GC}	C_G(overlap+channel)
cut-off	$C_{ox}WL$	0	0	$C_{ox}WL$	$C_{ox}WL+ 2C_oW$
resistive	0	$C_{ox}WL/2$	$C_{ox}WL/2$	$C_{ox}WL$	$C_{ox}WL+ 2C_oW$
saturation	0	$2/3\ C_{ox}WL$	0	$2/3C_{ox}WL$	$2/3C_{ox}WL+ 2C_oW$

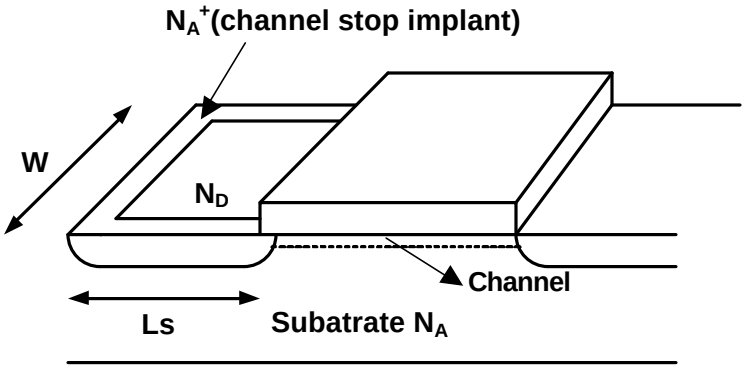


→ around threshold transistor is very non-linear

Junction Capacitance (diffusion capacitance)

→ between source/drain and body

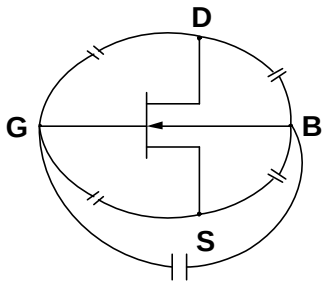
→ by applying bias to drain depletion region becomes larger



$C_{diff} = C_{\text{bottom-plate junction}} + C_{\text{sidewall junction}}$

$= C_j \cdot \text{area} + C_{jsw} \cdot \text{perimeter}$

$= C_j L_s W + C_{jsw}(2L_s + W)$



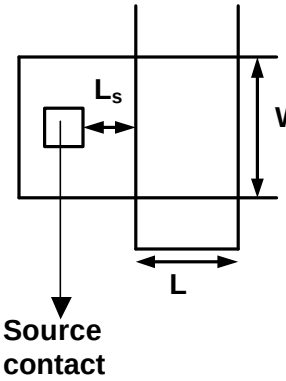
various capacitances

C_{ox}, C_o : determine gate cap

C_j, m_j, ϕ_b : related to bottom cap

C_{jsw}, m_{jsw}, ϕ_{bsw} : related to SW

Source/ Drain Resistance



$$R_{S/D} = R_c + \frac{L_s}{W} R_{\square}$$

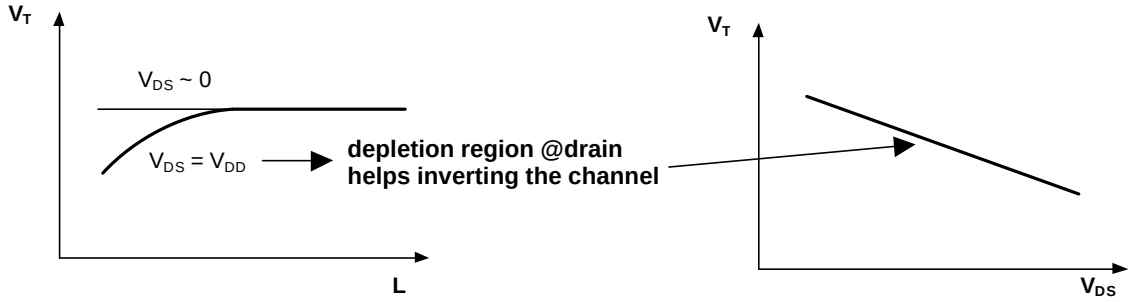
R_c : contact resistance

$R_{\square}$: sheet resistance

$$R = \rho \frac{L_s}{A} = \frac{r}{t_1} \frac{L_s}{W} = R_{\square} \frac{L_s}{W}$$

Secondary effect in MOS transistors

Threshold variation



short channel effect

drain-induced barrier lowering

V_T varies with operating voltage

narrow channel effect → $V_T \uparrow$

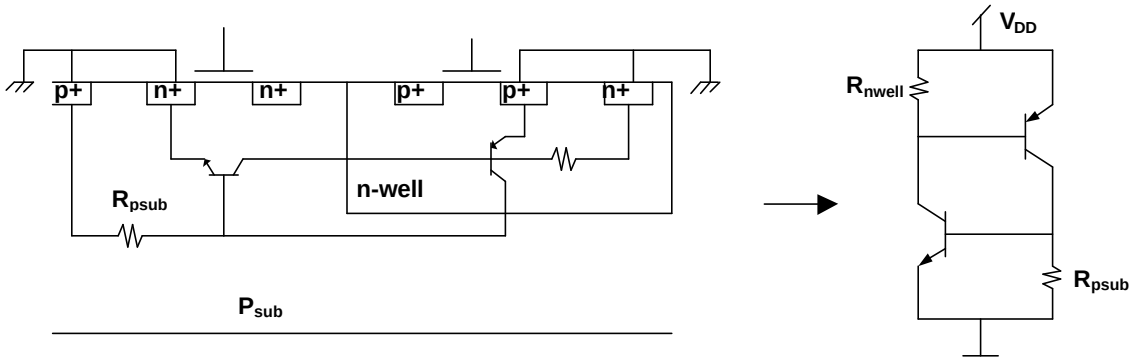
short channel effect → $V_T \downarrow$

$\Rightarrow$ Cancel each other

Hot carrier

Charging up the gate oxide → V_T variation with time

CMOS latch-up



To avoid latch-up

make R_{psub}, R_{nwell} small as possible

use lots of well/sub contact

guard-ring → circulates well/sub contact around transistor

Spice models

level I, level II, level III → not suitable for submicron

BSIM3VS → standard model now for sub-micron

Geometry-related parameters

W, L, : gate

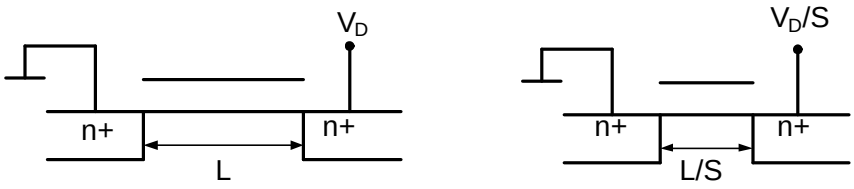
A_S, A_D, : source/drain area

P_S, P_D, : source/drain perimeters

NRS, NRD : # of squares of source/drain diffusion

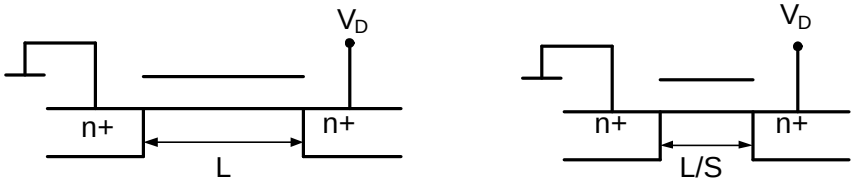
Technology scaling

Full scaling (constant E-field)



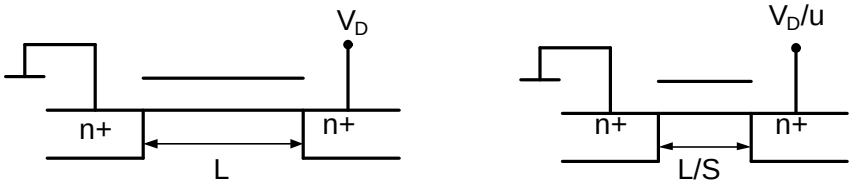
problem : small threshold → high leakage current

Fixed voltage scaling



problem : high e-field → hot carrier effect + breakdown

General scaling



problem : voltage scaling is usually as not aggressive