Advanced Interconnect technique

Reduced –Swing Circuit

$t_p = \frac{C_L V_{swing}}{I_{av}}$ → so to reduce t_p instead of increasing I_{av} we can reduce V_{swing}

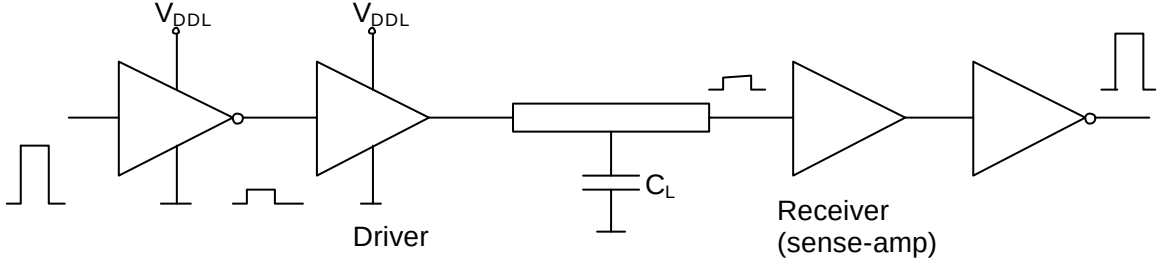
disadvantage → smaller noise margin

→ need amplifier at the receiver end

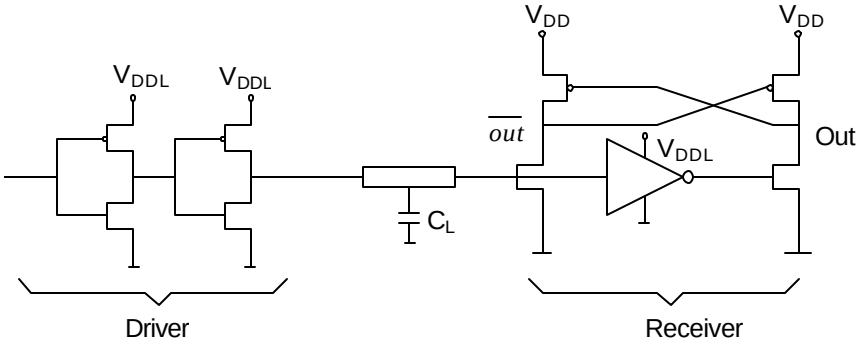
reduced swing circuit are need for

*address bus of µ-processors

*data lines in memory array → receiver is called sense amplifier



Static reduced swing network



→ acts as differential amplifier just two inverter as receiver is too slow since

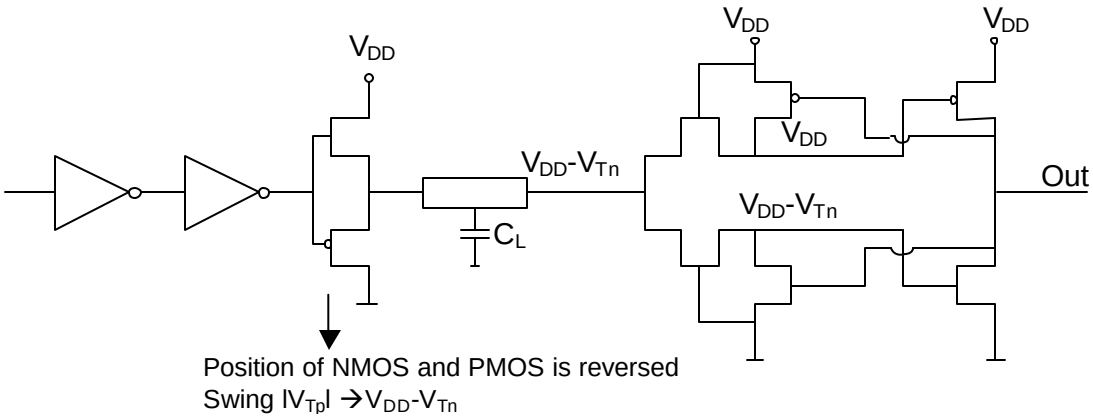
*0 → V_{DDL} signal cannot turn on NMOS completely so HL transition slow

*PMOS does not turn-off therefore increased static power consumption and even slower HL transition

Disadvantage : need two power supplies

Advantage : cross-coupled PMOS - → output is restored to VDD

→ positive feedback accelerate the transition

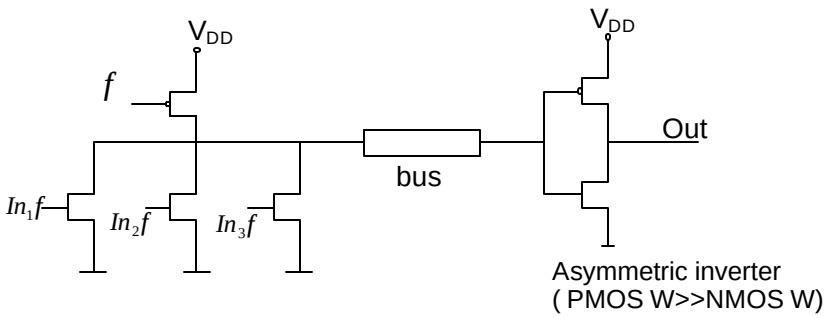


Avoids second supply → Vswing = V_{DD}-2V_T

Sensing delay is small as two inverter delay

Dynamic reduced –swing network

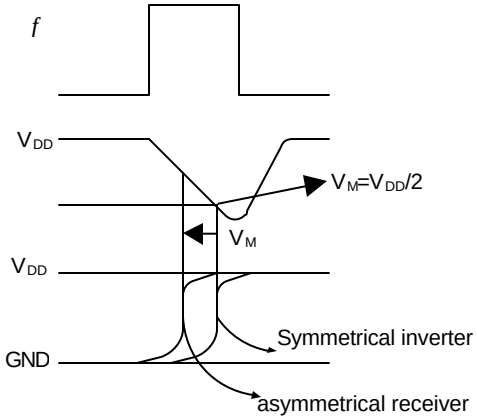
Suitable for large fan-in circuit such as buses



$f = 0$ → Bus wire is precharge to VDD

→ PMOS large → fast precharge to VDD

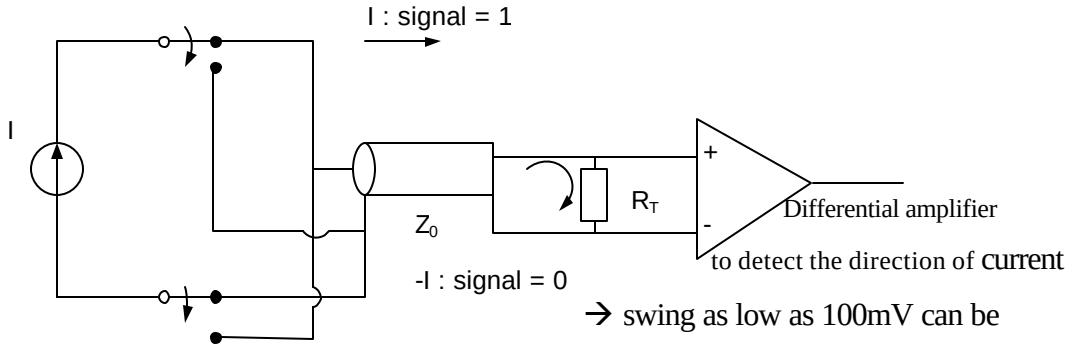
→ NMOS's are small so it takes time to discharge the line



Current-mode transmission technique

→ Instead of sending voltage signal for 1 and 0 send +I, -I for 1 and 0, respectively

→ output swing can be very low and is dependent on the termination resistance

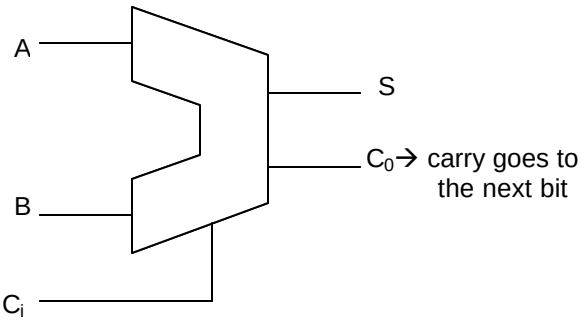


→ swing as low as 100mV can be easily detected.

Arithmetic Circuit

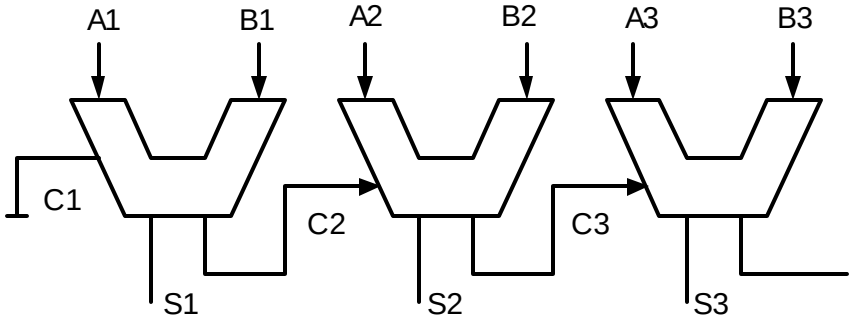
Adder

Full adder



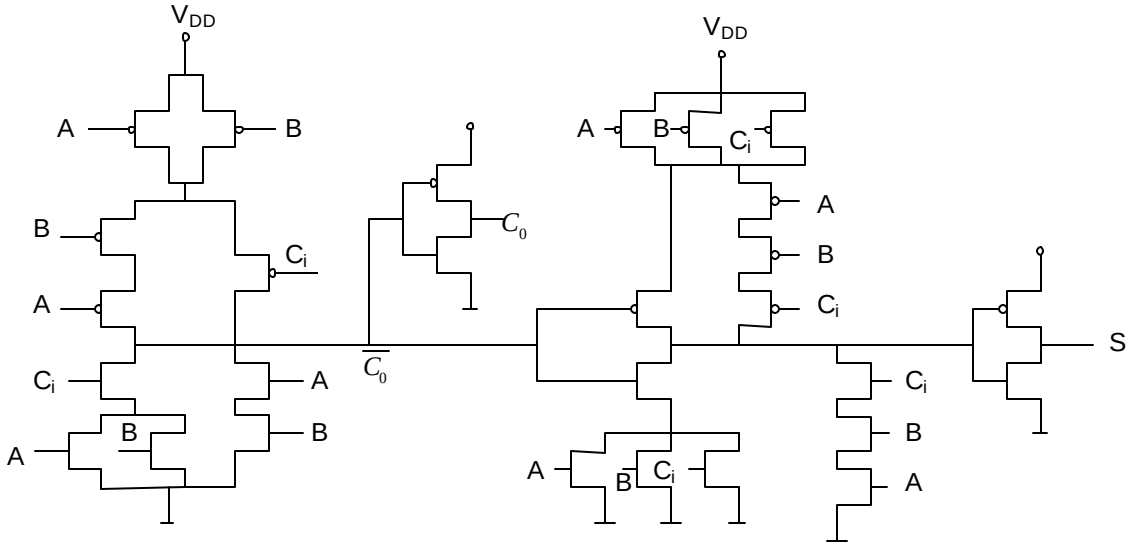
$$S = A \oplus B \oplus C_i = A\overline{B}\,\overline{C_i} + \overline{A}B\,\overline{C_i} + \overline{A}\,\overline{B}C_i + ABC_i$$

$$C_0 = AB + BC_i + AC_i$$



→ **Ripple carry adder**

$$t_{adder} = (N-1)t_{carry} + t_{sum}$$



→ Compared to A and B Ci is always critical path so always does as possible to output to reduce prop. delay

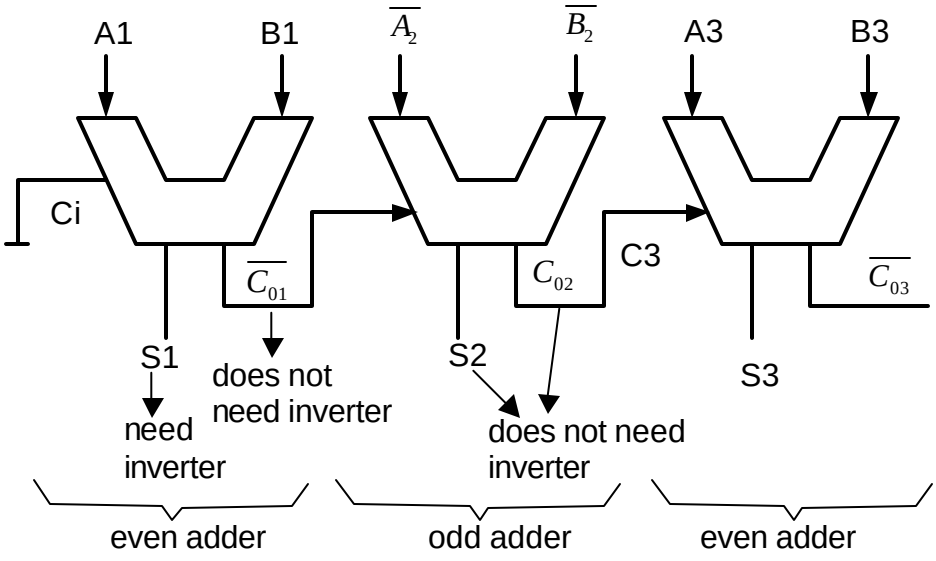
$$C_0 = AB + BC_i + AC_i$$

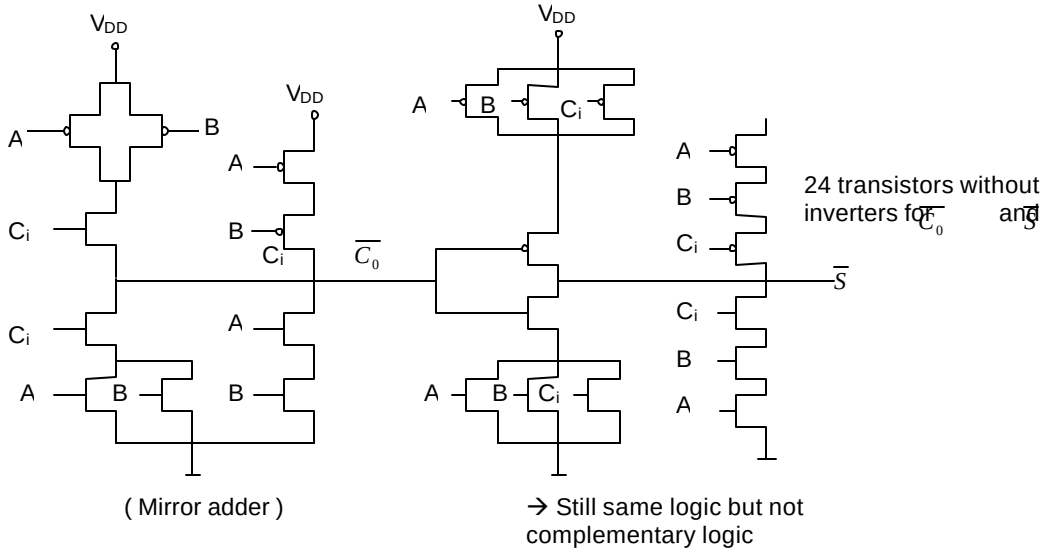
$$S = ABC_i + \overline{C_0}(A + B + C_i)$$

- large area
- PMOS stack → very slow
- Carry generation needs two gates ← minimizing the carry generation path is important
- Sum generation also needs an extra inverter gate but that is not important since it appears only once in the delay equation of ripple carry adder

Tricks to improve the performance

Remove the extra inverter an carry chain → generate add and even adders

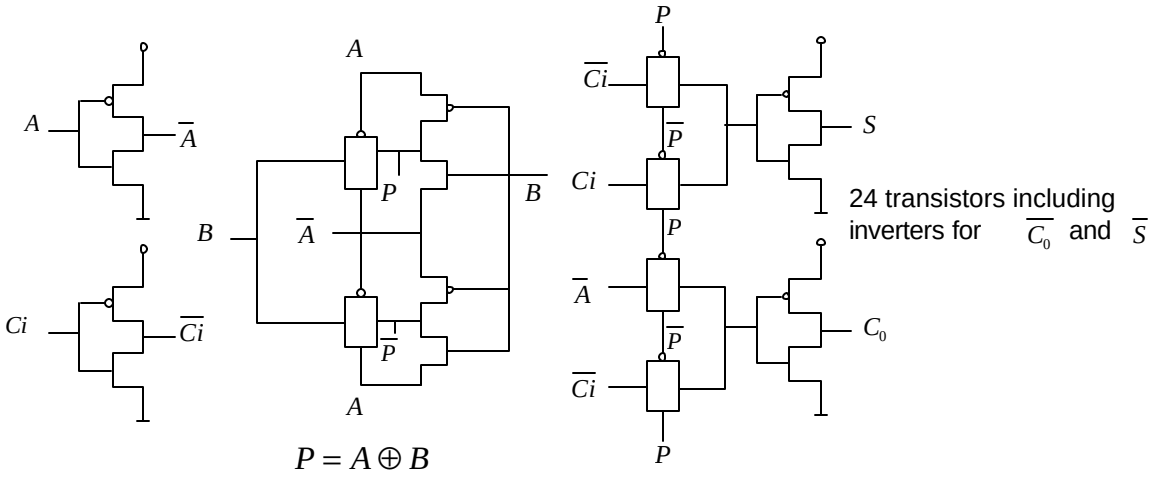




Transmission-Gate adder

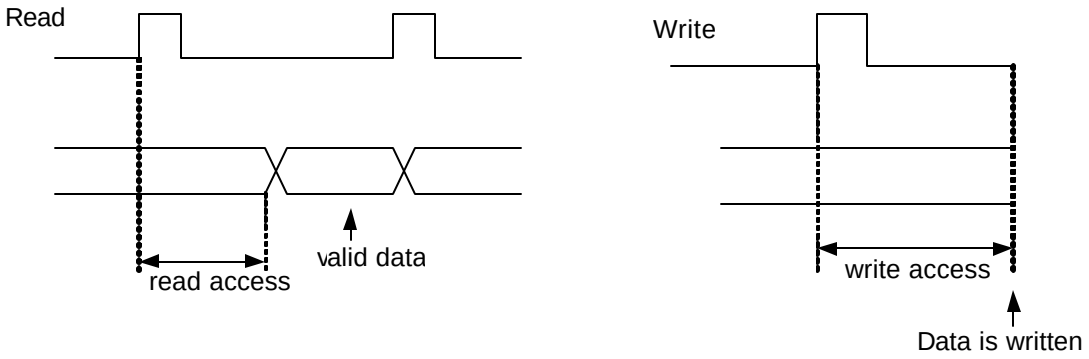
Full adder using MUX and XOR

→ can be easily realized in transmission-gate logic



Memory

Delay definitions

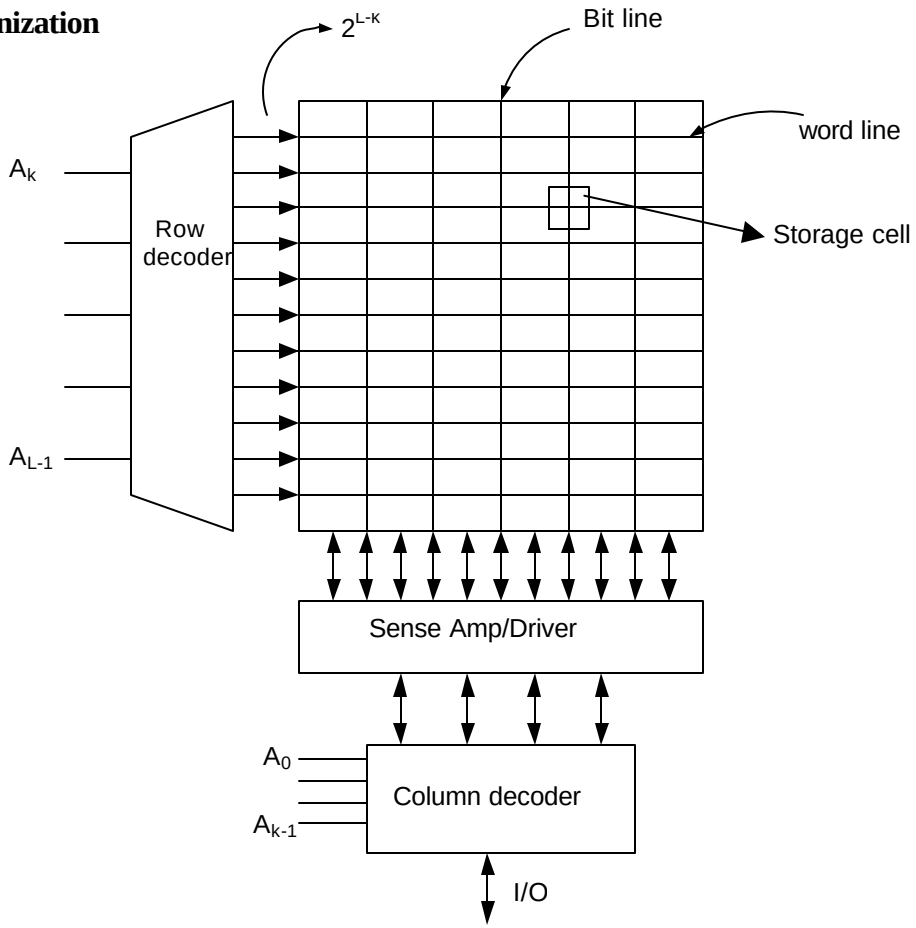


Memory classification

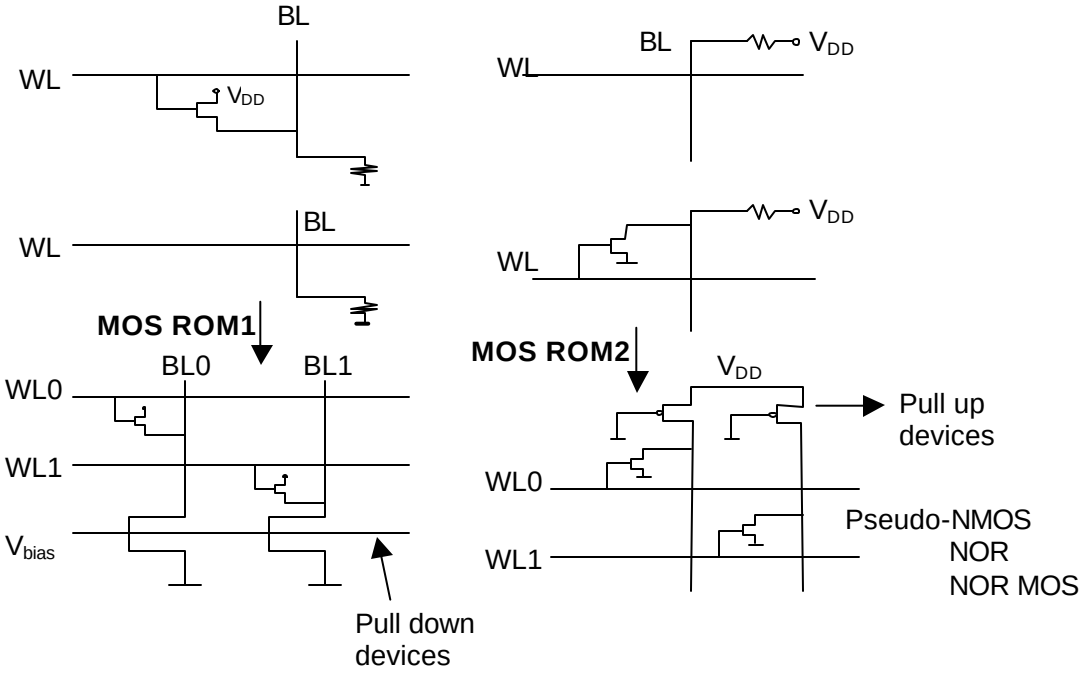
RWM		NVRWM	ROM
Random access	Non-random access	EPROM	Masked programmable PROM
SRAM	FIF0	E^2PROM	
DRAM	LIF0	Flash	
	Shift Reg.		
	CAM		

Contents-addressable memory

Array organization

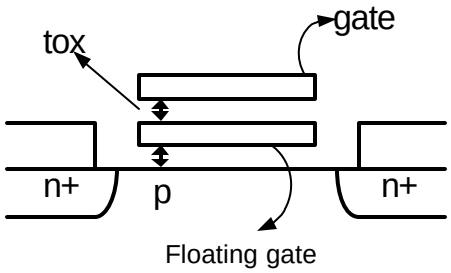


Memory Core



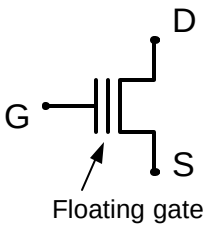
Non-Volatile Read-Write Memory

Floating gate transistor

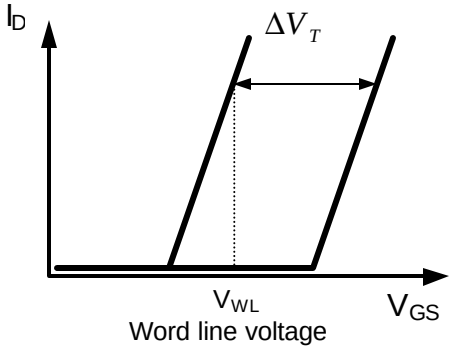


Use avalanche injection to charge-up the floating gate

(trapping of the electron on floating gate)



Threshold voltage is programmable



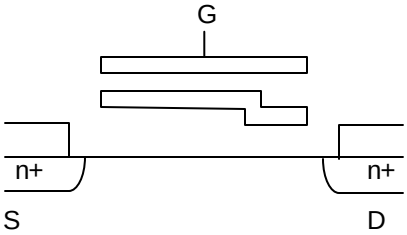
EPROM - Erasable-Programmable

Has a UV window → UV makes the oxide slightly conductive

→ charges on floating gate can be removed

→ slow process so erasing under UV can take few min.

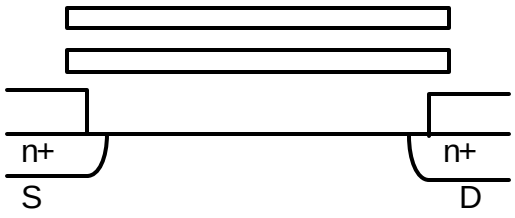
E^2PROM - Electrical erasable



By applying V_{GD} charge can be removed/ accumulated on the floating gate (~+_ 10V) depending on the polarity of the voltage

Flash E^2PROM

Combines the advantages of EPROM and EEPROM



+20 for programmable

-10 and overlap for erasing