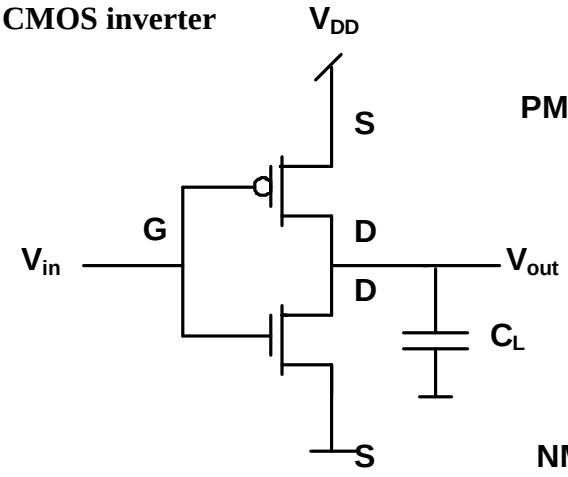
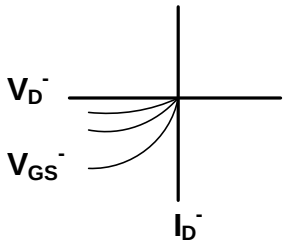
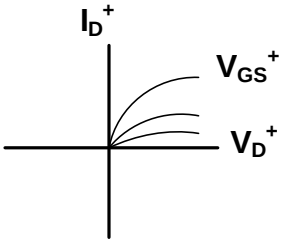
CMOS inverter







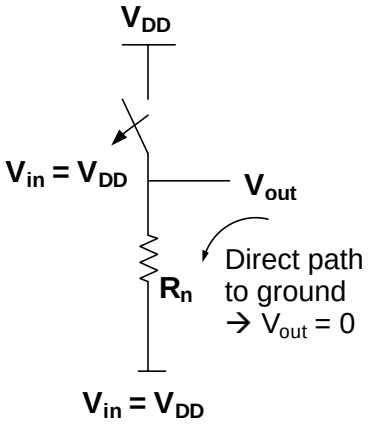
$V_{GSn} = V_{in}$ $I_{Dn} = I_D$

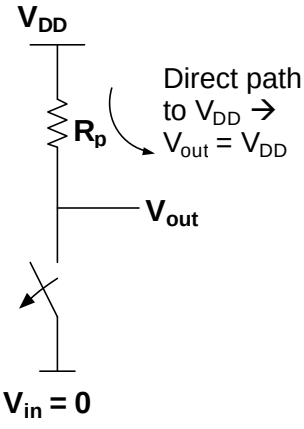
$V_{GSp} = V_{in} - V_{DD}$ $I_{Dp} = I_D$

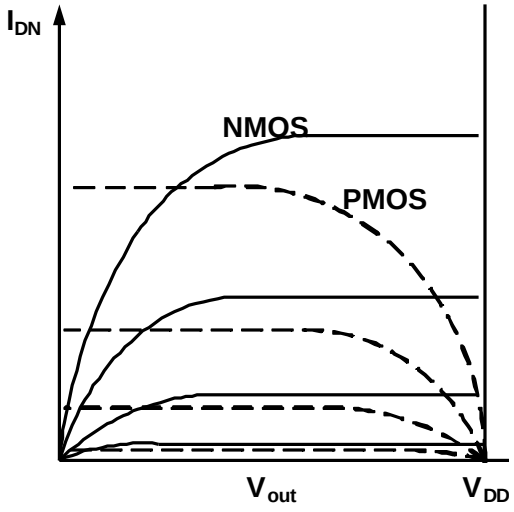
$V_{DSn} = V_{out}$

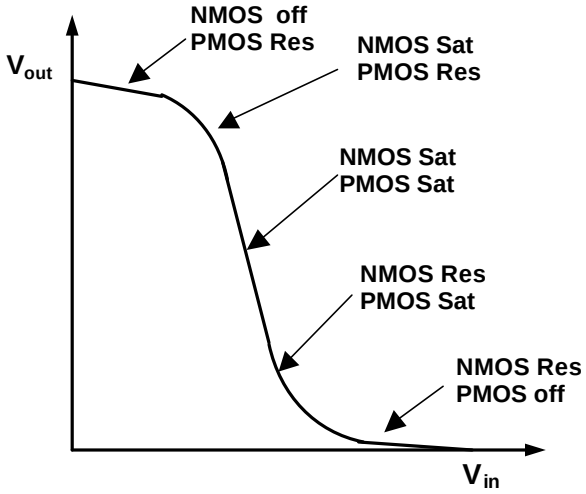
$V_{DSp} = V_{out} - V_{DD}$

$I_{DSp} = -I_{DSn}$









CMOS inverter / Static Behavior

Switching threshold V_M →

Both PMOS and NMOS are in velocity saturation

$I_{DN}+I_{DP} = 0$ → ignoring channel length modulation

$$(I)\quad K_n V_{Dsatn}\left(V_M - V_{Tn} - \frac{V_{Dsatn}}{2}\right) + K_p V_{Dsatp}\left(V_M - V_D - V_{Tp} - \frac{V_{Dsatp}}{2}\right) = 0$$

solving for V_M

$$V_M = \frac{\left(V_{Tn} + \frac{V_{Dsatn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{Dsatp}}{2}\right)}{1+r}, \quad r = \frac{K_p V_{Dsatp}}{K_n V_{Dsatn}} = \frac{u_{satp} W_P}{u_{satn} W_N}$$

For large V_{DD} → $V_M = \frac{rV_{DD}}{1+r}$, r=1 → $V_M=V_{DD}/2$ equal noise margins

For long channel devices → NMOS and PMOS transistors in saturation

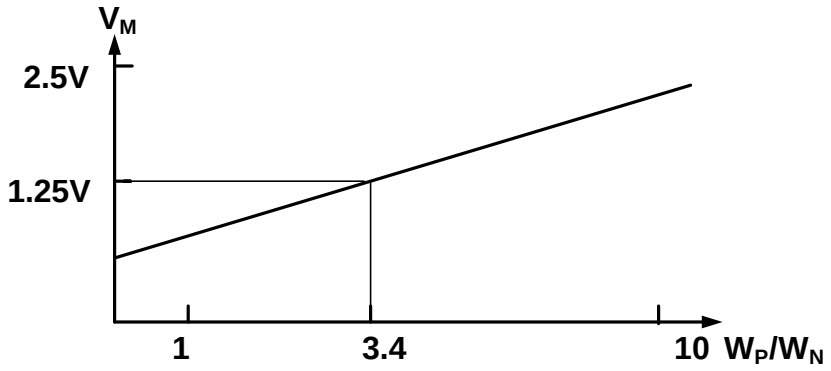
→ $V_M - V_T < V_{Dsat}$

(I) → $K_n(V_M - V_{Tn})^2 + K_p(V_M - V_{TP} + V_{DD})^2 = 0$

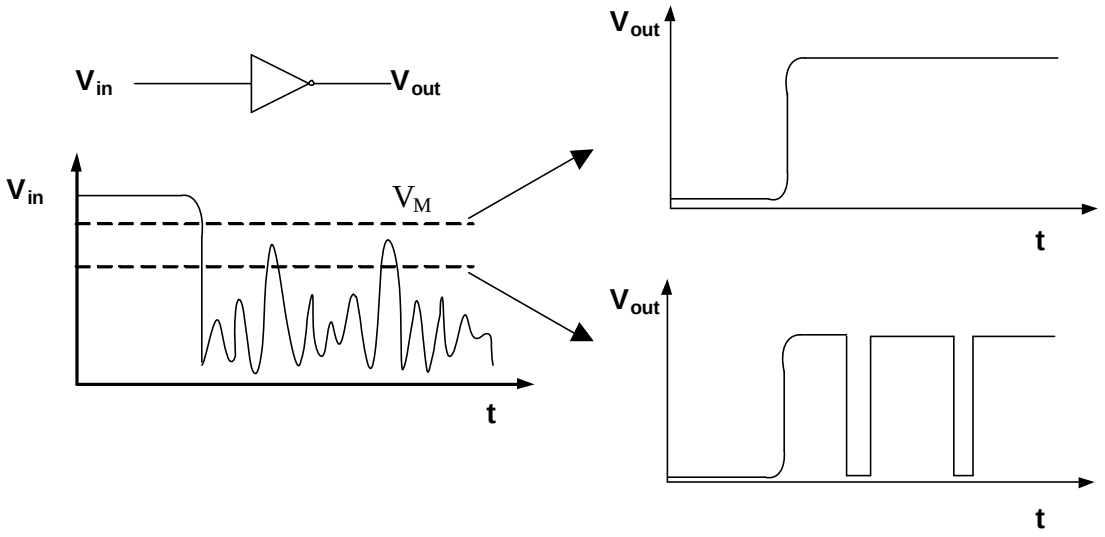
$$V_M = \frac{V_{Tn} + r(V_{DD} + V_{Tp})}{1+r}, \quad r = \sqrt{\frac{-K_p}{K_n}}$$

For 0.25u CMOS

$$(I) \rightarrow \frac{W_P / L_P}{W_N / L_N} = \frac{K'_N}{K'_P} \cdot \frac{V_{Dsat}n}{V_{Dsatp}} \cdot \frac{V_M - V_{Tn} - V_{Dsatn}/2}{V_{DD} - V_M + V_{Tp} + V_{Dsatp}/2} = 3.5$$



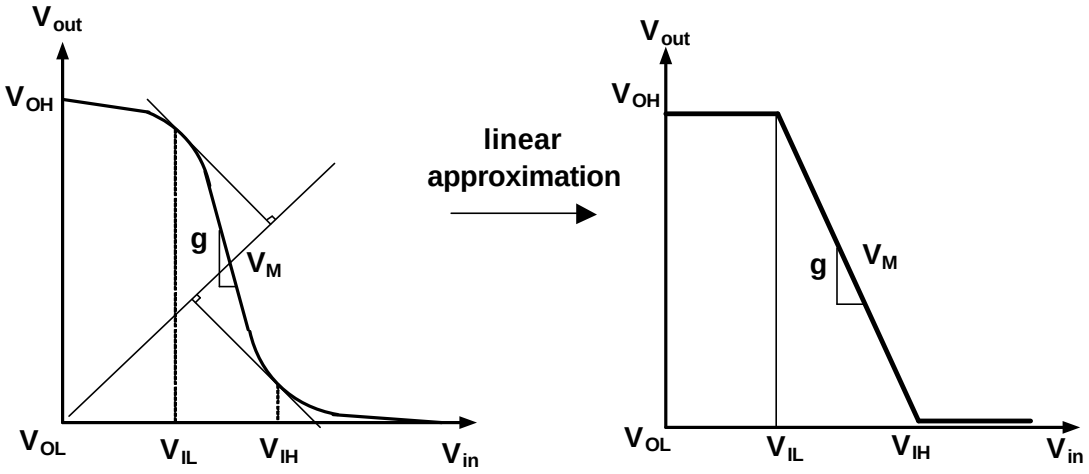
Sometimes you don't want symmetry noise on the Gnd plane



So you adjust (W/L)P/(W/L)N ratio to get nonsymmetric V_M. But as can be seen from figure V_M does not change a lot with the ratio.

Noise Margin

Other than threshold voltage, we are interested in knowing the noise margins.



$$V_{IH}-V_{IL}=\frac{-V_{DD}}{g},\quad V_{IH}=V_M-\frac{V_M}{g},\quad V_{IL}=V_M+\frac{V_{DD}-V_M}{g}$$

$$\rightarrow\ NMH=V_{DD}-V_{IH}=V_{DD}-V_M+\frac{V_M}{g},\quad NML=V_{IL}=V_M+\frac{V_{DD}-V_M}{g}$$

To find the gain, we need to take into account the channel length modulation otherwise gain $\rightarrow\infty$

$I_D = I_{Dp} + I_{Dn} = 0$

$$K_n V_{Dsatn}\left(V_{in} - V_{Tn} - \frac{V_{Dsatn}}{2}\right)(1 + l_n V_{out}) + K_p V_{Dsatp}\left(V_{in} - V_D - V_{Tp} - \frac{V_{Dsatp}}{2}\right)(1 + l_p (V_{out} - V_{DD})) = 0$$

$$\left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M} = g = \frac{1}{I_D(V_M)} \cdot \frac{K_n V_{Dsatn} + K_p V_{Dsatp}}{l_n - l_p} \approx \frac{1+r}{(VM - VTn - VDsatn/2)(l_n - l_p)}$$

→Gain is determined by technology parameters especially channel length modulation.

0.25u CMOS

W_P/W_N ratio = 3.4

$$\rightarrow\ r = \frac{K_p V_{Dsatp}}{K_n V_{Dsatn}} = \frac{3.4 \times 3 \times 10^{-5}}{11.5 \times 10^{-5}} \times \frac{1}{0.63} = 1.4,$$

$$g = \frac{1+1.4}{(1.25 - 0.43 - \frac{0.63}{2})(0.06+1)} = -27.2$$

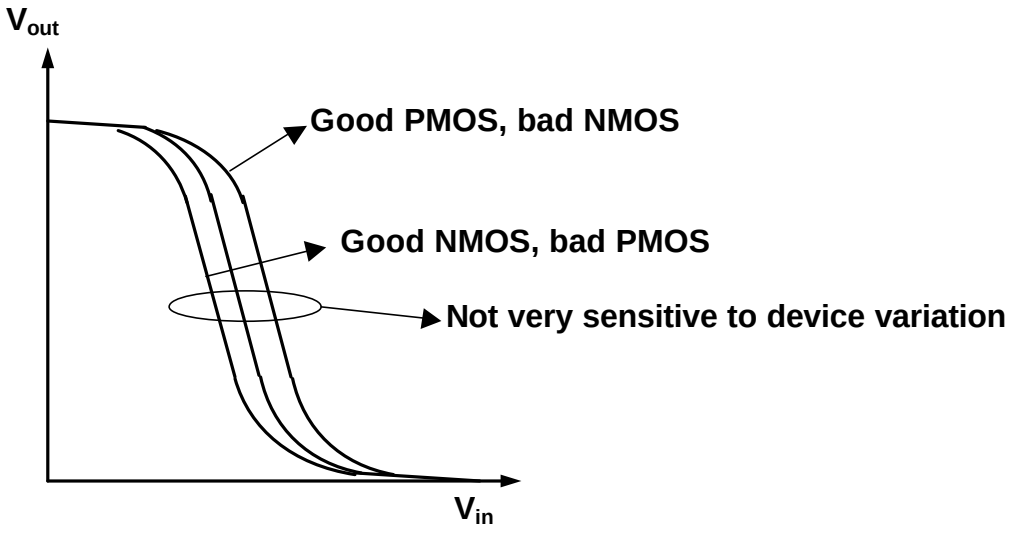
$$V_{IH} - V_{IL} = \frac{-2.5}{-27.2} = 0.09,\ V_{IH} = V_M\left(1 - \frac{1}{g}\right) = 1.25(1 + 0.036) = 1.287$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} = 1.2,\ NMH = V_{DD} - V_{IH} = 1.212,\ NML = V_{IL} = 1.2$$

Simulation → NMH = 1.05, NML = 1.03

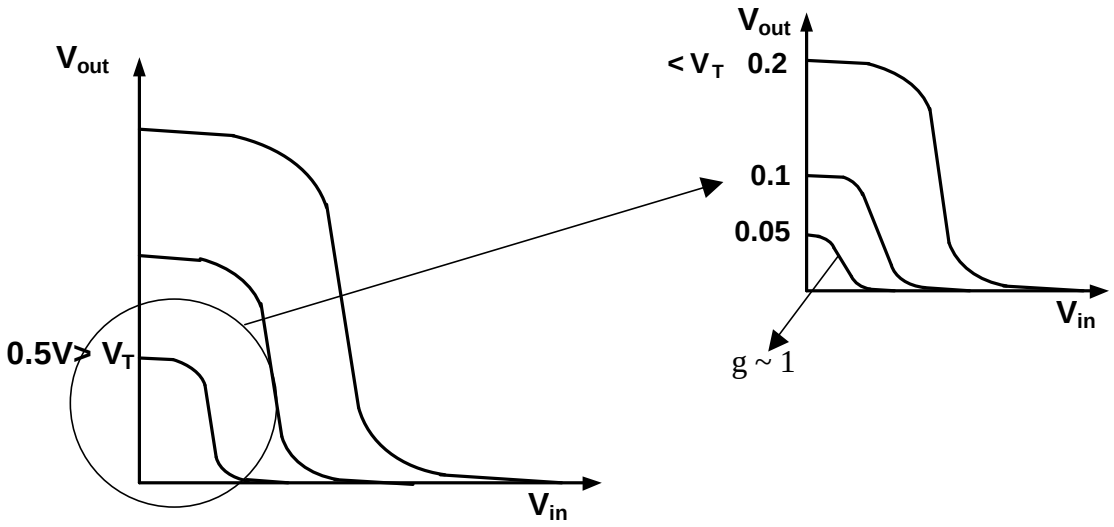
much lower because * the equation for gain overestimate the gain

*linear approximation



Scaling with Supply voltage

Devices work even in subthreshold → Inverter function



$V_{DD}\downarrow$ → Power ↓ but gate delay ↑

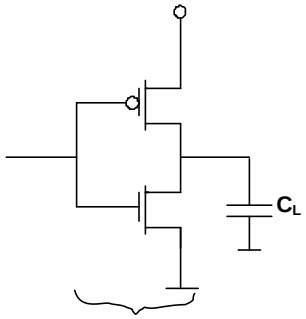
→ DC characteristic becomes sensitive to device parameter

→ More sensitive to external noise

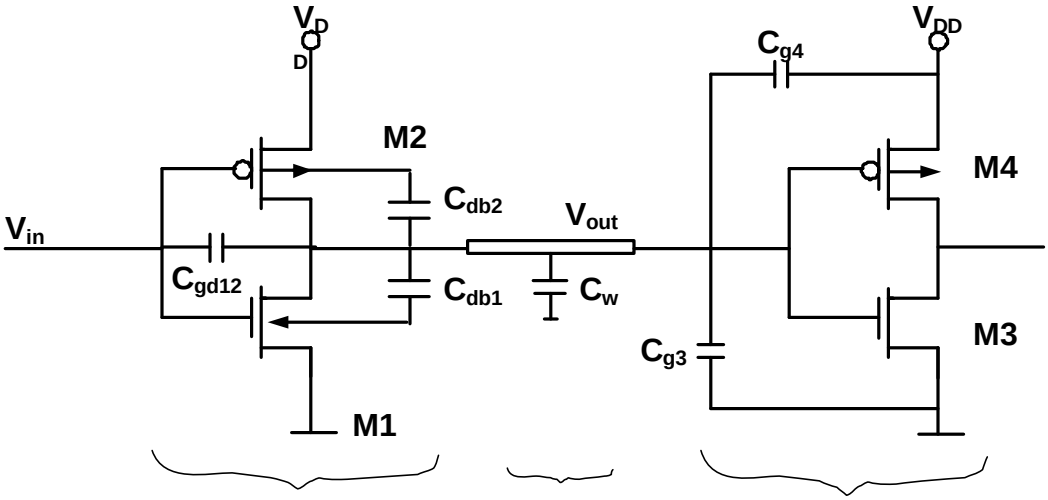
V_{DDmin} ~ 2 – 4 kT/q ~ 0.05 – 0.1 Volts

CMOS Inverter – Dynamic Behavior

C_L → make it as small as possible

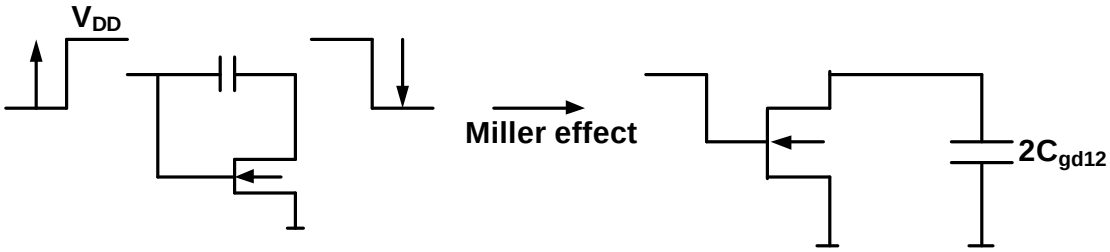


Has some parasitic capacitance → self-loading effect



Self-loading wire loading next gate loading

Gate-drain capacitance



C_{gd} → gate drain overlap capacitance

$$2\{C_{GD0}(NMOS)\cdot W_{NMOS} + C_{GDO}(PMOS)\cdot W_{PMOS}\}$$

Drain-Body capacitance (Diffusion capacitance)

$$C_{eq} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-f_{om}}{(V_{high} - V_{low})(1-m)} \left\{ (f_0 - V_{high})^{1-m} - (f_0 - V_{low})^{1-m} \right\}$$

K_{eq} for 0.25 μ CMOS

H → L	(NMOS)	$K_{eq} = 0.57$	H → L	(PMOS)	$K_{eq} = 0.79$
		$K_{eqsw} = 0.61$			$K_{eqsw} = 0.86$
L → H	(NMOS)	$K_{eq} = 0.79$	H → L	(PMOS)	$K_{eq} = 0.59$
		$K_{eqsw} = 0.81$			$K_{eqsw} = 0.79$

Wire Capacitance

can be calculated from the size of interconnects. Tables 4.2 , 4.3

Gate Capacitance

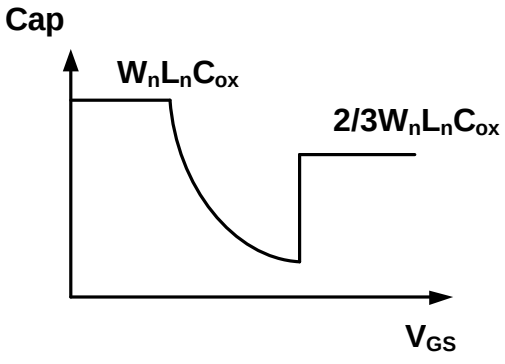
from fan-out transistors, $C_{fan\text{-}out} = C_{g3}, C_{g4}$

$C_{fan\text{-}out} = C_{gate}(NMOS) + C_{gate}(PMOS)$

$$= (\underbrace{C_{GS0n} + C_{GD0n}}_{overlap} + \underbrace{W_n L_n C_{ox}}_{channel}) + (\underbrace{C_{GS0p} + C_{GD0p}}_{overlap} + \underbrace{W_p L_p C_{ox}}_{channel})$$

no miller effect since fan-out gate has not become active (due to delay)

constant channel capacitance



→ Pessimistic approximation

0.25μ CMOS Cap

Minimum size of gate : $W_{PMOS} = 3W_{NMOS}$

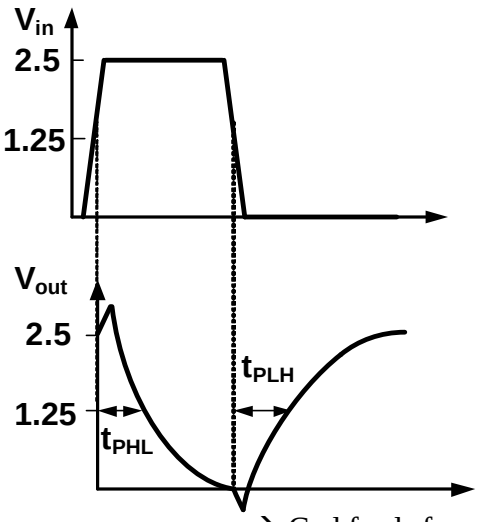
Capacitor	Expression	H→L (fF)	L→H (fF)	
C_{gd1}	$2CGD0_n\ W_n$	0.23	0.23	
C_{gd2}	$2CGD0_p\ W_p$	0.61	0.61	$C_{self\text{-}load}$
C_{db1}	$K_{eqn}AD_nCJ+K_{eqswn}PD_nCJSW$	0.66	0.90	C_{int} = 2.8fF
C_{db2}	$K_{eqp}AD_pCJ+K_{eqswp}PD_pCJSW$	1.50	1.15	
C_{g3}	$(CGD0_n+CGS0_n)W_n + C_{ox}W_nL_n$	0.76	0.76	
C_{g4}	$(CGD0_p+CGS0_p)W_p + C_{ox}W_pL_p$	2.28	2.28	C_{ext} = 3.15fF
C_w	extraction	0.12	0.12	
C_L	Σ	6.1	6.0	

Propagation Delay

$t_p \rightarrow\ t_{PHL} = 0.69\ R_{eqn}C_{LH\rightarrow L}$, $t_{PLH} = 0.69\ R_{eqn}C_{LL\rightarrow H}$

(I) $R_{eq} \cong \frac{3}{4}\frac{V_{DD}}{I_{Dsat}}(1-\frac{7}{9}lV_{DD}) \rightarrow I_{Dsat} = K'\frac{W}{L}\left((V_{DD}-V_T)V_{Dsat}-\frac{V_{Dsat}^{\ 2}}{2}\right)$

0.25μ CMOS t_{PHL} = 36ps, t_{PLH} = 29ps $\rightarrow t_p = \frac{t_{PHL}+t_{PLH}}{2} = 32.5\,p\,\text{sec}$



→ Cgd feeds forwards the input signal to the output

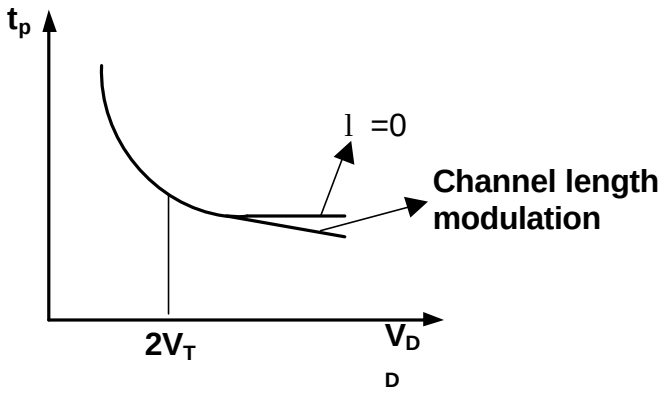
Effect of V_{DD} on t_p

$\lambda = 0$ → No channel length modulation

$$t_p = 0.69 R_{eq} \cdot C_L = 0.69 \times \frac{3}{4} \frac{V_{DD} C_L}{K' \frac{W}{L} V_{Dsat} \left((V_{DD} - V_T) - \frac{V_{Dsat}}{2} \right)}$$

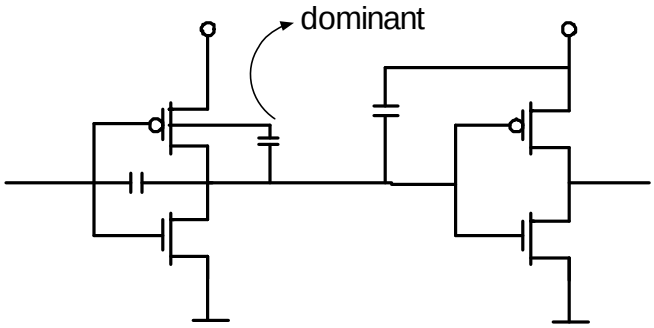
$V_{DD} \uparrow \rightarrow t_p = \dfrac{0.52 C_L}{\dfrac{W}{L} K' V_{Dsat}}$ independent of V_{DD}

$V_{DD} \downarrow \rightarrow t_p \uparrow$



Design Technique to Reduce Delay Time

* $C_L \downarrow$ make drain pad of PMOS small → C_{db2} dominant



* W/L ↑ $t_p \propto Re \propto 1/(W/L)$ → trade off with C_L

* $V_{DD} \uparrow$ due to channel length modulation

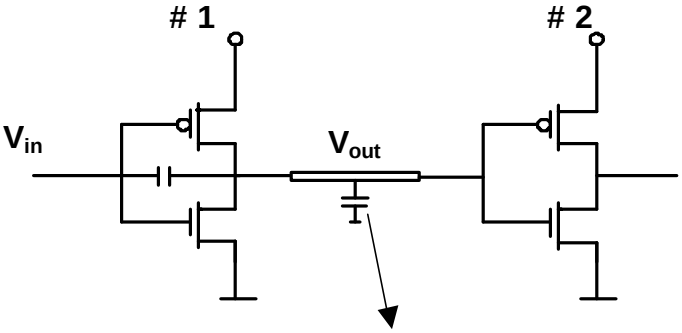
Propagation Delay

PMOS to NMOS device size ratio 3 ~ 3.5 symmetric operation

→ not necessarily fast response

Case (I)

How to find optimum W_p/W_n ratio for fastest response



$$C_L = \underbrace{(C_{dp1} + C_{dn1})}_{self-load} + \underbrace{(C_{gp2} + C_{gn2})}_{fan-out} + C_w$$

PMOS β times larger than NMOS $b = \dfrac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n}$

$$C_L \approx (bC_{dn1} + C_{dn1}) + (bC_{gn2} + C_{gn2}) + C_w = (b+1)(C_{dn1} + C_{gn2}) + C_w$$

$$t_p = \frac{1}{2}(t_{PHL} + t_{PLH}) = \frac{0.69}{2}\left((b+1)(C_{dn1} + C_{gn2}) + C_w\right)\left(R_{eqn} + \frac{R_{eqp}}{b}\right)$$

$$t_p = 0.345R_{eqn}\left((b+1)(C_{dn1} + C_{gn2}) + C_w\right)\left(1 + \frac{r}{b}\right), \quad r = \frac{R_{eqp}}{R_{eqn}}$$

$$t_p = 0.345R_{eqn}\left(C_{dn1} + C_{gn2} + b(C_{dn1} + C_{gn2}) + C_w + \frac{r}{b}(C_{dn1} + C_{gn2}) + \frac{r}{b}C_w + r(C_{dn1} + C_{gn2})\right)$$

$$\frac{\partial t_p}{\partial b} = 0 = C_{dn1} + C_{gn2} - \frac{r}{b^2}(C_{dn1} + C_{gn2} + C_w)$$

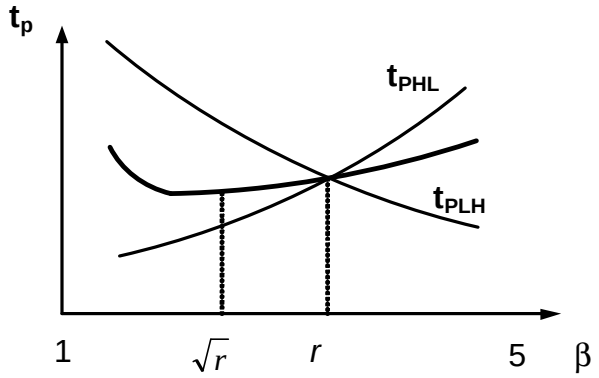
$$b_{opt} = \sqrt{\frac{r(C_{dn1} + C_{gn2} + C_w)}{C_{dn1} + C_{gn2}}}$$

$C_w \downarrow$ → $\beta_{opt} = \sqrt{r}$ not r to get the max speed!

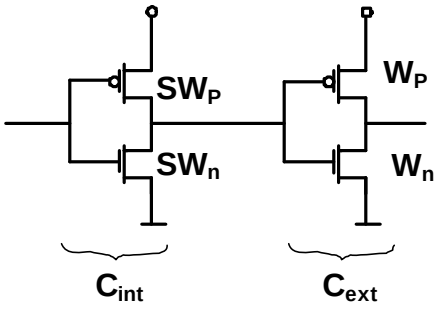
0.25 μ CMOS

$$r = \left.\frac{R_{eqp}}{R_{eqn}}\right|_{\min size\cdot transistor} = \frac{31k\Omega}{13k\Omega} = 2.4 \rightarrow \text{symmetry } t_{PHL},\ t_{PLH},$$

$\beta_{opt} = \sqrt{r}$ =1.6 → optimum point ~ 1.9



Case (II) : assume fixed W_p/W_n ratio



$$\frac{SW_p}{SW_n} = \frac{W_p}{W_n} = same \cdot ratio$$

Scaling effect on delay time

$$t_p = 0.69R_{eq}(C_{\text{int}} + C_{ext}) = 0.69R_{eq}C_{\text{int}}\left(1+\frac{C_{ext}}{C_{\text{int}}}\right) = t_{p0}\left(1+\frac{C_{ext}}{C_{\text{int}}}\right)$$

t_{p0} : intrinsic or unloaded delay C_{int} : miller + diffusion caps only

sizing effect : S

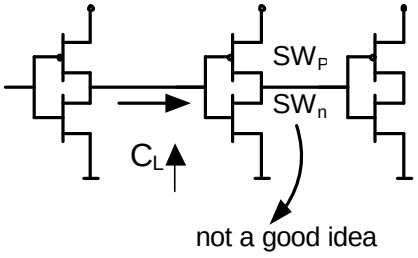
$$tp = 0.69\left(\frac{R_{ref}}{S}\right)\left(SC_{\text{int},ref}\right)\left(1+\frac{C_{ext}}{SC_{\text{int},ref}}\right)$$

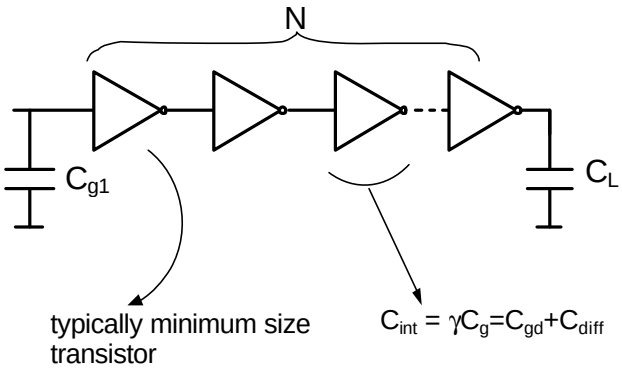
$$= 0.69R_{ref}C_{\text{int},ref}\left(1+\frac{C_{ext}}{SC_{\text{int},ref}}\right) = t_{p0}\left(1+\frac{C_{ext}}{SC_{\text{int},ref}}\right)$$

→minimum delay or intrinsic delay or unloaded delay does not change with sizing.
→ S↑ → t_p → t_{p0}

If driver transistors are scaled up, the effect of load (fan-out+C_w) transistor will be masked.

Case II : Chain of Inverters

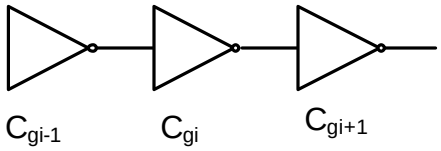




f = fan-out = C_{ext}/C_g C_{ext} : external load capacitance of gate

C_g : input capacitance of gate

$$t_p = t_{p0}\left(1+\frac{C_{ext}}{C_{int}}\right) = t_{p0}\left(1+\frac{f}{g}\right)$$



optimum performance when $C_{gi} = \sqrt{C_{gi-1}\cdot C_{gi+1}}$

C_{gi} → geometric mean

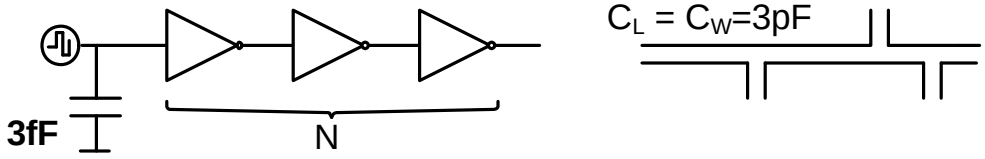
→ optimum performance is achieved when the scaling of each stage is geometric mean of the stage before and after.

$$f = \sqrt[N]{\frac{C_L}{C_{g1}}} = \sqrt[N]{F}$$ → optimum fan-out f~4, can find N

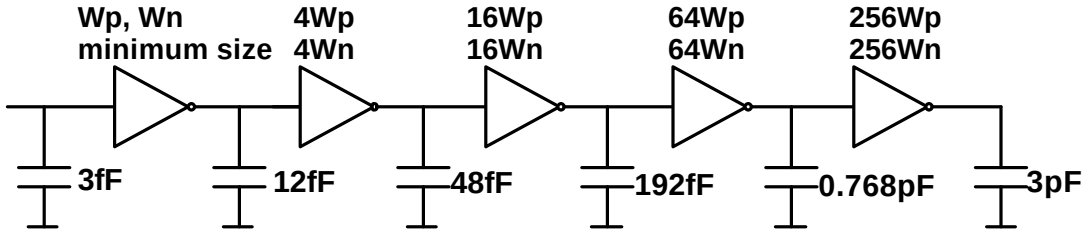
f : fan-out of each stage, F : overall effective fan-out

$$t_{p\min} = Nt_{p0}\left(1+\frac{\sqrt[N]{\frac{C_L}{C_{g1}}}}{g}\right)$$

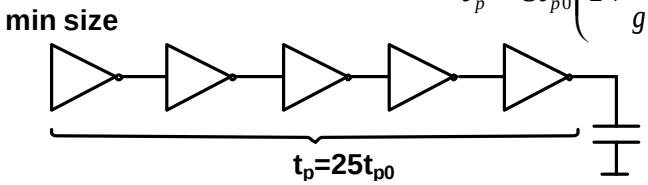
example : line driver for clock signal $C_W=C_L=3pF$, $C_{g1} \approx 3fF$



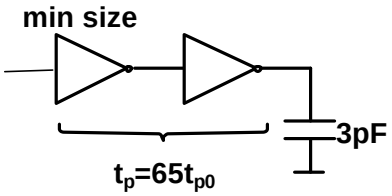
$$4^N = \frac{3pF}{3fF} = 1000 \rightarrow N\sim 5$$



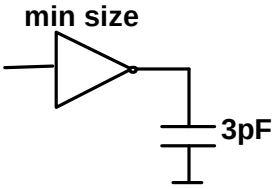
$$t_p = 5t_{p0}\left(1+\frac{4}{g}\right) = 25t_{p0}$$



$\rightarrow$ f=4



$$f = \sqrt[2]{1000} = 31.5 \rightarrow t_p = 2\times t_{p0}\left(1+\frac{31}{1}\right) \approx 65t_{p0}$$

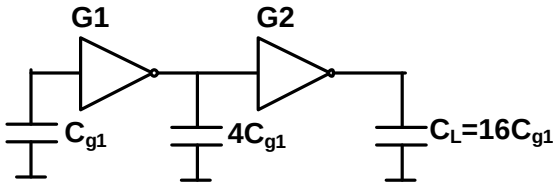


$t_p=1001t_{p0}$, N=1 $\rightarrow$ $t_p=1001t_{p0}$

Effect of Rise/Fall time on inverter delay

$$t_p = \underbrace{t_{step}}_{stage1} + h\ \underbrace{t_{step}}_{stage i-1}$$

η = 0.25 empirical constant



$$t_p = t_{p0}\left(1+\frac{4C_{g1}}{gC_{g1}}\right) + t_{p0}\left(1+\frac{16C_{g1}}{g\,4C_{g1}}\right) + ht_{p0}\left(1+\frac{4C_{g1}}{gC_{g1}}\right) = t_{p0}\left(1+\frac{4C_{g1}}{gC_{g1}}\right)(1+h) + t_{p0}\left(1+\frac{16C_{g1}}{g\,4C_{g1}}\right)$$

γ=1 $\rightarrow$ $t_p = t_{p0}\times 5(1+0.25) + t_{p0}\times 5 = 10t_{p0} + \underbrace{1.25t_{p0}}_{due\cdot to\cdot rise\cdot fall\cdot time} = 11.25t_{p0}$