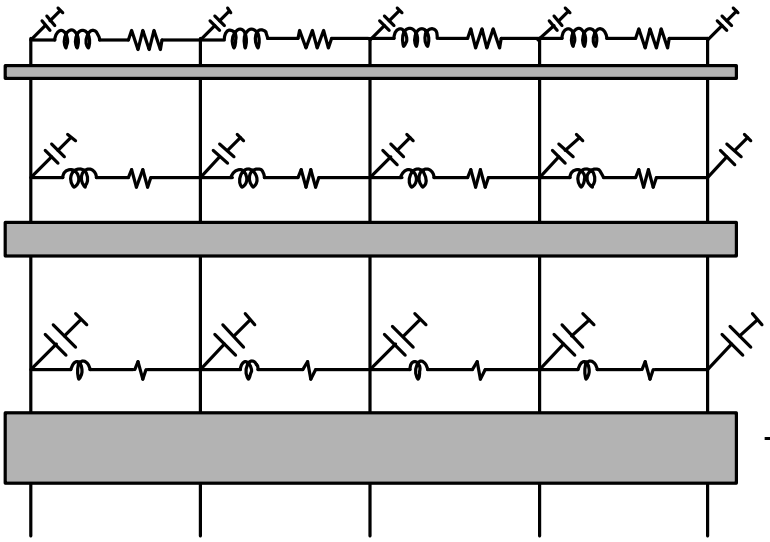
Interconnects

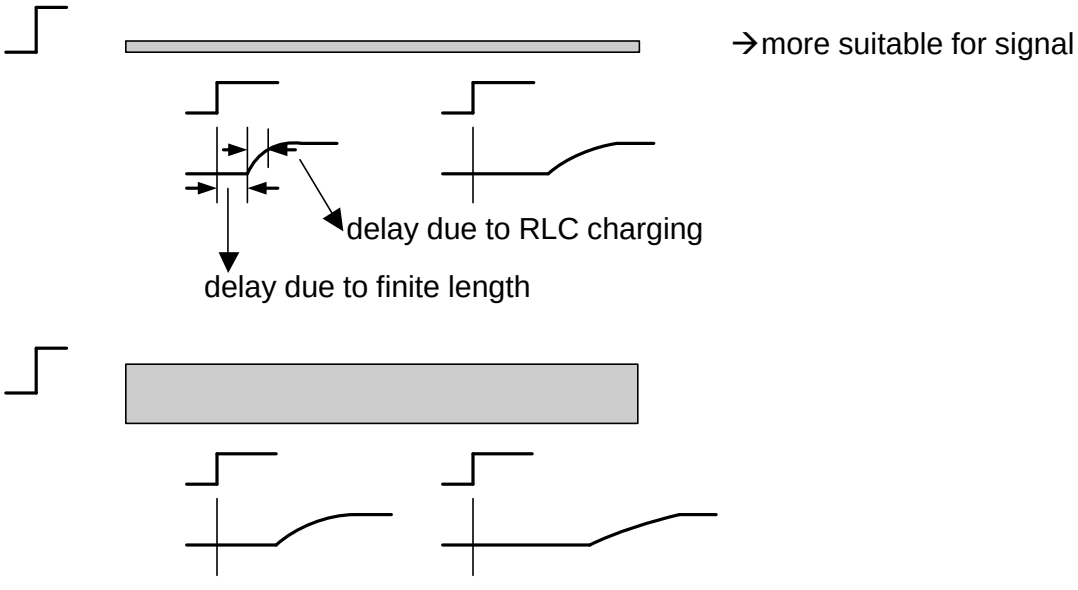
Assume 3 line : divide them into equal sections



→ high resistance
small capacitance
high inductance
→high impedance line
(inductive)

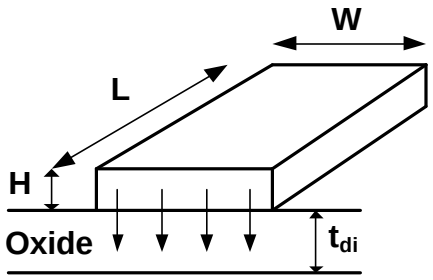
→ high capacitance
small resistance
small inductance
→low impedance line
(capacitive)

When you apply a signal (sharp step function)



→ Capacitance lines are suitable for power distribution → They kill the signal.

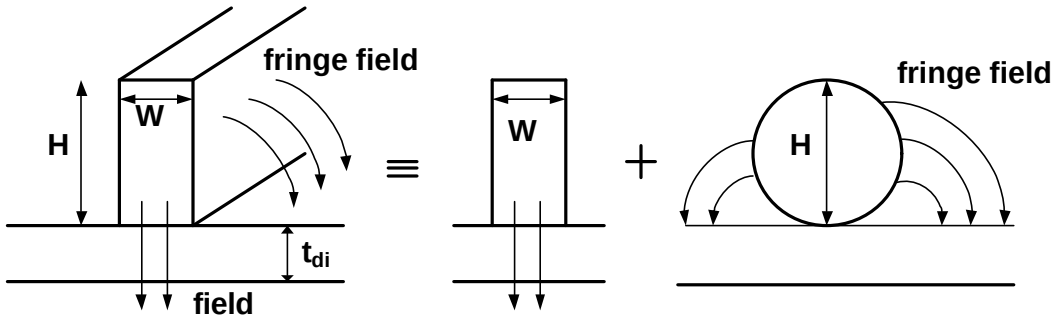
Line capacitance



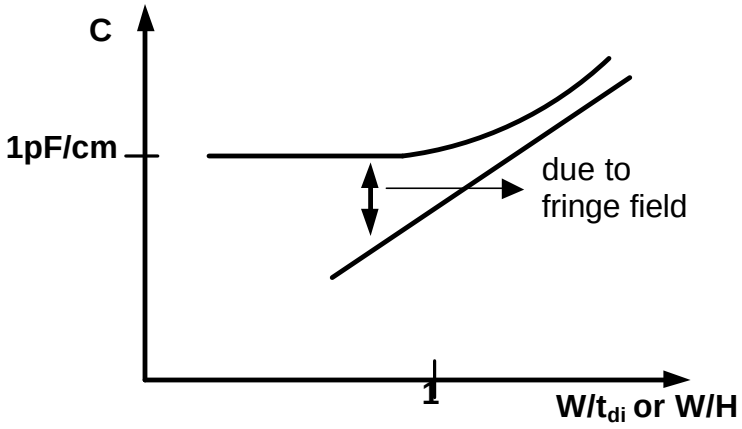
$$C = \varepsilon \frac{A}{d} = e_{di} \frac{WL}{t_{di}}$$ → first order approximation

As you go to deep submicron, make L ↓, but to reduce resistance you make H ↑

Submicron interconnect



$$C_{wire} = C_{pp} + C_{fringe} = \frac{W - H/2}{t_{di}} + \frac{27 e_{di}}{\log(t_{di}/H)}$$: be careful using this formula



Interwire capacitance

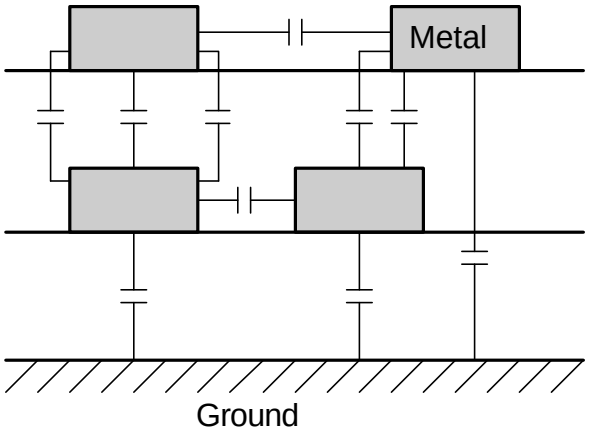


Table 4.2 (page 143) gives average capacitance between PP(parallel plate) and fringe.

Different interconnects in 0.25μ process

Poly – field oxide → high capacitance

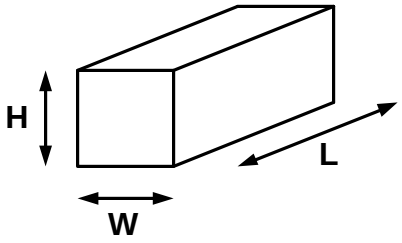
Metal – active > metal – field oxide

Table 4.3(page 144) gives interwire capacitance on same level.

Resistance

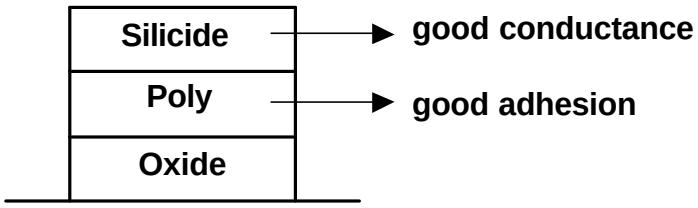
$R = \frac{rL}{HW}$? : resistivity (Ωcm) , H : constant

$R = R_{\square} \frac{L}{W}$ $R_{\square}$: sheet resistance((Ω/cm)



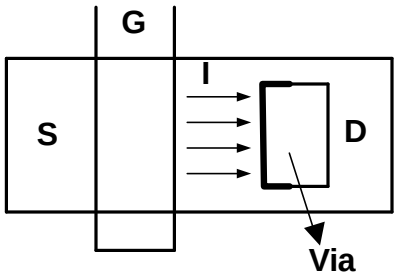
Silicide and polycide are used to reduce sheet resistance of diffusion/poly layers.

	n^+ , p^+	n^+ , p^+ + silicide	Poly	Polycide	Al
$R_{\square}$	50 ~ 150	3 ~ 5	150 ~ 200	4 ~ 5	0.05 ~ 0.1



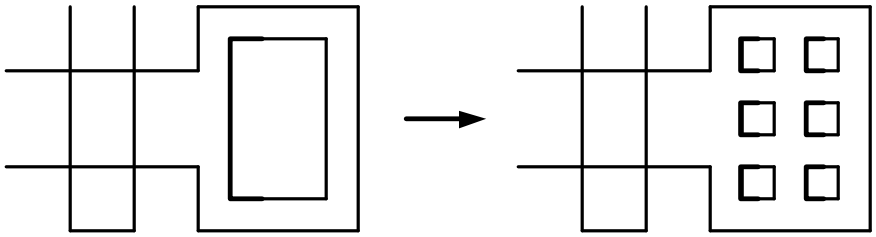
Unlike metal Si_2W and Si_2Ti can stand high temperature processing.

Contact Resistance



→ current flow from edges closes to active device due to **current crowding effect**

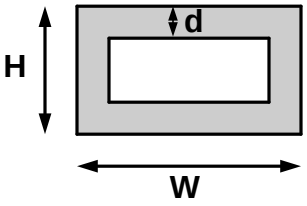
To add more perimeter divide a large contact to numerous small contact.



Contact resistance ↓

Skin effect

High frequency current goes through perimeter. (highrt field @ sharp edges pushes the current)



skin depth , $d = \sqrt{\frac{r}{pfm}}$? : resistivity

μ : permeability

lower resistivity → lower skin depth → more problems

0.69 of current flows through this skin depth.

Cross section :, skin effect → 2(W+H)d (cf. no skin effect → WH)

$$R = r\frac{L}{A} = r\frac{L}{2(W+H)d}\ , \qquad r = \frac{R}{L} = r(f) = \frac{r}{2(W+H)\sqrt{\frac{r}{pfm}}} = \frac{\sqrt{rpfm}}{2(W+H)}$$

onset of skin effects, fs → 2(W+H)d < W,H

2d = max(W or H) → $\frac{4r}{pfm} = [\max(WorH)]^2$

$$fs = \frac{4r}{pm[\max(WorH)]^2}$$ → skin effect show up in wider/taller metals

Inductance

Capacitance and inductance are always related

$C \cdot L = \mu \cdot \varepsilon$ = constant

Group velocity, $u = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{me}} = \frac{C_o}{\sqrt{e_r m_r}}$ in the material

C_o : speed of light,

μr = 1 unless you use magnetic, ferro- and para- materials

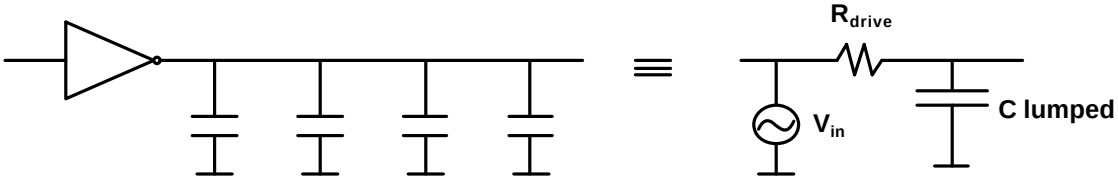
W = 0.4μ : C = 92aF/μm, L = 0.47pH/μm, r = 190mΩ/μm

W = 1μ : C = 110aF/μm, L = 0.39pH/μm, r = 75mΩ/μm

W = 10μ : C = 380aF/μm, L = 0.11pH/μm, r = 7.5mΩ/μm

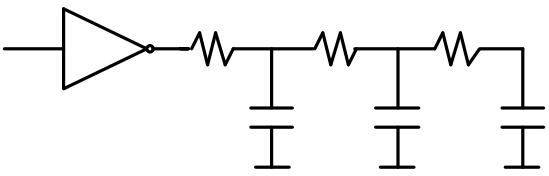
Wire Model

1. lumped capacitive

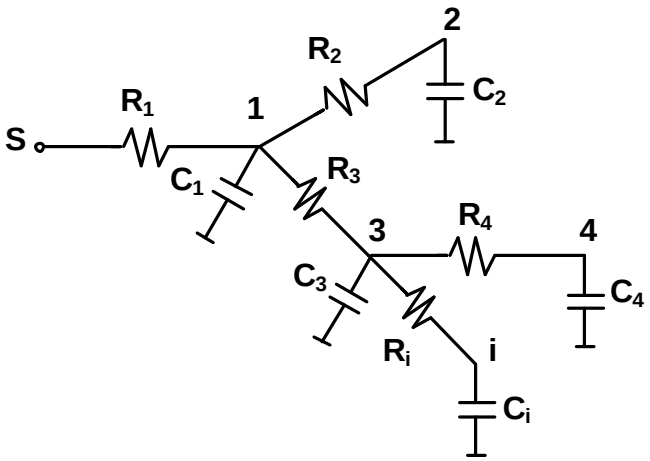


τ = RC → overestimates the delay as we will see soon

2. lumped RC Model



Elmore delay Formula



Path resistance : R_{ii}

$S \rightarrow i \quad R_1 + R_3 + R_i = R_{ii}$

Shared path resistance : Rik

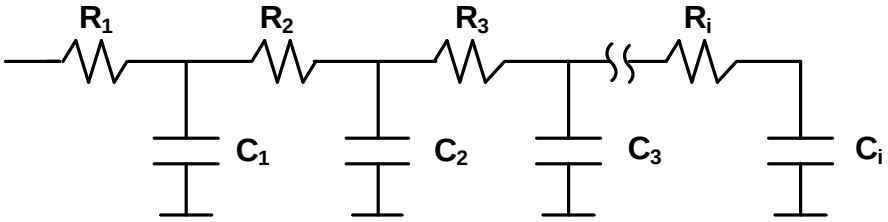
$S \rightarrow 1,2 : R_1 = R_{12}$

$S \rightarrow 2,3 : R_1 = R_{23}$

$S \rightarrow 1,4 : R_1 + R_3 = R_{14}$

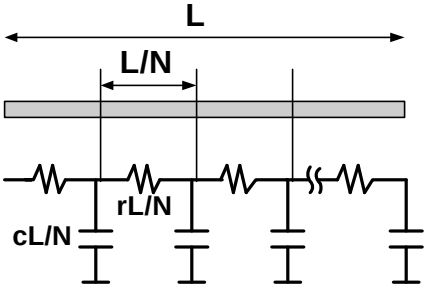
Elmore delay formula

$$t_{D_i} = \sum C_k R_k = R_1C_1 + R_1C_2 + (R_1+R_3)C_3 + (R_1+R_3)C_4 + (R_1+R_3+R_i)C_i$$



$$\tau_{Di} = C_1 R_1 + C_2 (R_1+R_2) + \cdots\cdots\cdots C_i(R_1+R_2+\cdots\cdots+R_i)$$

Distributed rc line



R = rL

C = cL

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \cdots\cdots + Nrc) = rcL^2 \frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

$N = 1 \rightarrow \tau = RC$

$N = \infty \rightarrow \tau = \frac{RC}{2} = rc\frac{L^2}{2}$

Delay : quadratic function of length

Delay → half of the delay of lumped RC Model

→ lumped RC Model is pessimistic

distributed rc line → complicated to calculate

	Lumped RC (N=1)	Distributed RC(N=∞)
t_p 0 → 50%	0.69 RC	0.38 RC
τ 0 → 63%	RC	0.5 RC
t_r 10% → 90%	2.2 RC	0.9 RC

Rule of Thumbs to use rc delay

rc delay should be considered when $t_{prc} \geq t_{pgate}$

critical length interconnect , L_{crit}

$$\tau_{prc} = 0.38RC = 0.38rcL^2 \rightarrow L_{crit} = \sqrt{\frac{t_{pgate}}{0.38rc}}$$

rc delay should be considered when input rise/fall time is smaller than RC rise/fall time

$t_{rise} < RC$, $t_{fall} < RC$

Transmission line effect

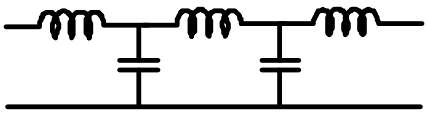
Rise/fall time → time of the flight of signal across the line

RC model → signal diffuses

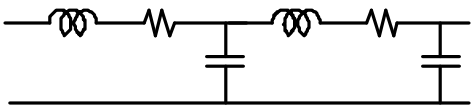
Transmission line model → signal propagates like a wave

Transmission line model

1. lossless transmission line model (only lc)



2. lossy rlc transmission line model



→ still assuming current through dielectric is negligible

Loss-less transmission line model

Wave function $\frac{\partial^2 u}{\partial x^2} = lc\frac{\partial^2 u}{\partial t^2}$, $lc = \frac{1}{u^2}$ =constant

group velocity, $u = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{me}} = \frac{C_o}{\sqrt{m_r e_r}}$ C_o : speed of light,

$\mu_r \sim 1$, ε_r : average dielectric constant

Propagation delay per unit wire length

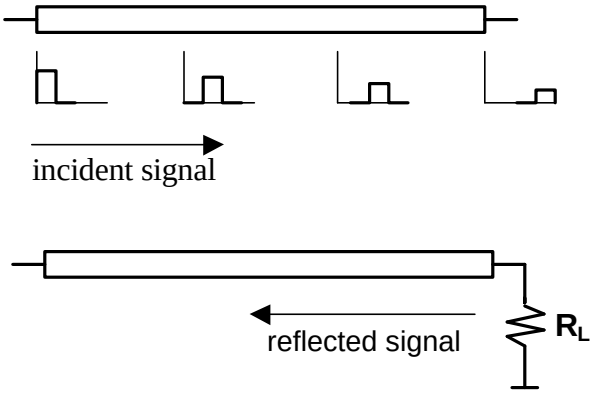
$t_p = \sqrt{lc}$ sec/m

Impedance of the line

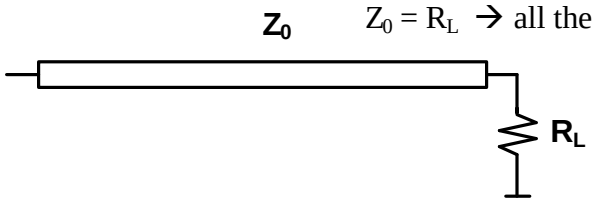
$z_0 = \frac{V}{I} = \sqrt{\frac{l}{c}}$ → characteristic impedance

independent of line length and frequency, only true for loss-less line

Signal propagation like a wave



Not always you get reflection → condition for no reflection



$Z_0 = R_L$ → all the signal is dissipated (transmitted)

Amount of reflection is determined by reflection coefficient, ?

$$r = \frac{V_{refl}}{V_{inc}} = \frac{R_L - Z_0}{R_L + Z_0}$$

$R_L = Z_0$ → rho = 0 : no reflection, matching condition

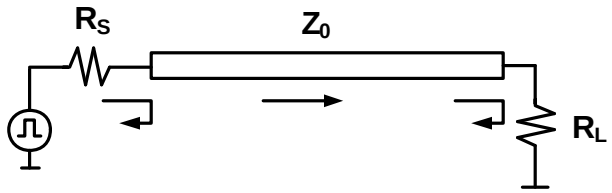
$R_L = \infty$ → rho = 1 : all the signal is reflected without phase change

$R_L = 0$ → rho = -1 : all the signal is reflected with 180^o phase change

(The sum of the signal and reflected signal @ the short termination = 0)

V@termination = $V_{inc}(1+rho)$

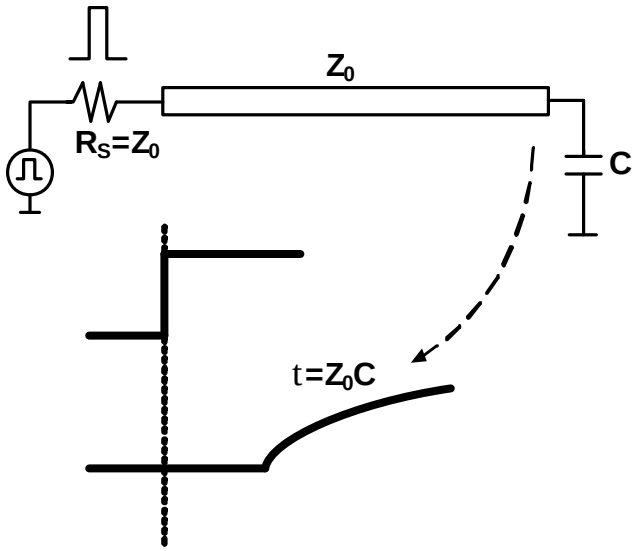
We also have reflection @ source



To have faster settling time → no reflection is desired → $R_S=R_L=Z_0$

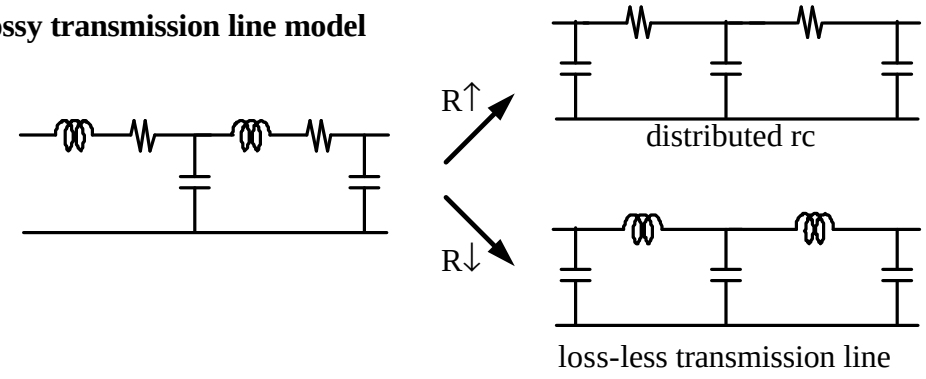
otherwise it takes a few propagation for the signal to reach steady-states

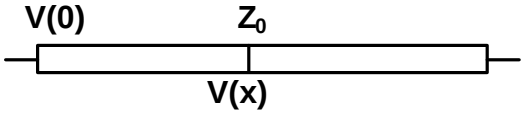
But in CMOS loads are usually capacitive



→ will be charged with a time constant of $\tau=Z_0C$

Lossy transmission line model





$$\frac{V(x)}{V(0)} = e^{\frac{-r}{2Z_0}x} \quad , \quad r = \frac{\text{resistance}}{\text{const length}}$$

Design Rule

(I) transmission line effects considered when t_r, t_f smaller than time of flight(t_{flight})

$$t_r(t_f) < 2.5t_{flight} = 2.5\frac{L}{u} \qquad u = \frac{C_0}{\sqrt{m_r e_r}}$$

If you assume capacitive instead of transmission line effect (ignoring inductive part)

→ optimistic t_p(propagation delay)

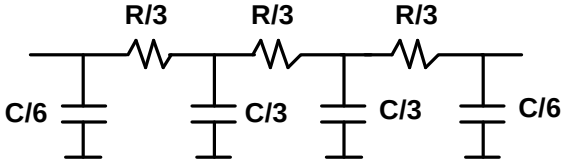
(II)transmission line effects considered when $R < 5Z_0$

If this does not hold → use distributed RC model

(I, II) Wire length, L $\qquad \frac{tr}{2.5}\frac{1}{\sqrt{lc}} < L < \frac{5}{r}\sqrt{\frac{l}{c}}$

Interconnect Spice Model

Distributed rc : RPERL
CPERL
L



p**/3 → 3% error**

Loss-less transmission line

Z0

TD : transmission delay

NL : electrical length of the line = $\frac{L}{l}$ ($l = \frac{u}{f}$, $TD = \frac{L}{u}$ → $TD = \frac{L}{fl}$)

→ NL = fTD