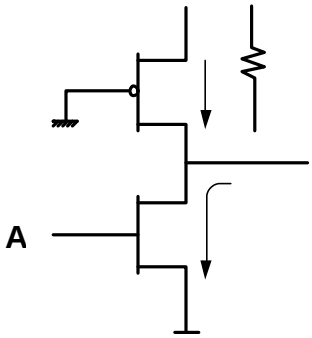
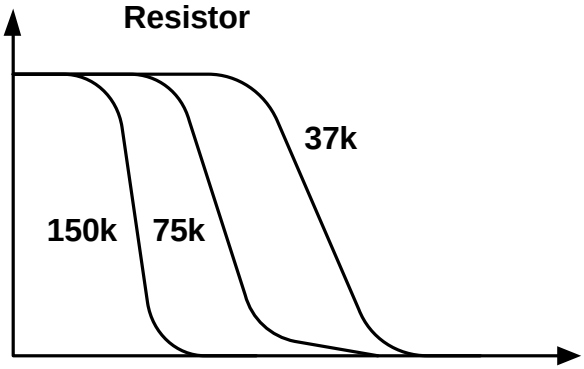
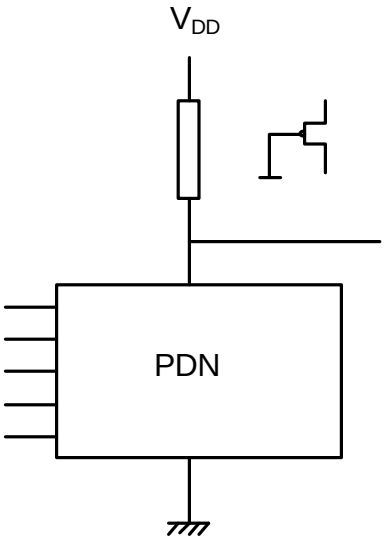
Ratioed Logic

Static logic → Ratioed logic





Ratioed logic



# of transistors in complementary logic = 2N

transistor in Ratioed logic = N+1

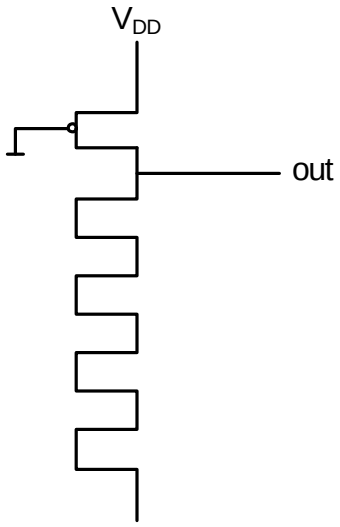
Advantages of Ratioed logic

- less # of transistors
- less interconnects → less complex layout

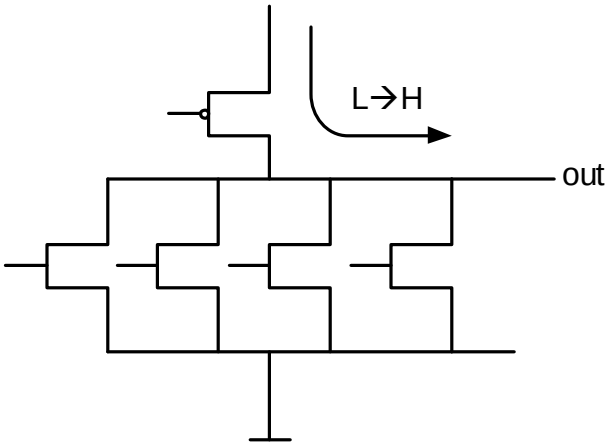
Disadvantages of ratioed logic

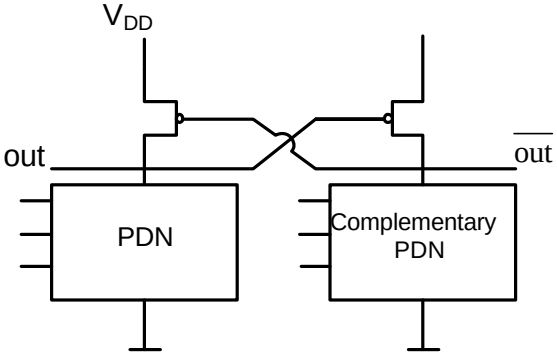
- Static power consumption when output = 0
- Level) depends on the ratio of PMOS to NMOS sizing
- slower in H→L transistors

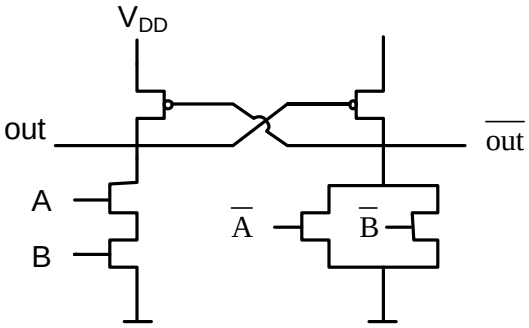
4-in NAND



4-in NOR



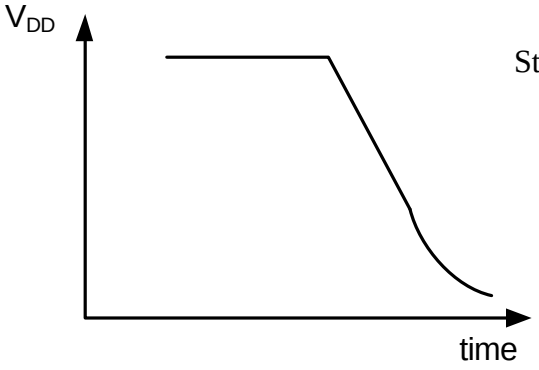




→ Different logic path positive feedback.

No direct path V_{DD} → 0 → static power = 0

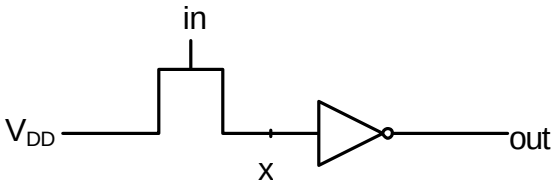
Out 1→0

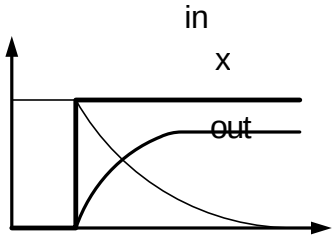


Still Ratioed logic since the transition is affected by sizing

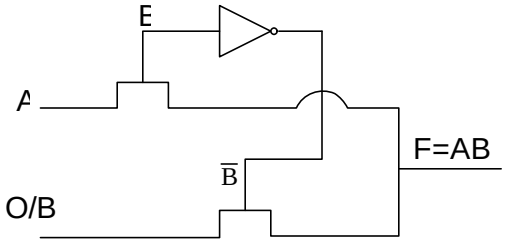
$V_{OL} = 0$

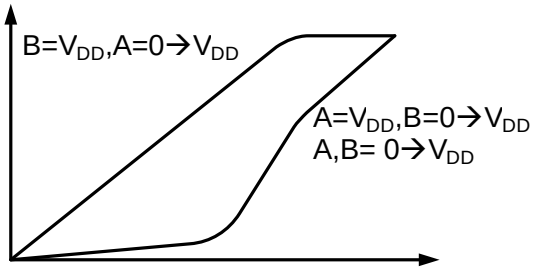
Pass transistor logic



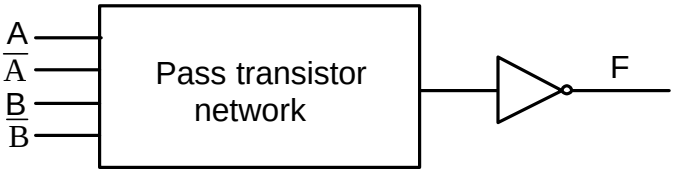


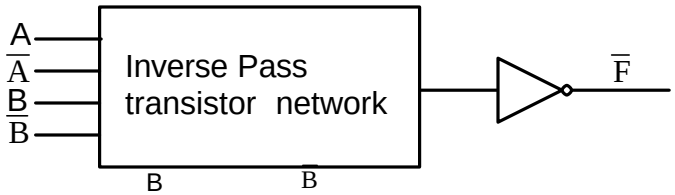
Pass transistor AND gate

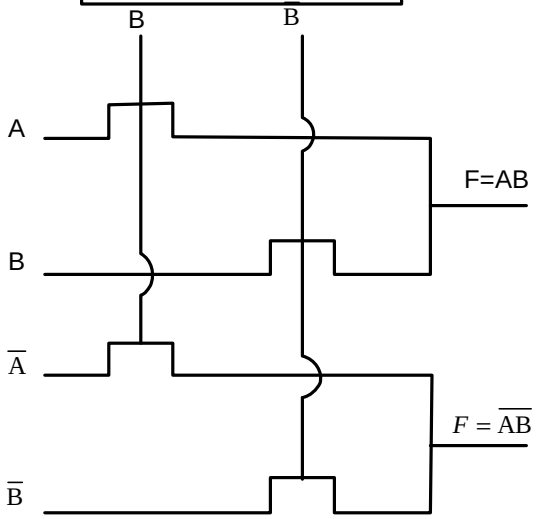




Complementary Pass transistor logic



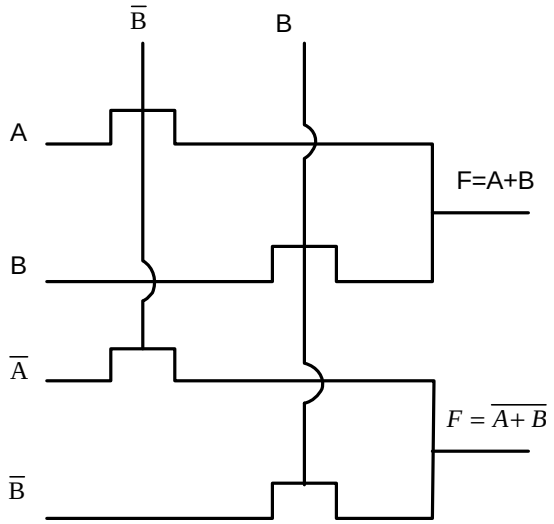




$$F = AB + B\overline{B} = AB$$

$$F = \overline{A}B + \overline{B}\overline{B} = \overline{A}B + B(A + \overline{A})$$
$$= \overline{A}B + A\overline{B} + \overline{A}\overline{B} + A\overline{B}$$
$$= \overline{A}(B + \overline{B}) + \overline{B}(\overline{A} + A)$$
$$= \overline{A} + \overline{B} = \overline{AB}$$

AND/NAND



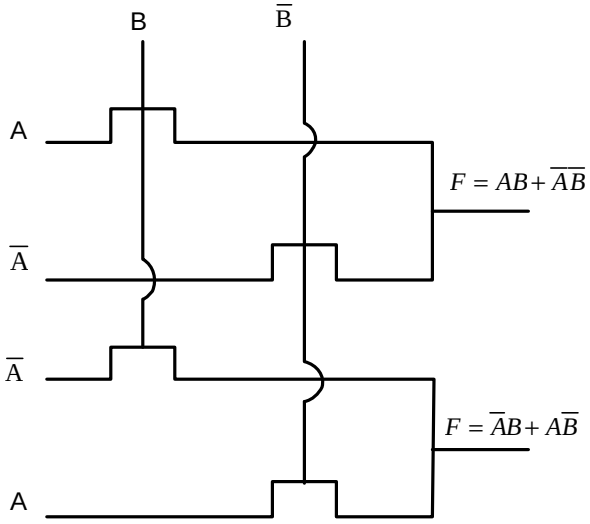
$= A\overline{B} + BB = A\overline{B} + B = A\overline{B} + B(A + \overline{A})$

$= A\overline{B} + BA + B\overline{A} + BA$

$= A(B + \overline{B}) = B(A + \overline{A}) = A + B$

$= \overline{A}\,\overline{B} + B\overline{B} = \overline{A}\,\overline{B} = \overline{A + B}$

OR/NOR



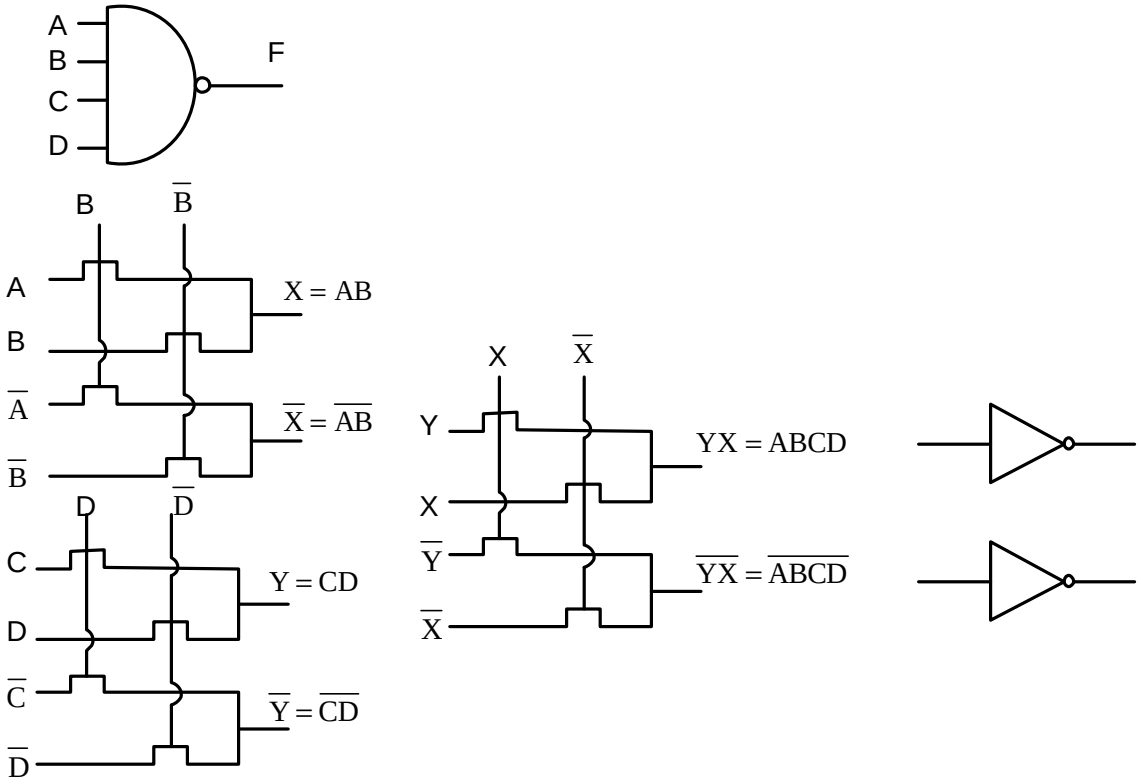
XOR/XNOR

→ Design are very modular

(all gates use exactly the same topology only the input are changed)

Problem arises when need more fan-in!

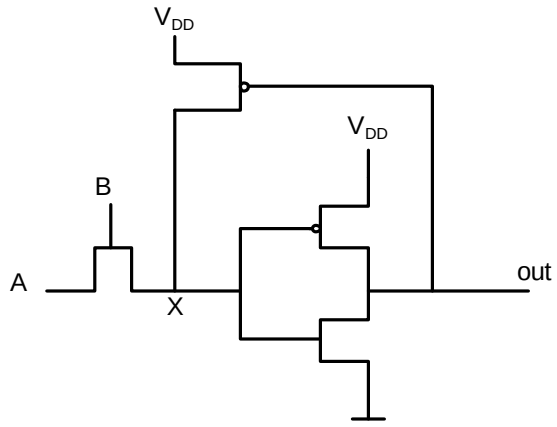
4-in NAND in CPL



Main problem with pass transistor is the level shift

To solve this problem

Solution 1. level restoration - using a PMOS transistor



X used to charge to V_{DD}-V_{th}

now the pmos transistor charges X to V_{DD}

Advantages

→ all levels are either Gnd or VDD

→ no static power

Disadvantages

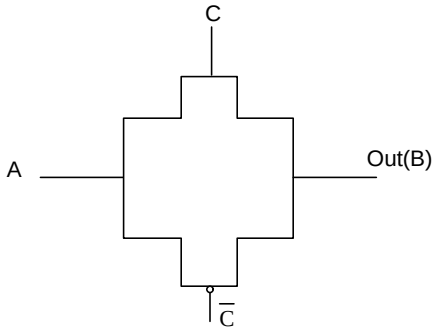
→ ratioed logic

→ pass trsnsistor has to be stronger than pmos

Solution 2 – multiple threshold transistor

zero or low threshold devices are used as pass transistors

Solution 3 - transmission Gate logic

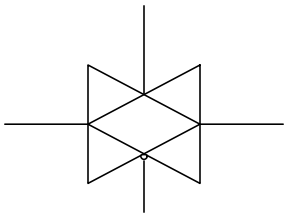


For charging out to V_{DD}

NMOS only charges it to V_{DD}-V_{tn}

But PMOS is still on and

continues charging up to V_{DD}



For charging out to 0

PMOS only discharges to V_{DD}-V_{tp}

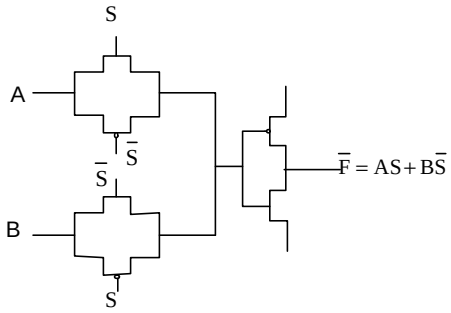
then PMOS turns off

but NMOS is still on V_G=V_{DD} and

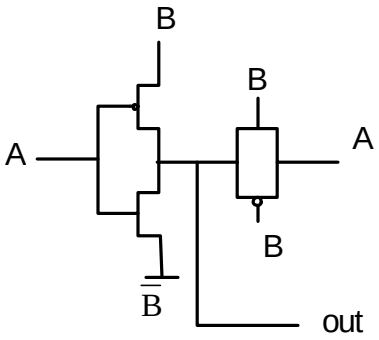
continues discharges to 0V

easy to make complex circuits

2-in MUX



XOR



B=1 → inverter enabled

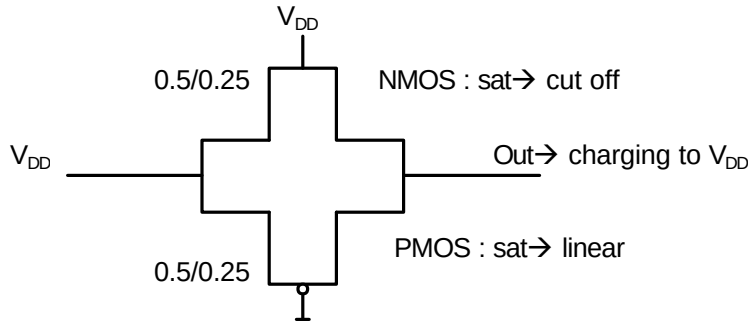
transistor gate disabled → $F = \overline{A}B$

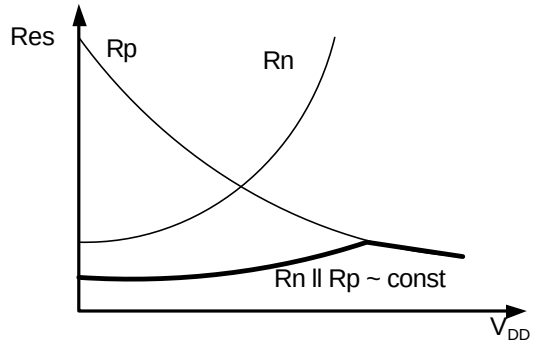
B=0 → inverter disabled

transistor gate enabled → $F = A\overline{B}$

→ $F = \overline{A}B + A\overline{B}$

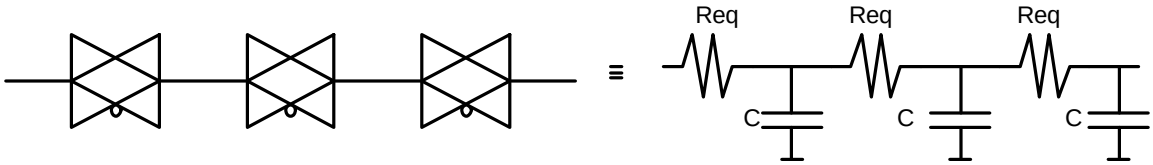
Delay of trans gate logic





→ transmission gate network Req = const is a very good assumption

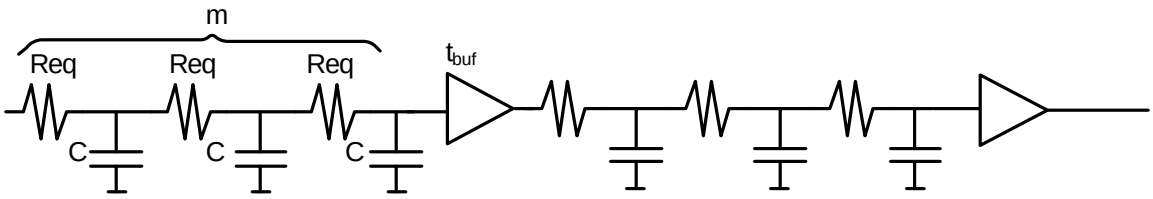
Delay in transmission gate network



Using Elmore delay

$$t_p = 0.69\sum_{k=0}^{n} C\mathrm{R}_{\mathrm{eq}} \cdot k \quad \rightarrow \; t_p = 0.69 CR_{eq}\frac{n(n+1)}{2} \quad \rightarrow \text{increase with } n^2$$

to improve the delay use buffer every m stage



Dependence becomes linear and not quadratic

$$t_p = 0.69\left[CR_{eq}\frac{n(m+1)}{2}\right] + \left(\frac{n}{m} - 1\right)t_{buf} \quad \text{optimum m} \rightarrow \frac{\partial tp}{\partial m} = 0 \rightarrow m_{op}t = 1.7\sqrt{\frac{t_{buf}}{CR_{eq}}}$$

$m_{opt} = 3 \sim 4$