Power Consumption

P_{peak}, peak power is important for supply line sizing

$P_{peak} = i_{peak}\ V_{supply} = \max[P(+)]$

$$P_{av} = 1/T \int_0^T P(t)dt = \frac{Vsupply}{T} \int_0^T isupply(t)dt$$

P(t) : instantaneous power

Power consumption : dynamic (charging up caps during transition)

static (true CMOS has no static consumption)

MOS 10pA leakage, 1M trans → static current 10mA

dynamic power consumption ∝ switching frequency

1.5A @1.8GHz → 4W

power consumption related to propagation delay

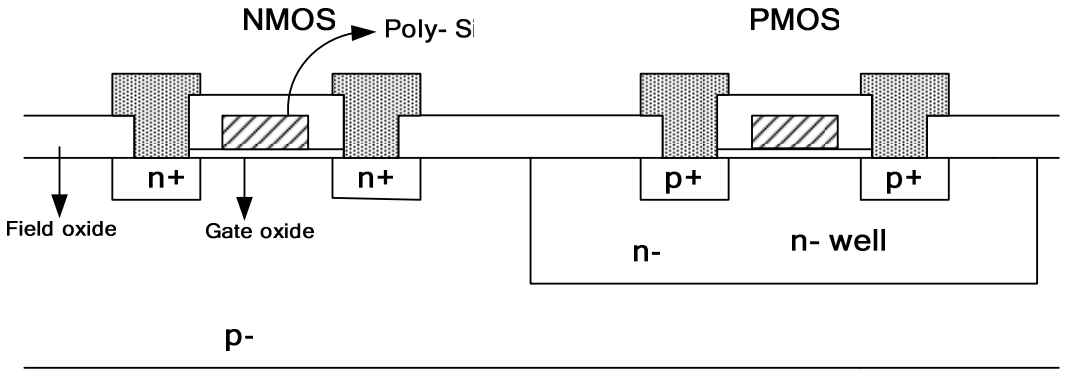
power delay product : $PDP = t_p \times P_{av}$

PDP measured by ring oscillator

CMOS Technology

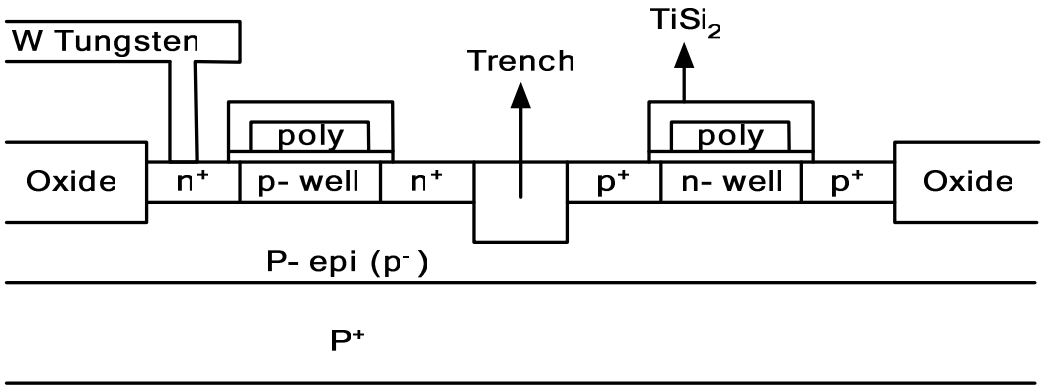
Smaller feature size : density ↑
switching speed ↑ → for the same of dynamic power ↓
V_{DD} ↓ → power decrease
leakage ↑ → static power ↑
cost/cm2 ↓ (cost of mask) 0.13μ $1M/step
cost/transistor ↑
complexity ↑

CMOS Process



n- well CMOS Process

New Processes use epi-layer



Dual- well epi process

IBM → 90nm trans. SOI substrate → f_T, f_{max} > 200GHz

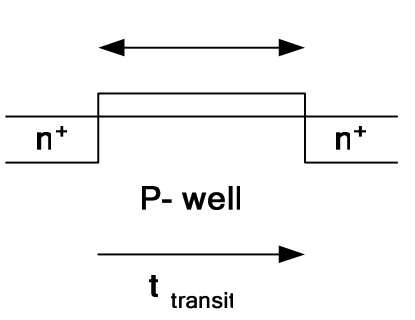
Silk layer (Dow chemical)

8-level of metallization → 2 of them are Cu (Copper interconnect)

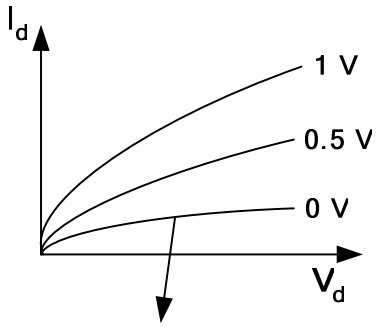
0.6V supply (digital)

0.9V supply (analog)

Short channel effects



reduced dynamic power

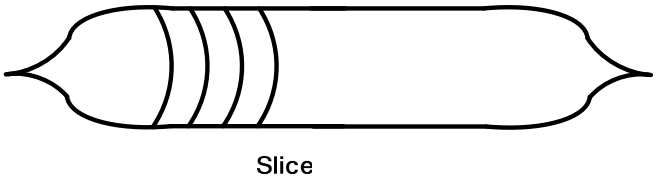


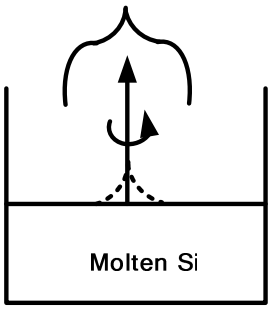
can not close the channel

→ Some leakage always exist

→ Increase static power

Si-wafer

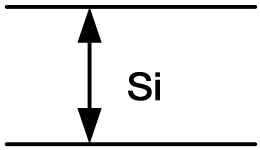




Thickness	Resistivity	Size
2mm(MEMS App.)	P- lightly doped sub. (30-100Ωcm)	4”
1mm	P+ highly doped (1-10 Ωcm)	↓
400µ	high resistivity (10k Ωcm)	12”
	after processing 1kΩcm	

200µ, 100µ, 50µ difficult to handle

Bulk → Bulk CMOS

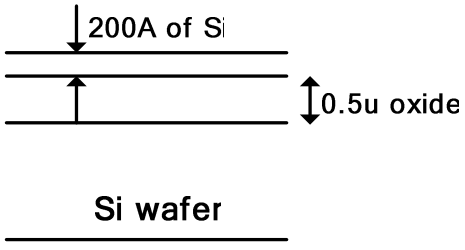


SOI → partially depleted, fully depleted

reduced parasitics → better performance 20% ↑

better on-off characteristics Simox wafers

→ implanting Oxygen in Si wafer

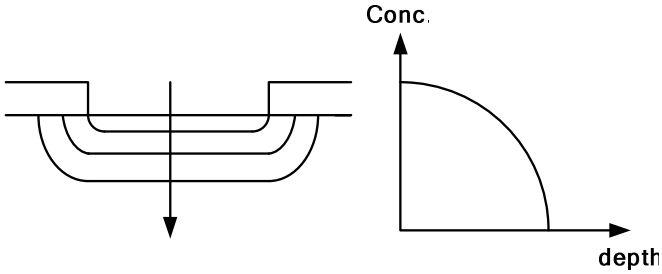


Photolithography

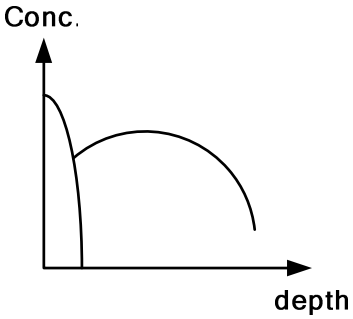
used for selective masking

Diffusion and Ion Implantation

Diffusion



Ion Implantation : Dose, Energy



Deposition

Field oxide, Si_3N_4 sacrificial (mask for ion implantation)

Etching

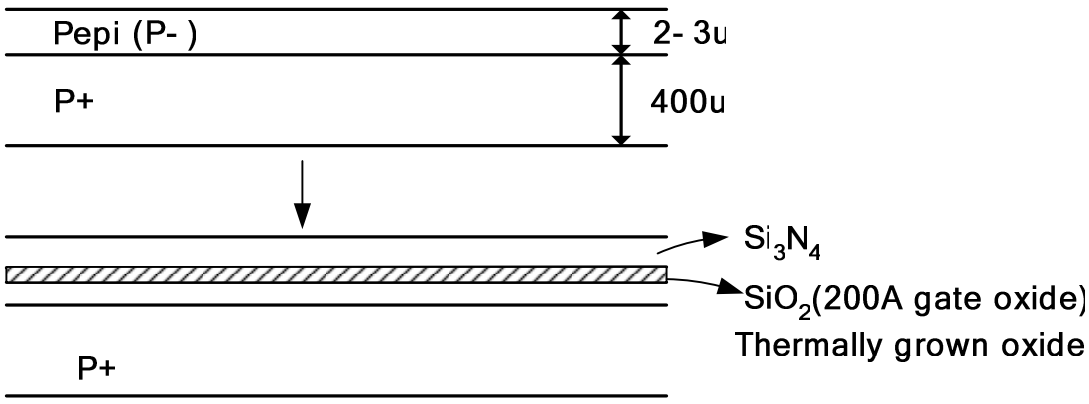
Wet & Dry etching (RIE-Reactive Ion Etching)

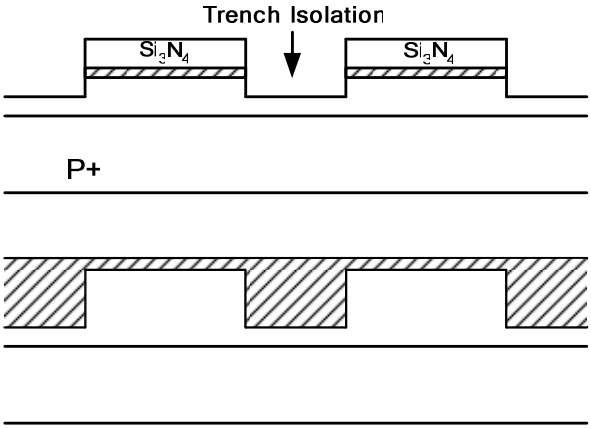
Planarization

For easy masking process

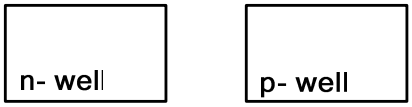
CMOS Process

Design rule (0.25μ) → set of minimum dimensions and spacing to get ~100% yield

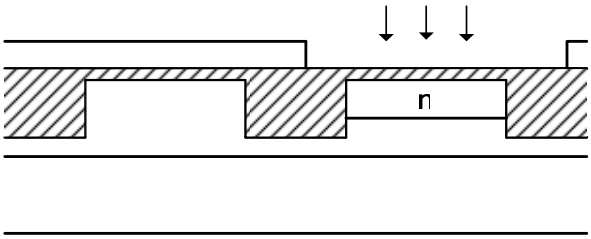




Use active mask

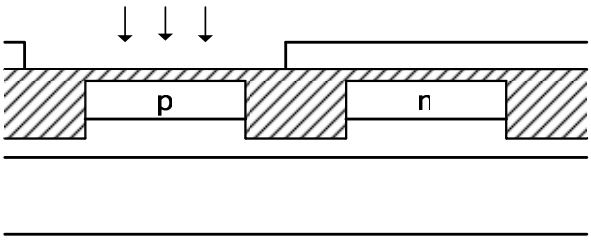


fill trenchs with field oxide(deposited)
+ Planarize

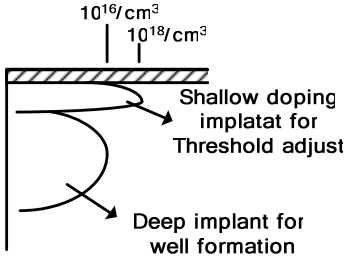


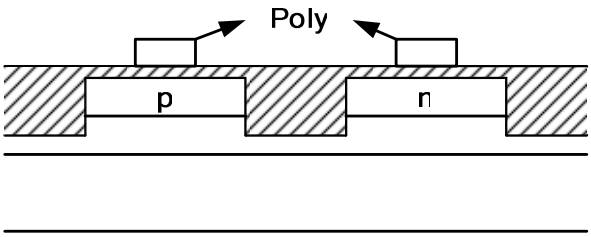
Use same active mask for
n- well and p- well formation

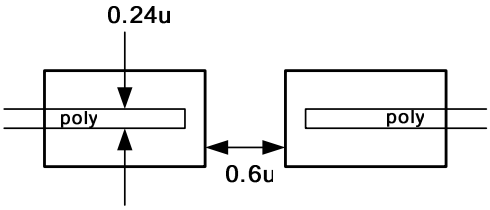
n- well
V_{TP} adjust

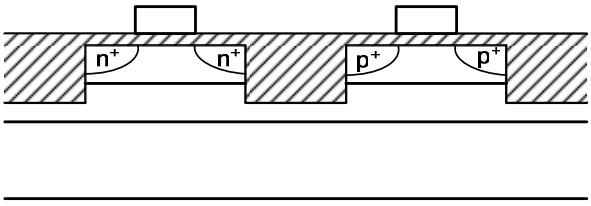


p- well
V_{TN} adjust



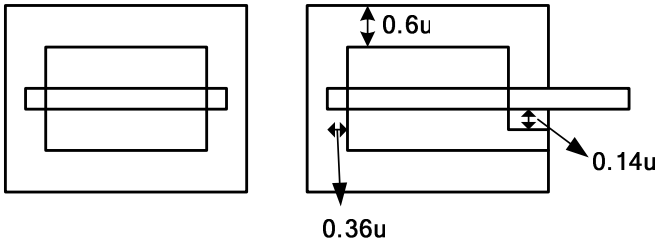


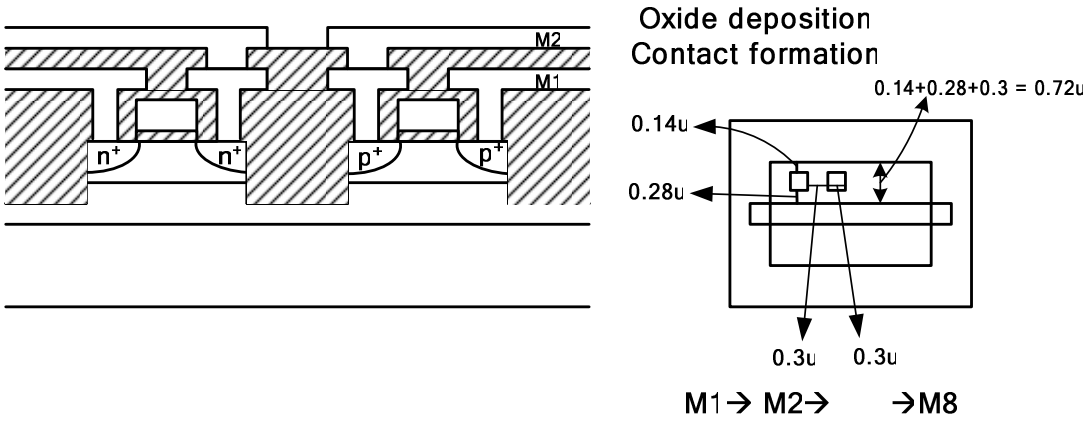




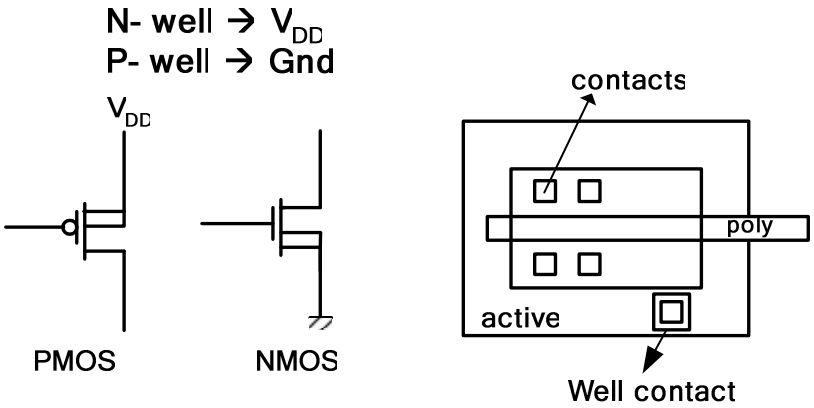
Source/drain implantation
(self- aligned process)

Select layers





⇒ to form a transistor



DRC (Design Rule Check)

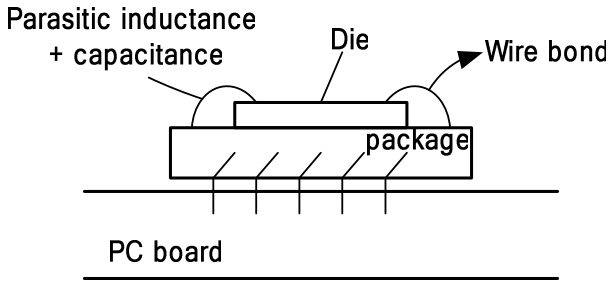
uses a technology file

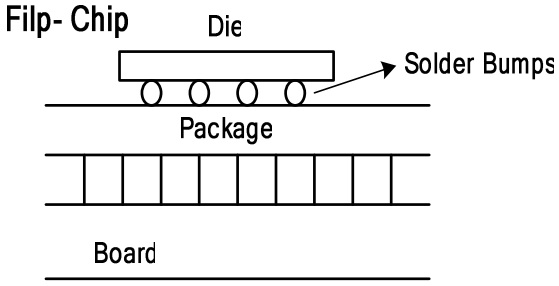
LVS (Layout vs. Schematic)

Extract circuit from layout → calculates parasitics

IC Packaging

Package account for 50% of delay





Different Packages : DIP → Dual-In-Line pakage

PGA → Pin-Grid-Array

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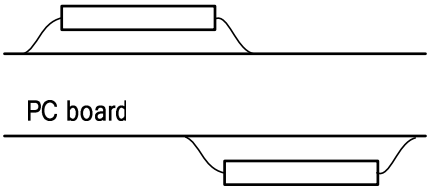
Surface mount → remove package

→ testing is difficult



Thermal Consideration

$$\frac{N_G}{t_p} \leq \frac{\Delta T}{\theta E}$$

N_G : number of gate/IC , t_P : Propagation delay

ΔT : max Temp. difference between IC & Environment

θ : thermal resistance from chip to environment

E : switching energy of each gate

$\Delta T/\theta = Q$: total power of IC

$Q \cdot t_p = PDP$: Power Delay Product

$NG \cdot E$ = total dynamic energy → assuming all gate are opening simultaneously

so thermal properties determine maximum integration level

→ activity factor = active gates/ total gates