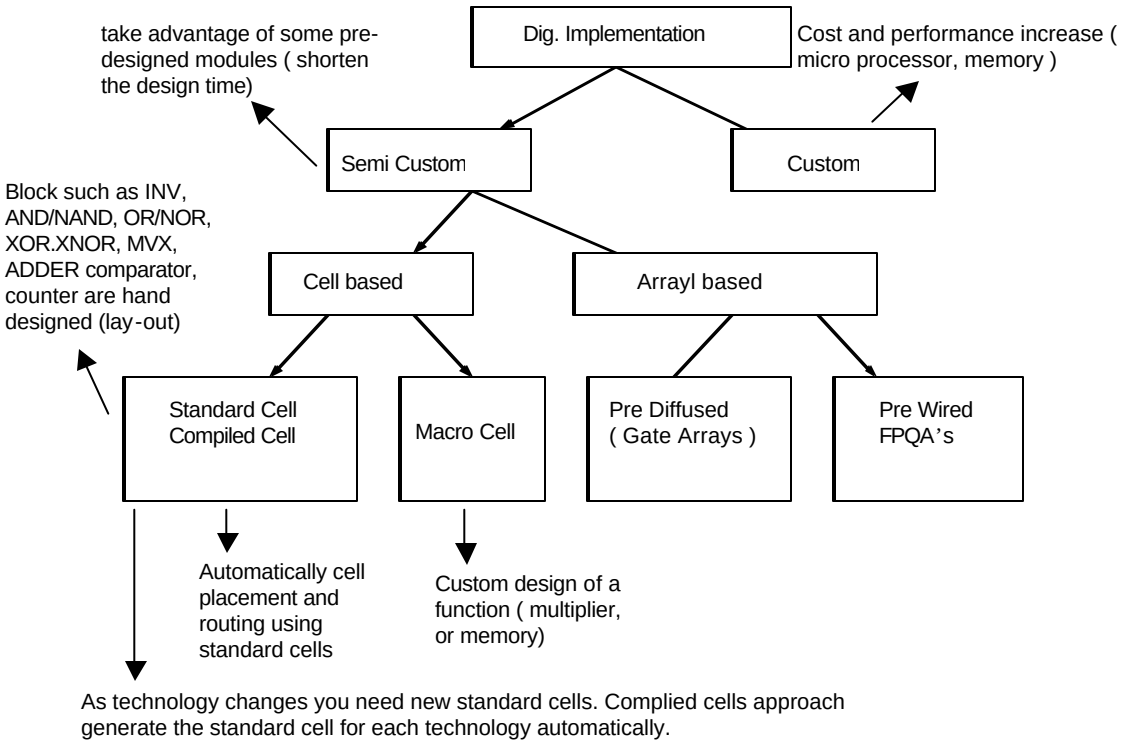
Implementing Strategies for Digital ICs



Semi custom Design Flow

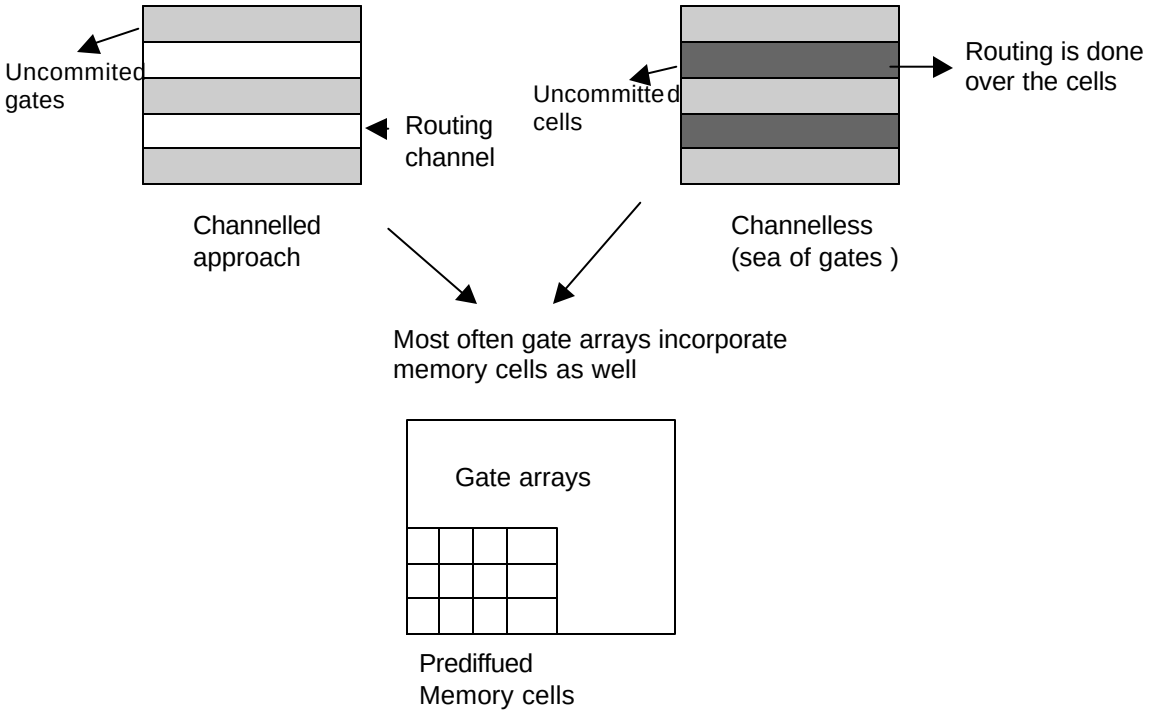
1. design capture using hardware description language (HDL) such as VHDL, Verilog, System C
2. logic Synthesis, module described by HDL
3. Prelayout Simulation and verification (performance analysis based on estimated parasitics)
4. Floor Planning → is done based on estimated module sizes
5. Placement → precise position of the cells is decided
6. Routing → interconnects between blocks
7. Extraction → model of the chip based on layout (device size, parasitics, caps and res)
8. Post layout simulation and verification
9. tape out

Array based implementation

The idea is to trade-off performance/size/power consumption to achieve quick design cycle.

Prediffused Arrays(Mask-programmable) (Gate Arrays)

Wafer is processed with transistors on then up to metallization step.(uncommitted cells). Connections after the Ckts is decided and next steps will be carried over.



Disadvantages

In the past with designing 50000 gates (design cycle → weeks) it made sense to save a few weeks in turn-around by using pre-diffused. Todays deep submicron technology allows you to put multi-million gates → design cycle (month) → saving few weeks does not make much sense, especially because metallization is the lengthy past of the process.

Advantages

Cost can be a deciding factor making sub 0.25u masks are $1M using pre-diffused arrays, you can only need max 1 sub 0.25 mask as most metallizations layers are not sub 0.25

Prewired Arrays (all the processing steps are done)

→ use fuse or antifuse to implement logic → need programming

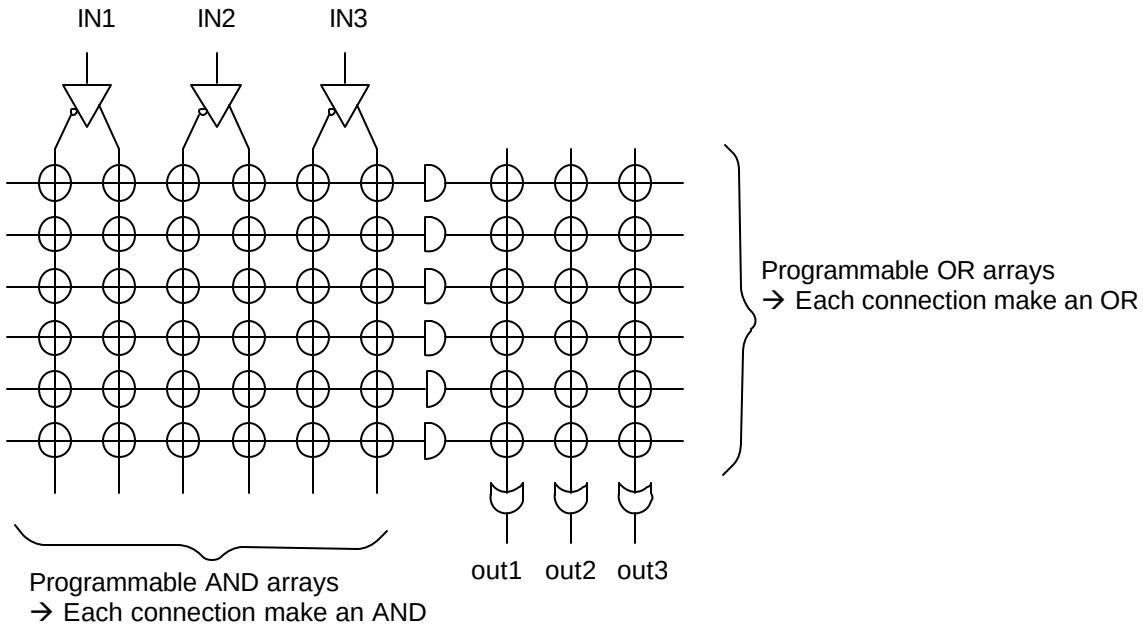
therefore called field-programmable Gate Arrays (FPGA)

Fused → thin metallization that can be blown using high voltage/high current

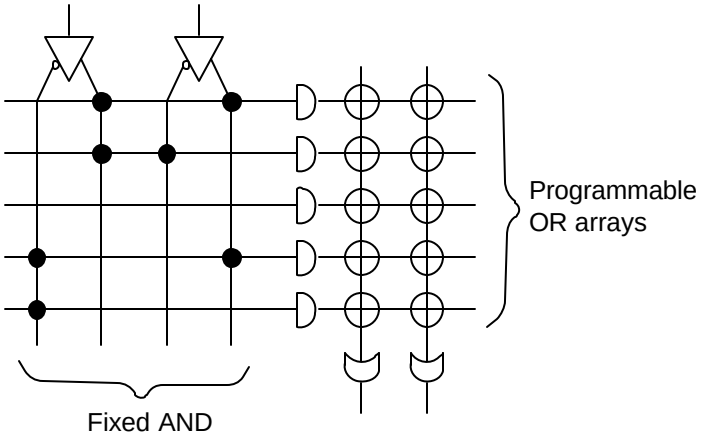
Antifuse → by applying high voltage → high field ONO will be melted and replaced by Poly → short circuit after programming

Antifuse is preferred as it reduces the programming time → you can need to make a few connection on an array (most fuses/antifuses have to be open ckt)

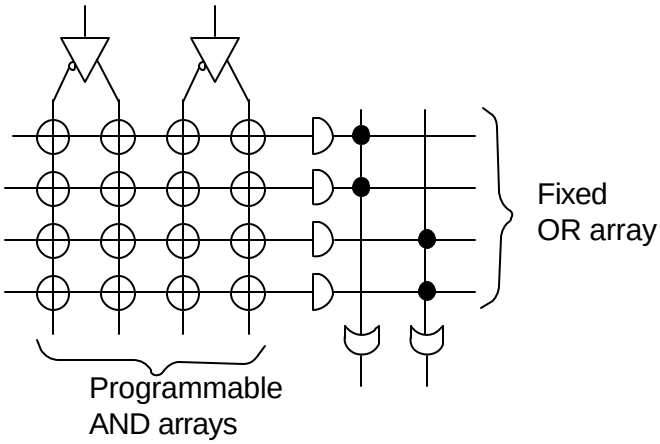
Programmable logic Array (PLA)



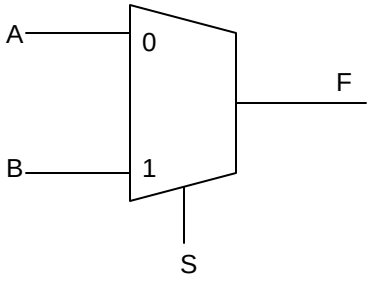
PROM (fixed AND Array)



PAL (Programmable Array logic)



Cell based programmable logic



A	B	S	F
0	0	0	0
0	X	1	X
0	Y	1	Y
0	Y	X	XY
X	0	Y	$X\overline{Y}$
Y	0	X	$\overline{X}Y$
Y	1	X	X+Y
1	0	X	$\overline{X}$
1	0	Y	$\overline{Y}$
1	1	1	1

You can get any function by Deciding what input is Provided to the MVX

The inputs are decided using fuses in the array

Programmable interconnect

Instead of blowing fuses you can use pass transistor