Advanced Current Mirrors and OPAMPs

Short channel length L → degraded output resistance → current mirrors such as cascode with high output resistance are needed → signal swing is limited in cascode as 2 transistors have to stay in saturation.

Wide-swing Cascode Current Mirror

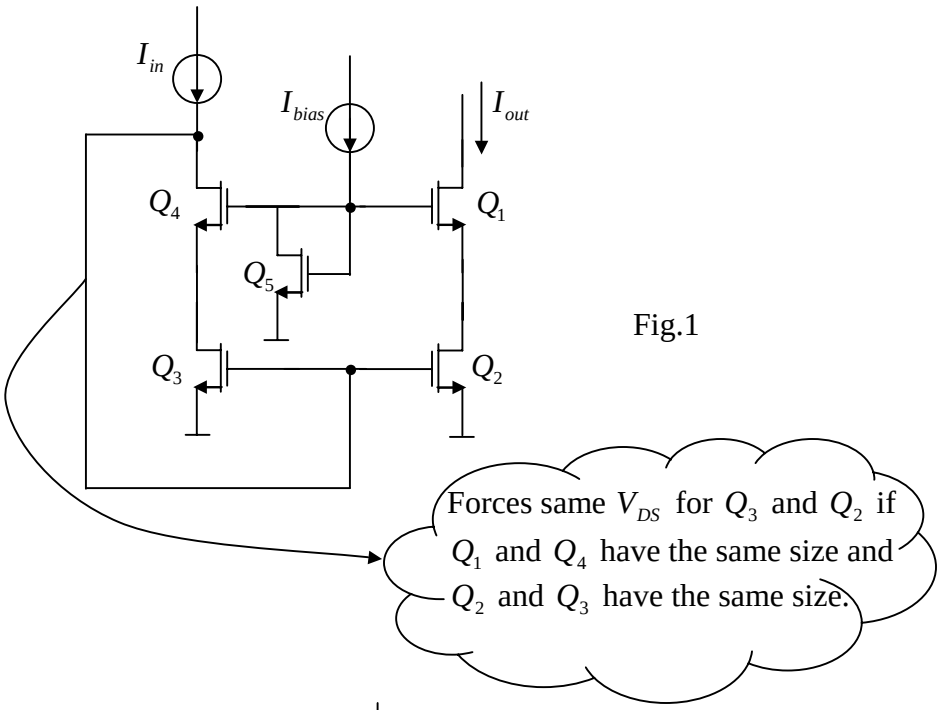


Fig.1

Function of Q_4

Circuit can work without Q_4:

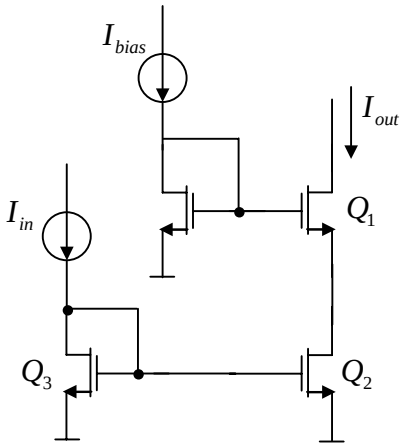


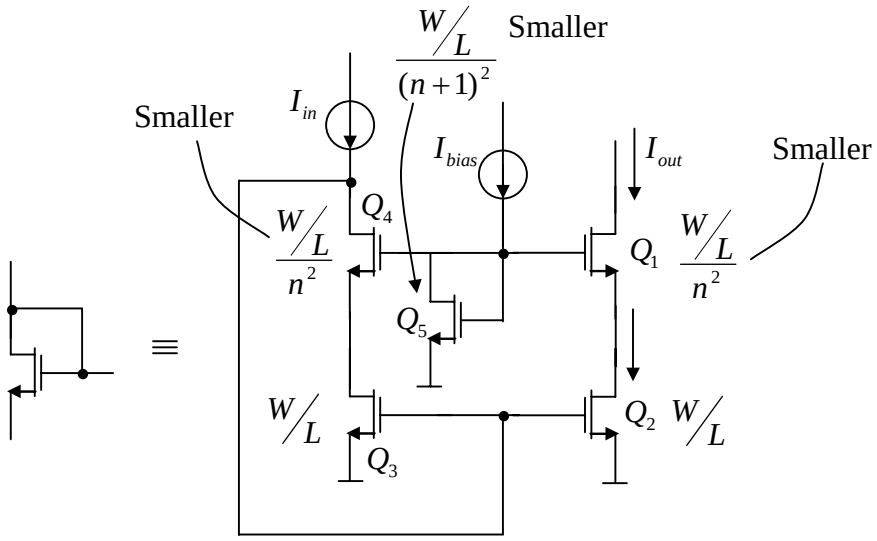
Fig.2

The difference that Q_4 makes is to reduce drain-source voltage across Q_3 → Q_3 and Q_2 drain-source voltage will be very close in the presence of Q_4.

→ Since output impedance (resistance) of the transistors Q_3 and Q_4 are finite, keeping their drain-source voltage the same helps making $I_{out} = I_{in}$ independent of their r_{ds}.

So all Q_3-Q_4 does is to act like a diode connected transistor as shown in Fig2.

Transistor sizing is important for propos function of the current source. For now let's assume all the drain current are equal.



Q_3 and Q_4 are current mirrors → $V_{gs_2} - V_{tn} = V_{gs_3} - V_{tn} = \sqrt{\dfrac{2I_{D_2}}{\mu_n C_{ox}(\frac{W}{L})}}$

our assumption (needs to be verified) → $I_{D_2} = I_{D_5}$ →

$$\mu_n C_{ox}(\frac{W}{2L})(V_{GS_2} - V_{tn})^2 = \mu_n C_{ox}\frac{W}{2L(n+1)^2}(V_{GS_5} - V_{tn})^2$$

→ $V_{GS_2} - V_{tn} = \dfrac{V_{GS_5} - V_{tn}}{n+1}$ → $\boxed{V_{GS_5} - V_{tn} = (n+1)(V_{GS_2} - V_{tn})}$

For the same reason:

$$V_{GS_1} - V_{tn} = V_{GS_4} - V_{tn} = n(V_{GS_2} - V_{tn})$$

$$V_{GS_1} = n(V_{GS_2} - V_{tn}) + V_{tn}$$

Gate of Q_4, Q_5 and Q_1 are connected together →

$$V_{G_5} = V_{G_4} = V_{G_1} = V_{GS_5} = (n+1)(V_{GS_2} - V_{t_n}) + V_{t_n}$$

Connection $= V_{DS_2}$

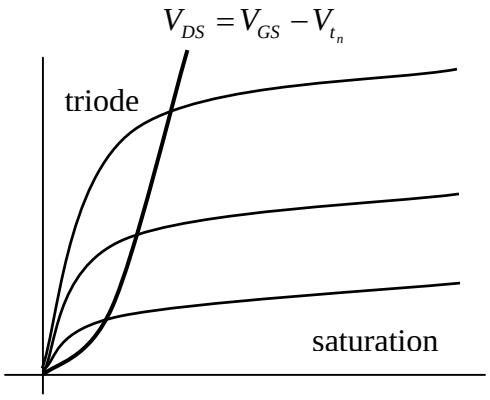
$= V_{G_5}$

$$V_{DS_2} = V_{DS_3} = V_{GS_5} - V_{GS_1} = (n+1)(V_{GS_2} - V_{t_n}) + V_{t_n} - n(V_{GS_2} - V_{t_n}) - V_{t_n}$$

Because of symmetry } Q_4 forces this relationship.

$$\Rightarrow V_{DS_2} = V_{DS_3} = V_{GS_2} - V_{t_n} = V_{GS_3} - V_{t_n}$$

→ Both Q_2 and Q_3 are at the edge of triode regime.



Minimum output voltage can be calculated:

$V_{out} > V_{DS_{1\min}} + V_{DS_{2\min}}$ → $V_{DS_{Q_2}}$ is always at minimum.

$$V_{out} > V_{GS_1} - V_{t_n} + V_{GS_2} - V_{t_n}$$

$$V_{out} > n(V_{GS_2} - V_{t_n}) + V_{GS_2} - V_{t_n}$$

$$V_{out} > (n+1)(V_{GS_2} - V_{t_n})$$

For $n=1 \Rightarrow V_{out} > 2(V_{GS_2} - V_{t_n})$

If you set $(V_{GS_2} - V_{t_n}) = 0.2v \Rightarrow V_{out} > 0.4v \rightarrow Q_4$ has to be in saturation as well

$$V_{DS_4} = V_{G_3} - V_{DS_3} = V_{GS_3} - (V_{GS_3} - V_{t_n}) = V_{t_n}$$

Connection
to keep Q_4 in saturation

$$V_{DS_4} > V_{GS_4} - V_{t_n}$$

$$\Rightarrow V_{t_n} > n(V_{GS_2} - V_{t_n})$$

If $\left.\begin{array}{l} V_{GS_2} - V_{t_n} = 0.2v \\ \text{and} \quad V_{t_n} = 0.5v \end{array}\right\} \rightarrow n_{\max} = 2.5 \Rightarrow n = 1, \text{ or } 2$ is acceptable.

Remember that we assumed $I_{D_5} = I_{D_3} = I_{D_2}$

$\Rightarrow I_{bias} = I_{in} = I_{out}$ has to be satisfied. But I_{in} and I_{out} may vary depending on the V_{out} (finite output resistance)

If you set $I_{bias} = \max(I_{in})$ *or* I_{out}, then all transistors will stay in saturation.

Variation in designs

- $\left(\frac{W}{L}\right)_5$ is typically smaller than $\frac{(W/L)}{(n+1)^2}$ to ensure Q_2 and Q_3 have slightly larger V_{DS} than minimum → helps offset body effect in Q_1 and Q_4 that pushes Q_2 and Q_3 to triode regime
- $\left(\frac{W}{L}\right)_5$ and I_{bias} can be scaled down (same current density) to save power in I_{bias} branch
- L of Q_2 and Q_3 set to minimum ~$0.18\,\mu$ in $0.18\,\mu$ technology

  L of Q_1 and Q_4 can be double the min size ~ 0.36μ (same $\frac{W}{L}$ as in the figure)

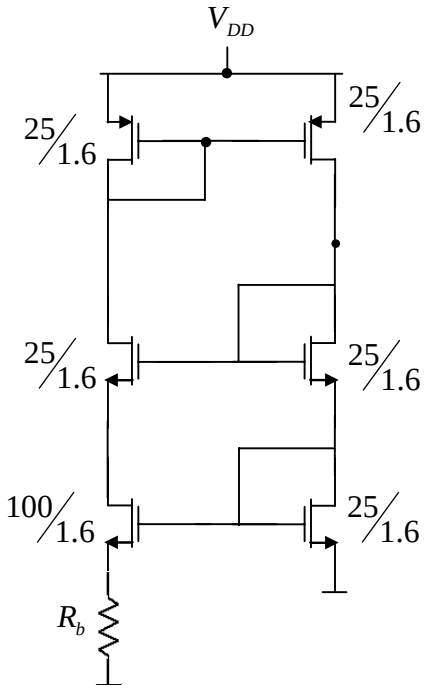
Larger L helps boosting output resistance of Q_1.

This current mirror is the most popular current mirror design.

Wide Swing Constant-Transconductance Bias Circuit

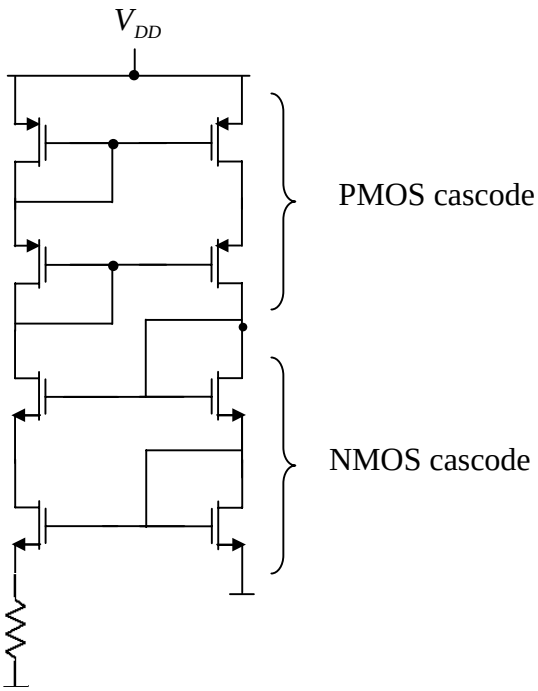
Remember the biasing circuit of the previous OPAMP (I_D, g_m independent of V_{DD})

We can make this bias circuit wide swing.

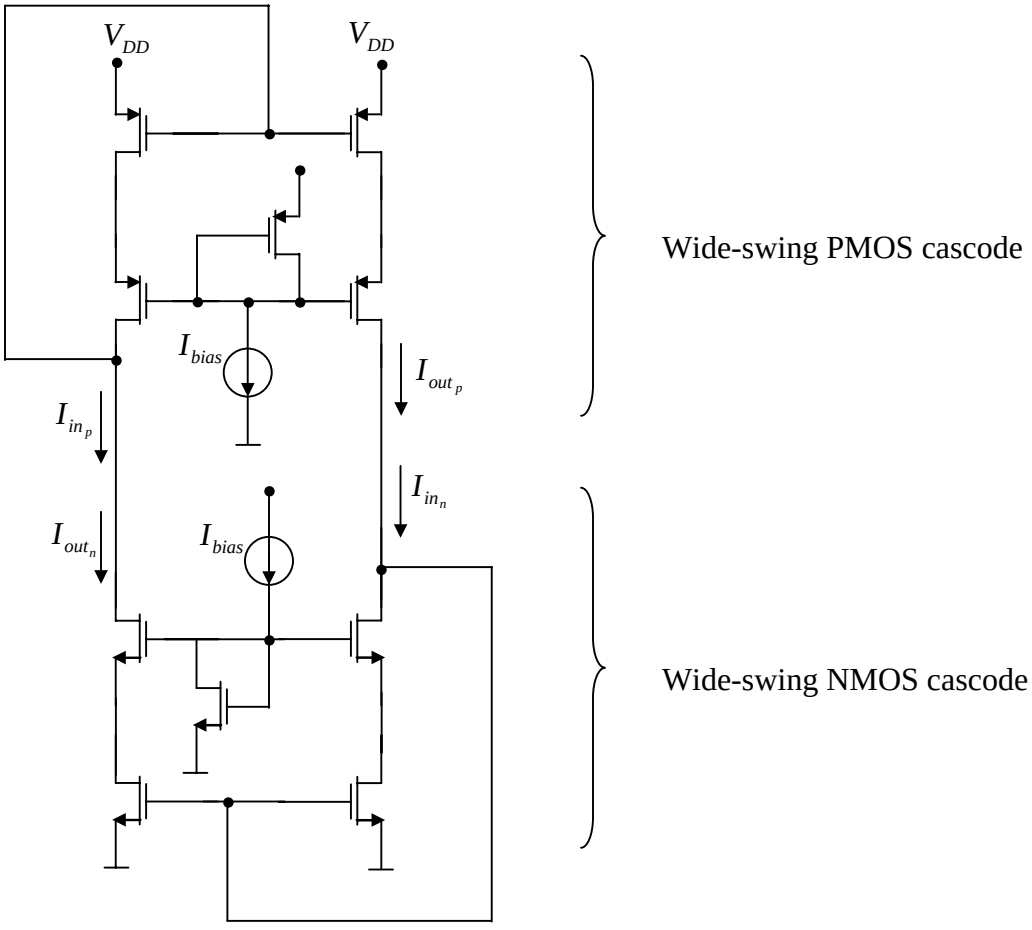


1st modification:

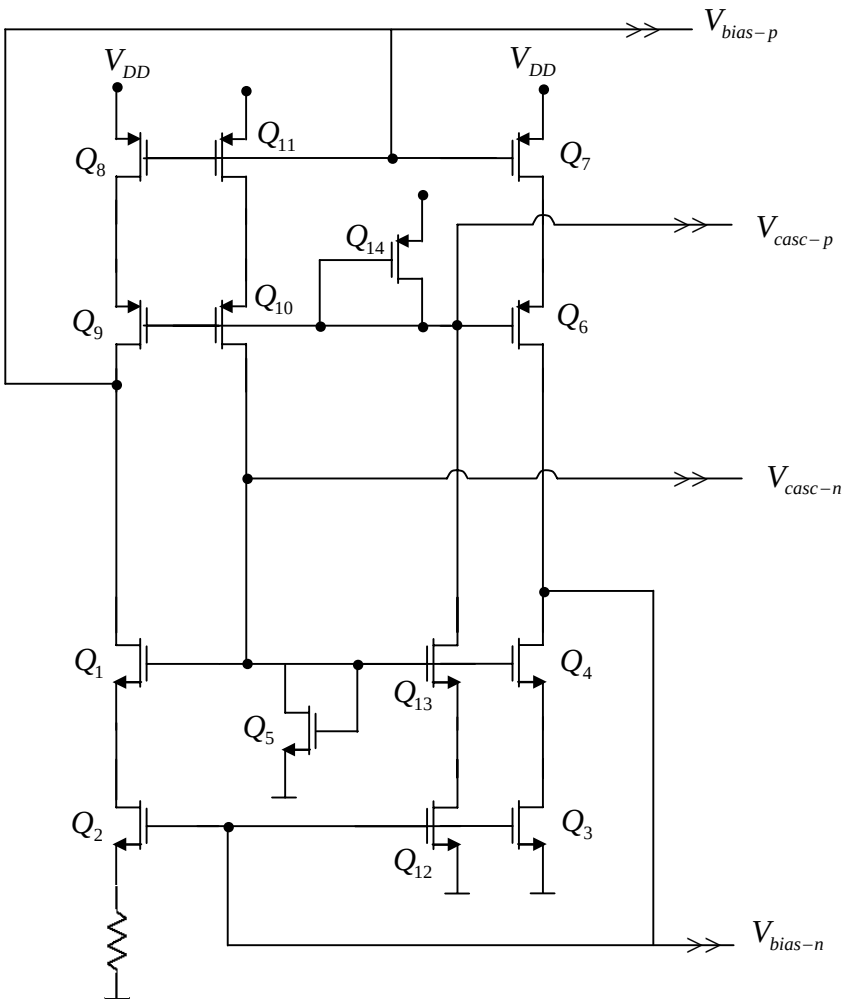
Instead of PMOS current mirrors use PMOS cascode current mirrors (1)



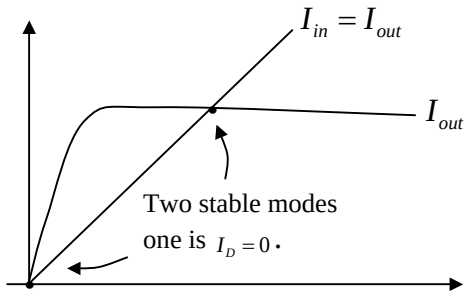
Now substitute the cascode with wide-swing cascade:



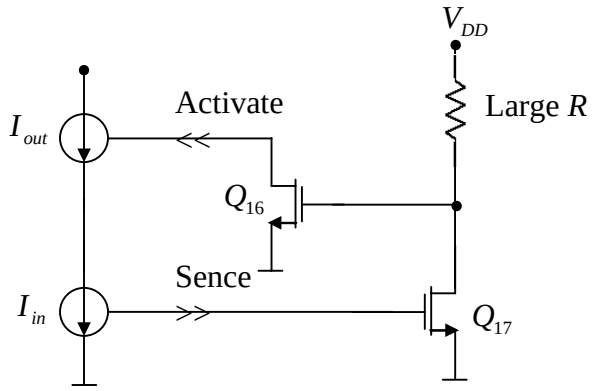
So the circuit looks like this:



Problem is there are two stable modes for this circuit.

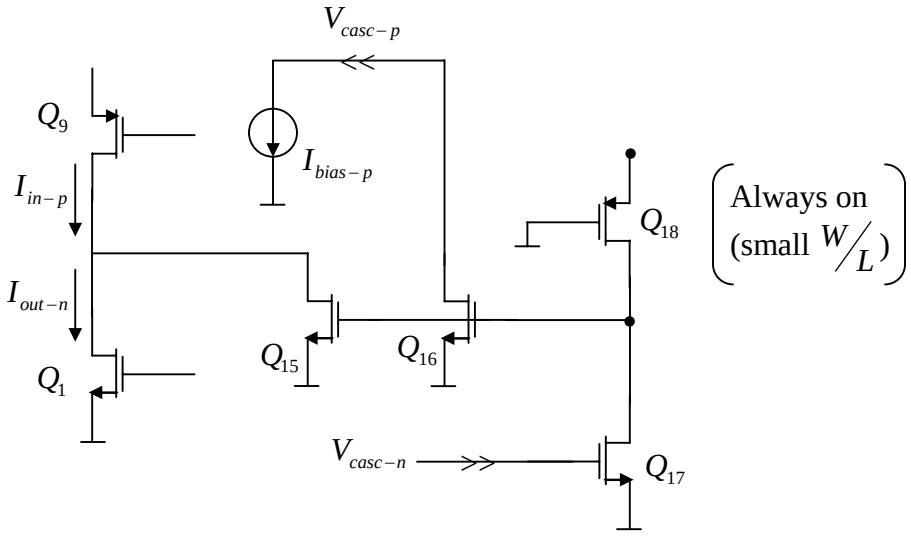


Therefore a lot of biasing circuits like the one discussed here use start-up circuitry.



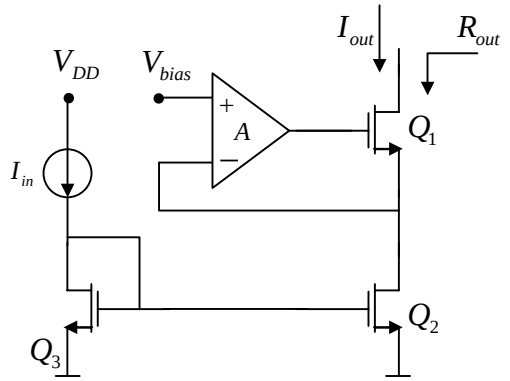
When there is no current in $I_{in} = I_{out}$ branch, then Q_{17} is off → gate of Q_{16} rises → Q_{16} is on → I_{out} starts to flow ↑ → I_{in} ↑ → Q_{17} is on now and remain on → Q_{16} is off.

Current in start-up circuitry must be small so we typically use large *R*.



Enhanced output impedance current mirrors

Use feedback to increase output impedance



Cascode output impedance

$$r_{out} = r_{ds_1}(1 + r_{ds_2} g_{m_1}) \approx r_{ds_1}.r_{ds_2} g_{m_1}$$

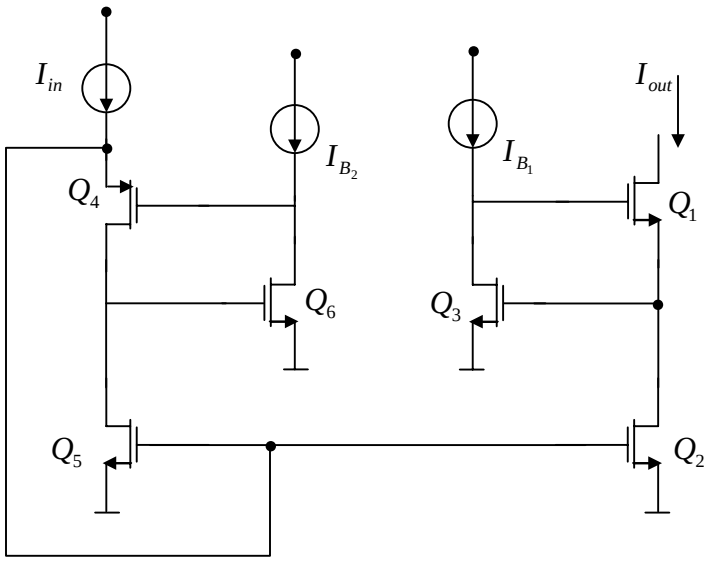
With feedback

$$R_{out}\big|_{with\ \ feedback} = r_{out}(1 + A)$$

$$\rightarrow R_{out} = g_{m_1} r_{ds_1} r_{ds_2} (1 + A)$$

In reality output resistance will be limited by a mechanism known as impact ionization.

Implementation



Q_3 is the feedback amplifies (common-source), if I_{B_1} output is equal to r_{ds_3} (same current for both devices).

$A = g_{m_3} \frac{r_{ds_3}}{2}$ ← feedback stage gain

$$R_{out} = r_{out}(1+A) \approx Ar_{out} = \frac{g_{m_3} r_{ds3}}{2} \times g_{m_1} r_{ds_1} . r_{ds_2}$$

$$\Rightarrow \mathrm{R}_{out} = \frac{g_{m_1} g_{m_3} r_{ds_1} r_{ds_2} r_{ds_3}}{2}$$

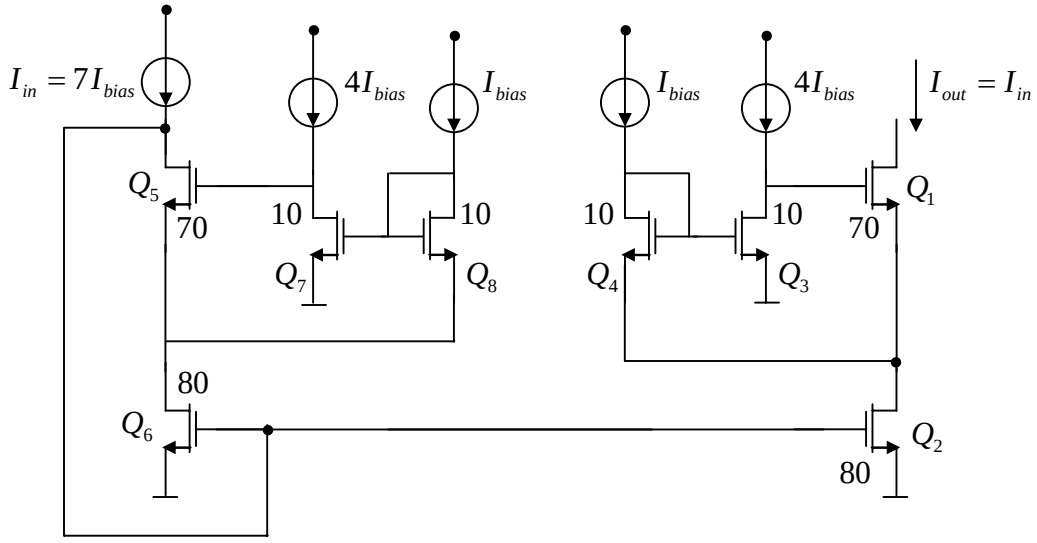
Q_4, Q_5 and Q_6 works just like a diode connected transistor except that because of perfect symmetry current in Q_2 and Q_5 are exactly identical → $\mathrm{I}_{out} = \mathrm{I}_{in}$ as V_{out} varies.

Problem with this realization is that the circuit is not wide-swing mainly because Q_2 and Q_5 are not biased at their minimum V_{DS}.

$V_{DS_2} = V_{DS_5} = V_{G_3}$ → Not $V_{GS} - V_{tn}$ so this is not small voltage!

Wide swing high impedance

To improve the voltage swing at V_{out} we use the following circuit:



Q_3 and Q_7 have 4 times higher current density.

$$\frac{I_{D_3}}{(W/L)_3} = \frac{I_{D_7}}{(W/L)_7} = 4 \times \frac{I_{D_1}}{(W/L)_1}$$

$$\rightarrow V_{G_3} - V_{t_n} = V_{G_7} - V_{t_n} = 2 \times (V_{G_1} - V_{t_n})$$

2
4
5
6
8

$$\Rightarrow V_{G_3} = 2\,(V_{GS_4} - V_{t_n}) + V_{t_n}$$

For Q_2 $\Rightarrow V_{DS_2} = V_{S_4} = V_{G_3} - V_{GS_4} = 2(V_{GS_4} - V_{t_n}) + V_{t_n} - V_{GS_4}$

$\rightarrow V_{DS_2} = V_{GS_4} - V_{t_n} = V_{GS_2} - V_{t_n}$ $\rightarrow$ Q_2 is biased on the edge of triode region

$\rightarrow$ Min output voltage: $V_{out} > V_{DS_2} + V_{GS_2} - V_{t_n}$

$$= 2(V_{GS_2} - V_{t_n})$$