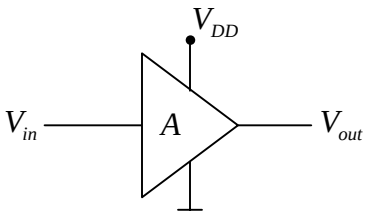
Operational Amplifier

Need for high gain stage:



$V_{out} = AV_{in}$

$A \to \infty$

problem is that with V_{in} having even small DC component

V_{out} will be saturated to either V_{DD} or ground.

Assume $V_{DD} = 3v$

$A = 100{,}000$

$V_{in} = 1mvDC + 1\mu v.Cos(2\pi ft)$

$V_{out} = AV_{in} = 100v + 0.1v.Cos(2\pi ft)$

We don't have 100v bias on the amplifier

$\Rightarrow \quad V_{out} \approx V_{DD} = 3v \quad \Rightarrow$ so the gain stage will not work if DC signal is present.

How about noise?

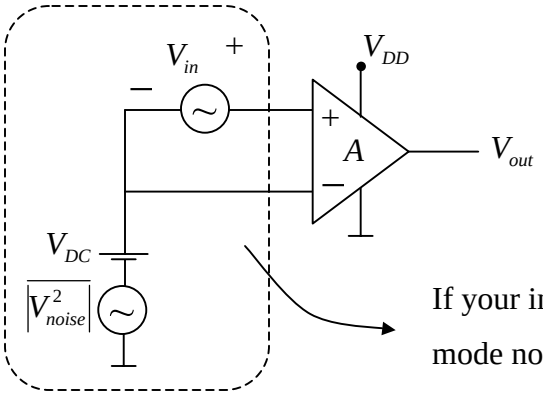
$V_{in} = 1\mu v.Cos(2\pi ft) + 10\mu v \ \ noise \quad \rightarrow \quad V_{out} = 0.1v.Cos(2\pi ft) + 1v \ \ noise$

Signal

Therefore the noise masks the output performance because it is amplified with the same gain as signal being amplified.

Solution

→ use high gain differential amplifier.



If your input signal has DC component or common mode noise component it will not be amplified by the differential amplifier.

Assume: $A_{|diff \ \text{mode}} = 100{,}000$

$A_{|common \ \text{mode}} = 0.01$

$V_{in|diff} = 1\mu v Cos(2\pi ft)$

$\overline{|V_{noise}|} = 100\mu v \ \ ac$

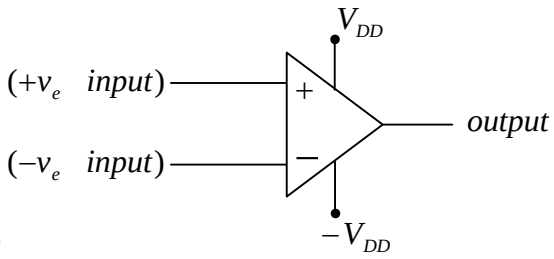
$V_{DC} = 1v$

$\rightarrow \ V_{out} = A_{|diff \ \text{mode}}.V_{in|diff} + A_{|common \ \text{mode}}(V_{DC} + \overline{|V_{noise}|})$

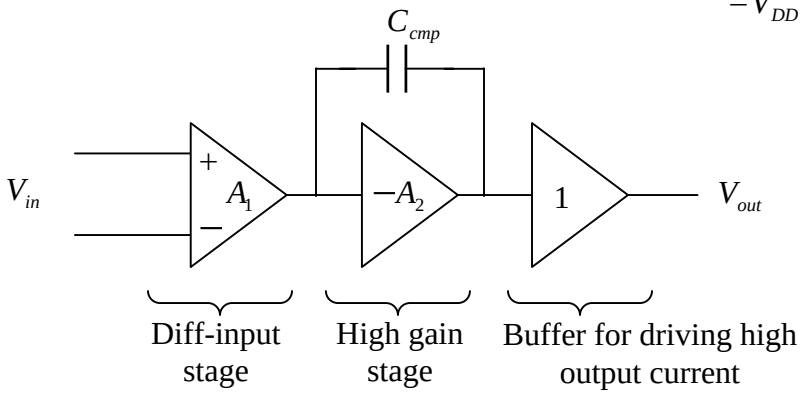
$= 0.1v Cos(2\pi ft) + 0.01v + 1\mu v_{|noise}$

$+ added \ \ noise \ \ of \ \ the \ \ diff - amp$

High gain differential-stage are called <u>OPAMPS</u>

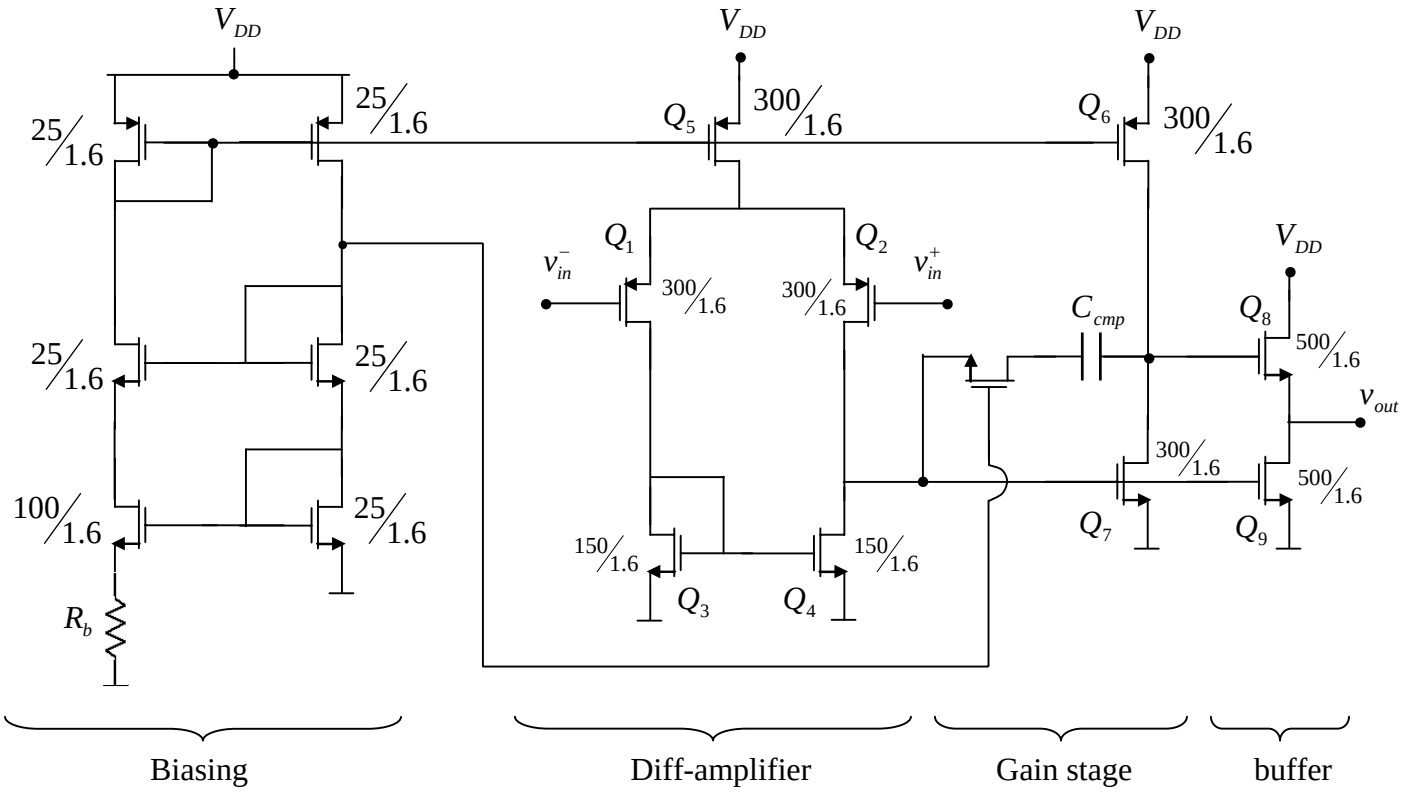


Usually they are built as following:



C_{cmp} is used to stabilize the system when if is need with feedback.

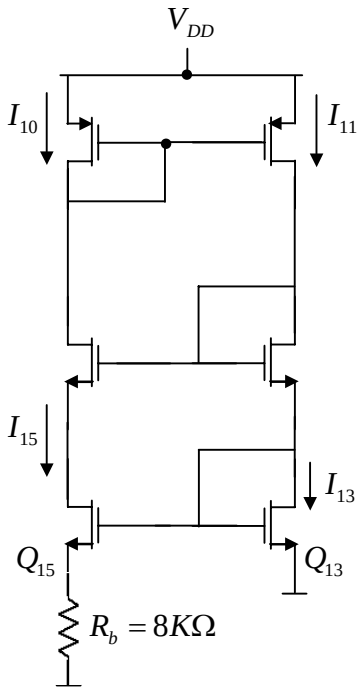
<u>Example of such OPAMP</u>



Let's simplify it:

Biasing: 2 PMOS current mirror

4 NMOS → cascode current source with source degeneration



$$I_{10} = I_{11} = I_{15} = I_{13}$$

$$I_{13} = \frac{\mu_n C_{ox} W_{13}}{2L_{13}} \times (V_{GS_{13}} - V_{t_n})^2$$

$$V_{GS_{13}} = V_{GS_{15}} + I_{15} \times R_b$$

$$I_{15} = \frac{\mu_n C_{ox} W_{15}}{2L_{15}} \times (V_{GS_{15}} - V_{t_n})^2$$

$$I_{15} = I_{13} \;\rightarrow\; W_{15}(V_{GS_{15}} - V_{t_n})^2 = W_{13}(V_{GS_{13}} - V_{t_n})^2$$

$$\left.\begin{array}{l} W_{15} = 100\mu m \\ W_{13} = 25\mu m \end{array}\right\} \;\rightarrow\; 2(V_{GS_{15}} - V_{t_n}) = (V_{GS_{13}} - V_{t_n})$$

$$\rightarrow\; 2V_{GS_{15}} - V_{GS_{13}} = V_{t_n}$$

$$\rightarrow\; 2V_{GS_{15}} - V_{GS_{15}} - I_{15}R_b = V_{t_n} \quad \rightarrow\; V_{GS_{15}} - V_{t_n} = I_{15}R_b$$

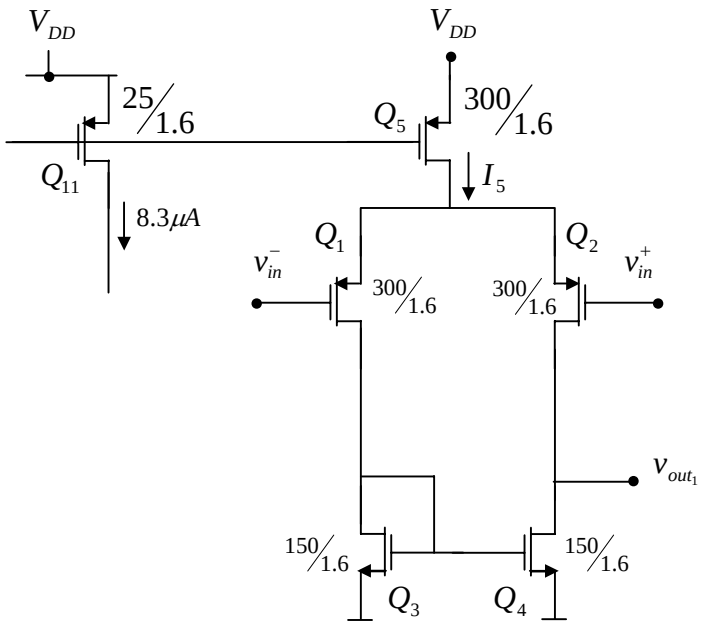
$$I_{15} = \frac{\mu_n C_{ox} W_{15}}{2L_{15}} \times (V_{GS_{15}} - V_{t_n})^2 = \frac{\mu_n C_{ox} W_{15}}{2L_{15}} \times (I_{15}R_b)^2$$

Current independent of V_{DD}.

$$\rightarrow\; I_{15} = \frac{2L_{15}}{\mu_n C_{ox} W_{15} \times R_b^2} = I_{10} = I_{11} = 8.3\mu A$$

$$R_b = 6.2K\Omega,\; \mu_n C_{ox} = 100\,{}^{\mu A}\!/_{V^2},\; L_{15} = 1.6\mu m,\; W_{15} = 100\mu m$$

Differential Amplifier:



$$I_5 = \frac{W_5}{W_{11}} \times I_{11} = \frac{300}{25} \times 8.3\mu A \approx 100\,\mu A \;\rightarrow\; I_{D_1} = I_{D_2} = 50\,\mu A$$

The diff-stage is differential input- single stage output.

Therefore the gain is:

$$A_{v_1} = \frac{v_{out_1}}{v_{in}^+ - v_{in}^-} = g_{m_1}(r_{ds_2} \,||\, r_{ds_4})$$

$$\left.\begin{aligned} g_{m_1} &= \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 . I_{D_1}} \\ \mu_p C_{ox} &= \frac{1}{3}\mu_n C_{ox} = 33\,{}^{\mu A}\!/_{V^2} \end{aligned}\right\} \;\rightarrow\; g_{m_1} = \sqrt{2 \times 33 \times 10^{-6} \times \frac{300}{1.6} \times 50 \times 10^{-6}}$$

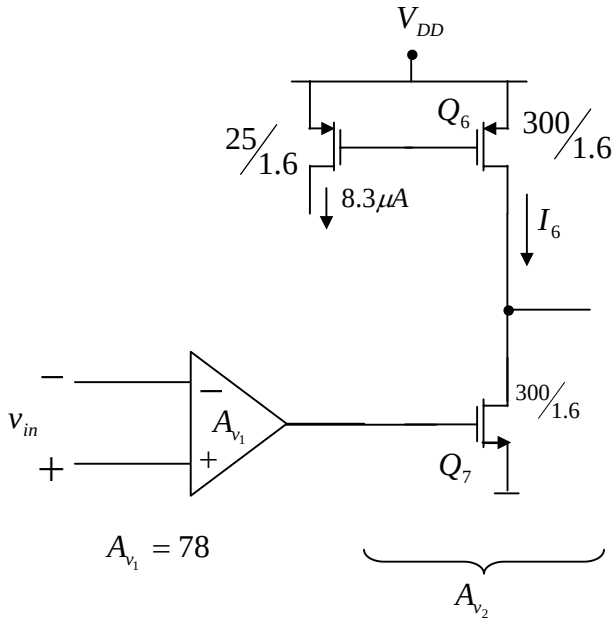
$$\boxed{g_{m_1} = 0.78\,{}^{mA}\!/_{V} = g_{m_2}}$$

Assume $\lambda = 0.1$:

$$r_{ds_2} = r_{ds_4} = \frac{1}{\lambda I_D} = \frac{1}{0.1 \times 50 \times 10^{-6}} = \frac{10^6}{5} = 200K\Omega$$

$$\rightarrow\; A_{v_1} = 0.78 \times (200 \,||\, 200) = 78$$

Gain-stage



$$A_{v_2} = -g_{m_7}\left(r_{ds_7} \parallel r_{ds_6}\right)$$

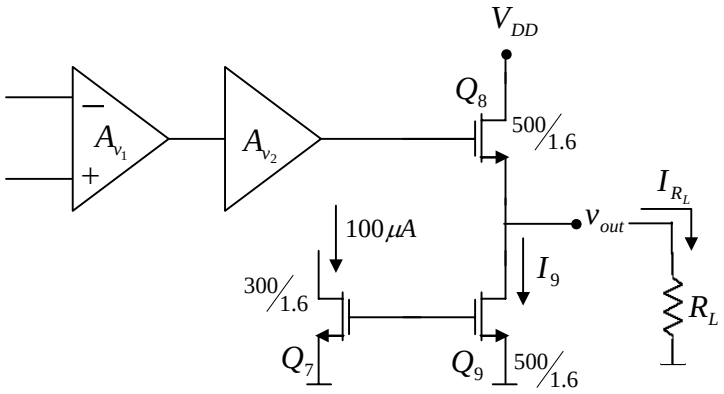
$$I_6 = \frac{W_6}{W_{11}} \times I_{11} = \frac{300}{25} \times 8.3\mu A = 100\mu A = I_{D_7}$$

$$g_{m_7} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_7 . I_7} = \sqrt{2 \times 100 \times 10^{-6} \times \frac{300}{1.6} \times 100 \times 10^{-6}} = 1.9\, mA/v$$

$$r_{ds_7} = r_{ds_6} = \frac{1}{\lambda \times I_{D_7}} = 200K\Omega$$

$$\rightarrow \quad A_{v_2} = -1.9 \times (200 \parallel 200) = -193$$

Source-follower



$$I_9 = \frac{W_9}{W_7} \times I_7 = \frac{500}{300} \times 100 = 167\mu A = I_8$$

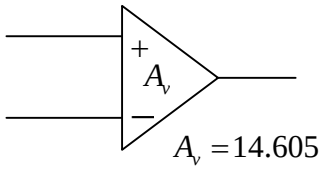
$$\rightarrow \quad g_{m_8} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_8 I_{D_8}} = 3.23\, mA/v$$

$$R_L = 10K\Omega$$

$$g_s = \frac{g_m \gamma}{2\sqrt{V_{SB} + 2\Phi_f}}$$

$$A_{v_3} \approx \frac{g_{m_8}}{1/R_L + g_{m_8} + g_{s_8} + 1/r_{ds_8} + 1/r_{ds_9}} \approx \frac{3.23}{1 + 3.23} = 0.97$$

$$A_v = A_{v_1} \times A_{v_2} \times A_{v_3} = 78 \times (-193) \times 0.97 = 14.605$$



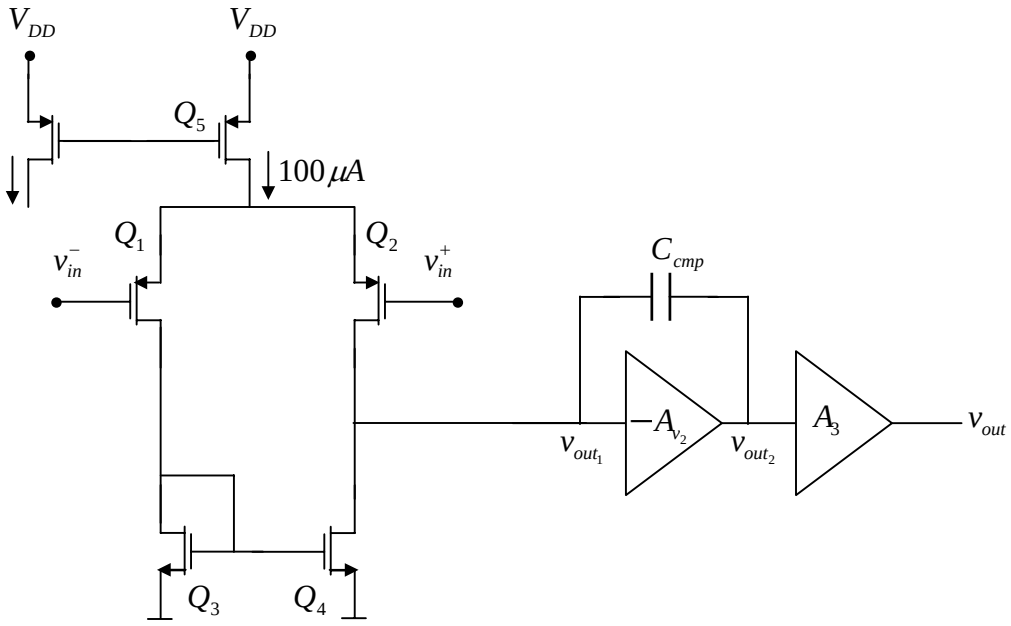
What other parameter are important:

* Frequency response
* Slew-rate
* Systematic offset voltage
* Output impedance

Frequency response

Is usually dominated by the compensation capacitor. We will take advantage of miller effect in calculating the frequency response:

For this calculation we ignore the NMOS transistor biased in triode that provides the lead compensation.



Since A_{v_2} is negative high gain, C_{cmp} can be represented by its miller equivalent:

$$C_{miller} = C_{cmp}(1 + A_{v_2}) \approx A_{v_2} C_{cmp}$$

At high frequencies the gain of the first stage is:

$$A_{v_1}(f) = \frac{v_{out_1}}{v_{in}} = -g_{m_1}.Z_{out_1}$$

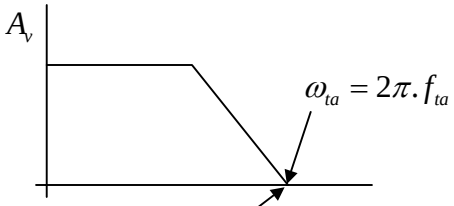
Where $Z_{out_1} = r_{ds_2} \parallel r_{ds_4} \parallel \frac{1}{j\omega C_{Miller}} \overset{\text{at high enough frequencies}}{\approx} \frac{1}{j\omega C_{Miller}}$

Overall gain:

$$A_v(f) = \frac{v_{out}}{v_{in}} = A_{v_3}.A_{v_2}.A_{v_1} = A_{v_3}.A_{v_2}.A_{v_1}(f) = A_{v_3}.\cancel{A_{v_2}} \left| \frac{g_{m_1}}{\cancel{A_{v_2}} \times j\omega C_{cmp}} \right|$$

≈ 1

$$A_v(f) = \frac{g_{m_1}}{\omega C_{cmp}}$$



Unity gain frequency is when $|A_v(f)| = 1$

$25MHz$

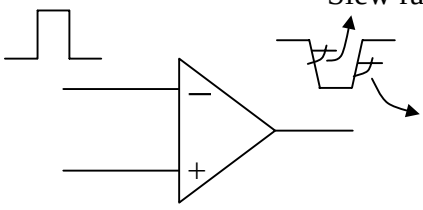
$$\boxed{\omega_{ta} = \frac{g_{m_1}}{C_{cmp}}} = \frac{0.78\times10^{-3}}{5\times10^{-12}} \rightarrow \boxed{f_{ta} = \frac{\omega_{ta}}{2\pi} \approx 25MHz}$$

$assume \quad 5pF$

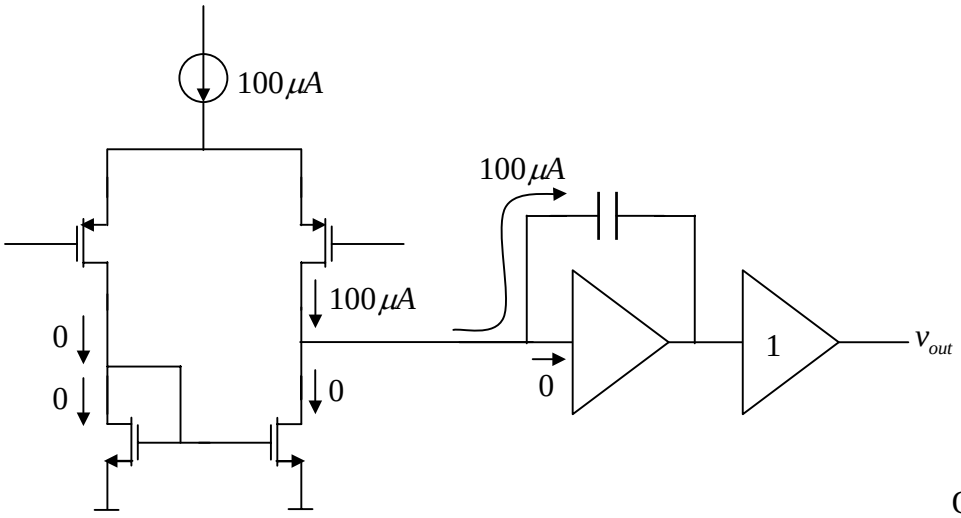
Slew Rate

Shows how the output of amplifier changes in response to large signal.

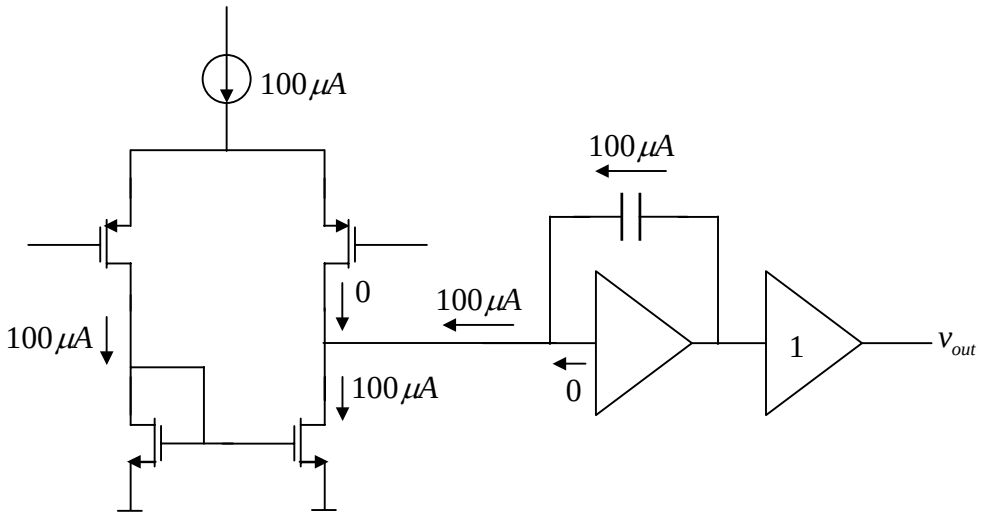
Slew rate = rate of change of output voltage



In this case only one branch of differential amplifier has current ($100\mu A$) and the other one is off.



Or

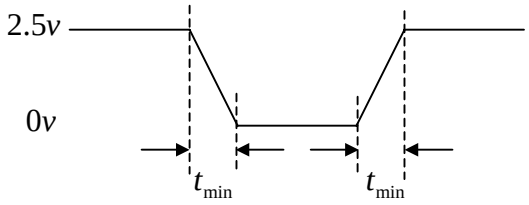


So in both cases, the capacitor C_{cmp} is either charged or discharged with a maximum current of $100\mu A$.

$$\Rightarrow \quad SR = \left.\frac{dv_{out}}{dt}\right|_{\max} = \frac{I_{C_{cmp}}|_{\max}}{C_{cmp}} = \frac{100\mu A}{5pF} = 20 V/\mu\sec$$

If the bias is $0 \rightarrow 2.5 \quad \Rightarrow$

$$t_{\min} = \frac{2.5}{20} = 125 \ n\sec$$



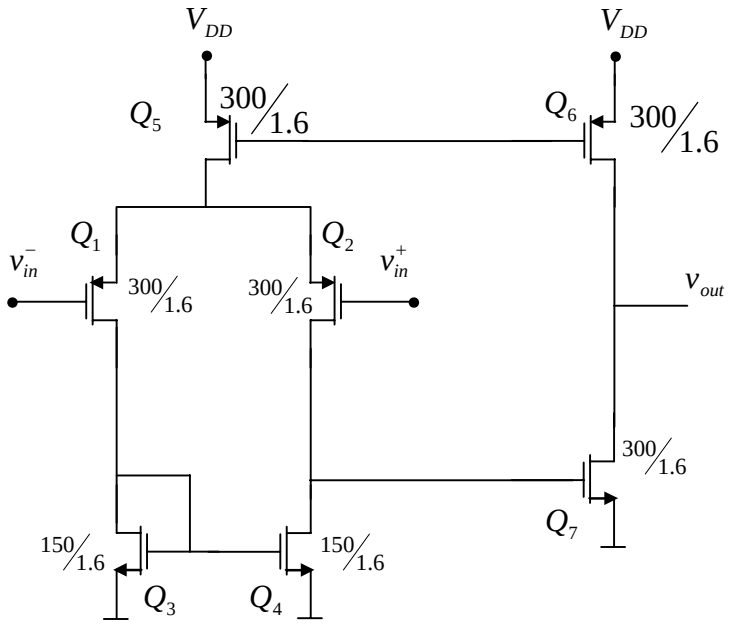
Systematic Offset Voltage

When $v_{in}^{+} = v_{in}^{-}$ then the output voltage v_{out} has to be zero volts. If it is not, there are two reasons:

1- Mistake in sizing the transistors of the two stages.

2- Mistake between the two transistors in the buffer stage.

Consider the first two stages:



If $v_{in}^- = v_{in}^+$ because of symmetry in the differential amplifier:

$$\left.\begin{aligned} &V_{DS_3} = V_{DS_4} = V_{GS_4} \\ &\textit{but} \quad V_{DS_4} = V_{GS_7} \end{aligned}\right\} \rightarrow \; V_{GS_4} = V_{GS_7}$$

$$-V_{tn} \qquad -V_{tn}$$

Assuming identical threshold voltages

$$\left.\begin{aligned} V_{GS_4} - V_{tn} &= \sqrt{\frac{2I_{D_4}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_4}} \\ V_{GS_7} - V_{tn} &= \sqrt{\frac{2I_{D_7}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_4}} \end{aligned}\right\} \Rightarrow \; \frac{I_{D_4}}{\left(\frac{W}{L}\right)_4} = \frac{I_{D_7}}{\left(\frac{W}{L}\right)_7}$$

To have $V_{out_2} = \dfrac{V_{DD} + Gnd}{2} = \dfrac{V_{DD}}{2} \;\Rightarrow\; I_{D_6} = I_{D_7} = 100\mu A$

$I_{D_6} = I_{D_5} = 2I_{D_4} \Rightarrow I_{D_7} = 2I_{D_4} = 100\mu A$

$\Rightarrow \left(\frac{W}{L}\right)_4 = \frac{1}{2}\left(\frac{W}{L}\right)_7$ which is what has been done in general to have 0V systematic offset voltage.

$\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5}$ because $\frac{1}{2}$ current of transistor #5 goes to transistor #4.

Input/Output resistances

$R_{in} = \infty$: Since we are using MOSFET.

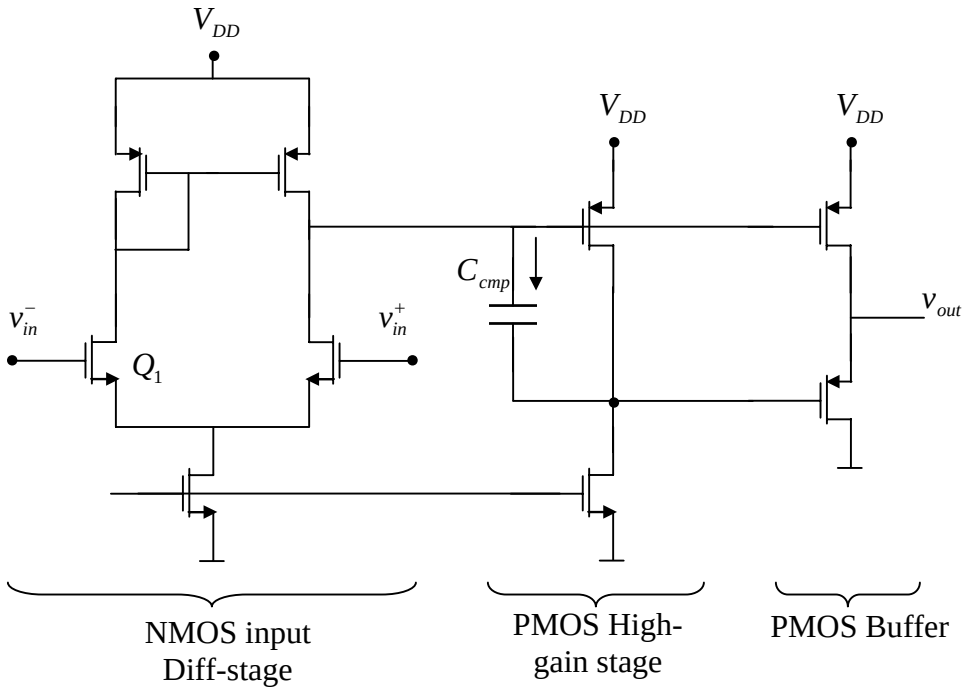
$R_{out} = \frac{1}{g_{m_8}} \| r_{ds_9} \approx \frac{1}{g_{m_8}} = \frac{1}{3.23} K\Omega \cong 310\Omega$

Note that: when you put feedback on the OPAMP you actually reduce R_{out} to $\frac{R_{out}}{1 + fA} \approx 0$.

feedback *Opamp gain*

N-channel or P-channel input stage

Same amplifier can be designed with NMOS input stage. The gain part will look like the following:



We calculated the slew-rate for this type of OPAMP:

$$SR = \left.\frac{dv_{out}}{dt}\right|_{\max} = \frac{I_{C_{cmp}}|_{\max}}{C_{cmp}} = \frac{2I_{D_1}}{C_{cmp}} = \frac{2I_{D_1}\omega_{ta}}{g_{m_1}} \quad (1)$$

$$C_{cmp} = \frac{g_{m_1}}{\omega_{ta}} \longrightarrow \text{unity gain frequency}$$

μ_n if done with NMOS input

$$\left.\begin{aligned} g_{m_1} &= \frac{\mu_p C_{ox} W}{L}\left(V_{GS_1} - V_{tn}\right) \\ I_{D_1} &= \frac{\mu_p C_{ox} W}{2L}\left(V_{GS_1} - V_{tn}\right)^2 \end{aligned}\right\} \rightarrow \frac{2I_{D_1}}{g_{m_1}} = \left(V_{GS_1} - V_{tn}\right)$$

$$(1) : SR = \sqrt{\frac{2I_{D_1}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1}}.\omega_{ta} = \left(V_{GS_1} - V_{tn}\right)\omega_{ta}$$

or μ_n

For the same power consumption, since $\mu_p < \mu_n$ ($\mu_p \approx \frac{1}{3}\mu_n$) P-channel input has a factor of $\sqrt{3}$ higher slew-rate.

If first stage is PMOS → 2nd stage is NMOS

The dominant pole of the opamp without compensation is set by 2nd-stage. Higher transconductance of second stage means higher BW for the opamp without compensation. That means smaller C_{cmp} can be chosen, therefore increasing the unity gain frequency of the opamp.

→ P-channel input stage → higher BW → lower C_{cmp} → higher unity gain frequency.

If first stage is PMOS → third stage (buffer) is NMOS

NMOS buffers are better than PMOS, since they have less voltage drop (higher g_m)

→ P-channel input → higher g_m for buffer transistor → less voltage drop at the buffer stage.

$$A_{v_3} = \frac{g_m}{\frac{1}{R_L} + g_m}$$

Noise consideration

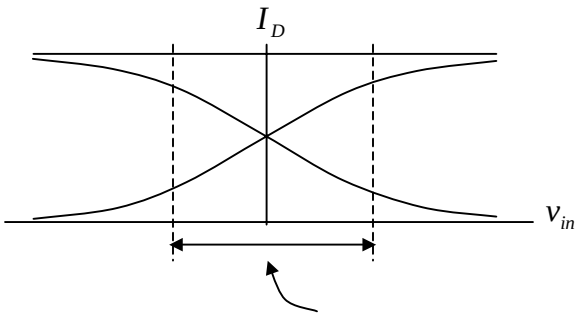
$1/f$ noise: PMOS input is better since PMOS transistor has less $1/f$ noise compared to NMOS.

Thermal noise: NMOS input is better since large transconductance (g_m) of the first stage minimizes the equivalent noise at the input.

To suppress thermal noise, one can use a folded cascode.

Linearity

PMOS input is better (lower distortion) due to higher $(V_{GS} - V_{tn})$.



Higher $(V_{GS} - V_{tn})$ by using PMOS increases the linear region of

P-channel input:

- Higher SR
- Higher unity gain frequency
- Larger $1/f$ noise
- Better linearity
- Worse thermal noise →

use folded cascode if this is an important consideration

Feedback and OPAMP compensation

OPAMPs are usually designed to have one dominant pole.