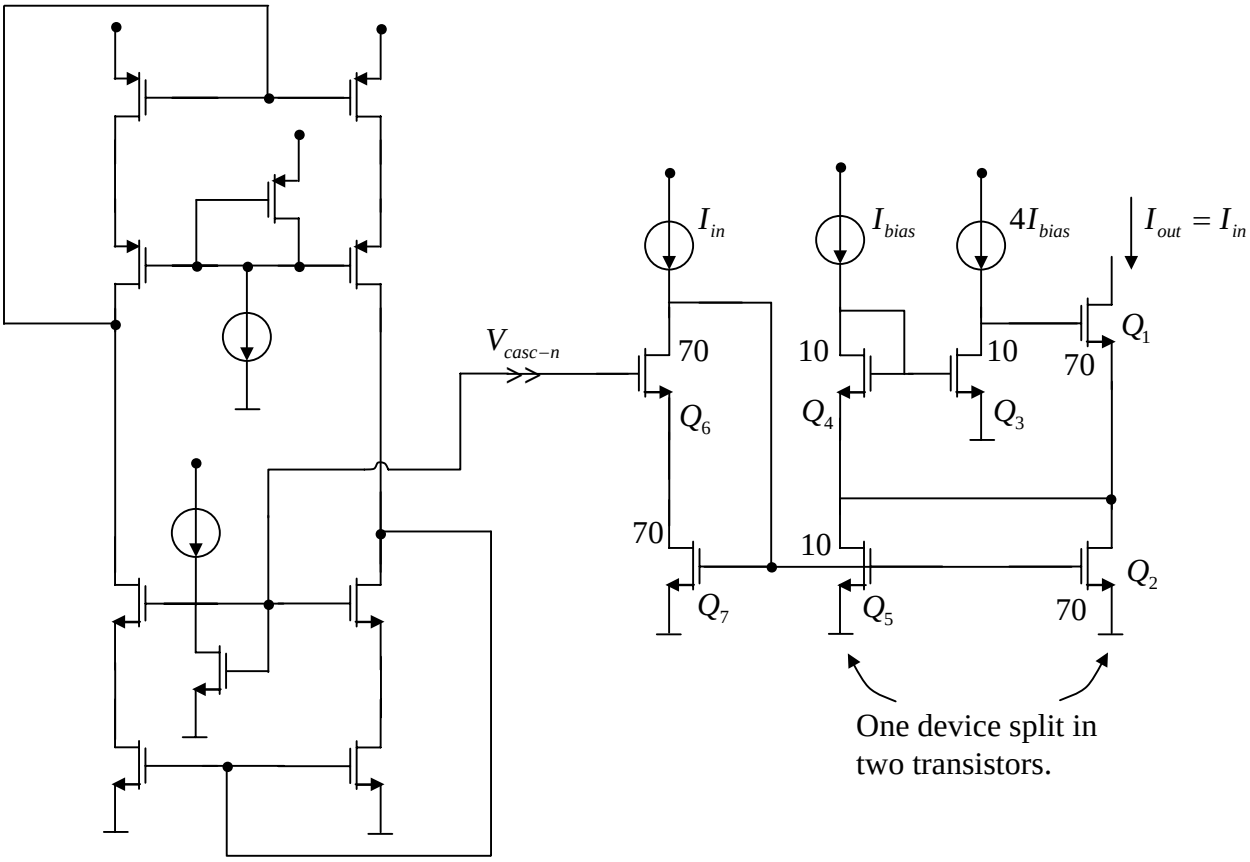
Modified version of wide-swing high-Z current mirror

Advantages compared to previous circuit:

Has smaller dissipated power ($\frac{1}{2}$ of the one + dissipation Of cascode stage)

And smaller area, and also more stable!



Folded cascode OPAMP

Modern OPAMPs are designed to drive capacitive loads

$\Rightarrow$ No need to have low output impedance

$\Rightarrow$ No need for last stage buffers

$\Rightarrow$ Can design higher speeds and larger signal swings.

All nodes are low-impedance except output node that is connected to a load capacitor

In the order of 1/transistor transconductance

$\Rightarrow$ Low impedance also helps reducing the voltage swing. So all nodes are under low voltage swing except for the output.

$\Rightarrow$ Compensation is done by using load capacitance:

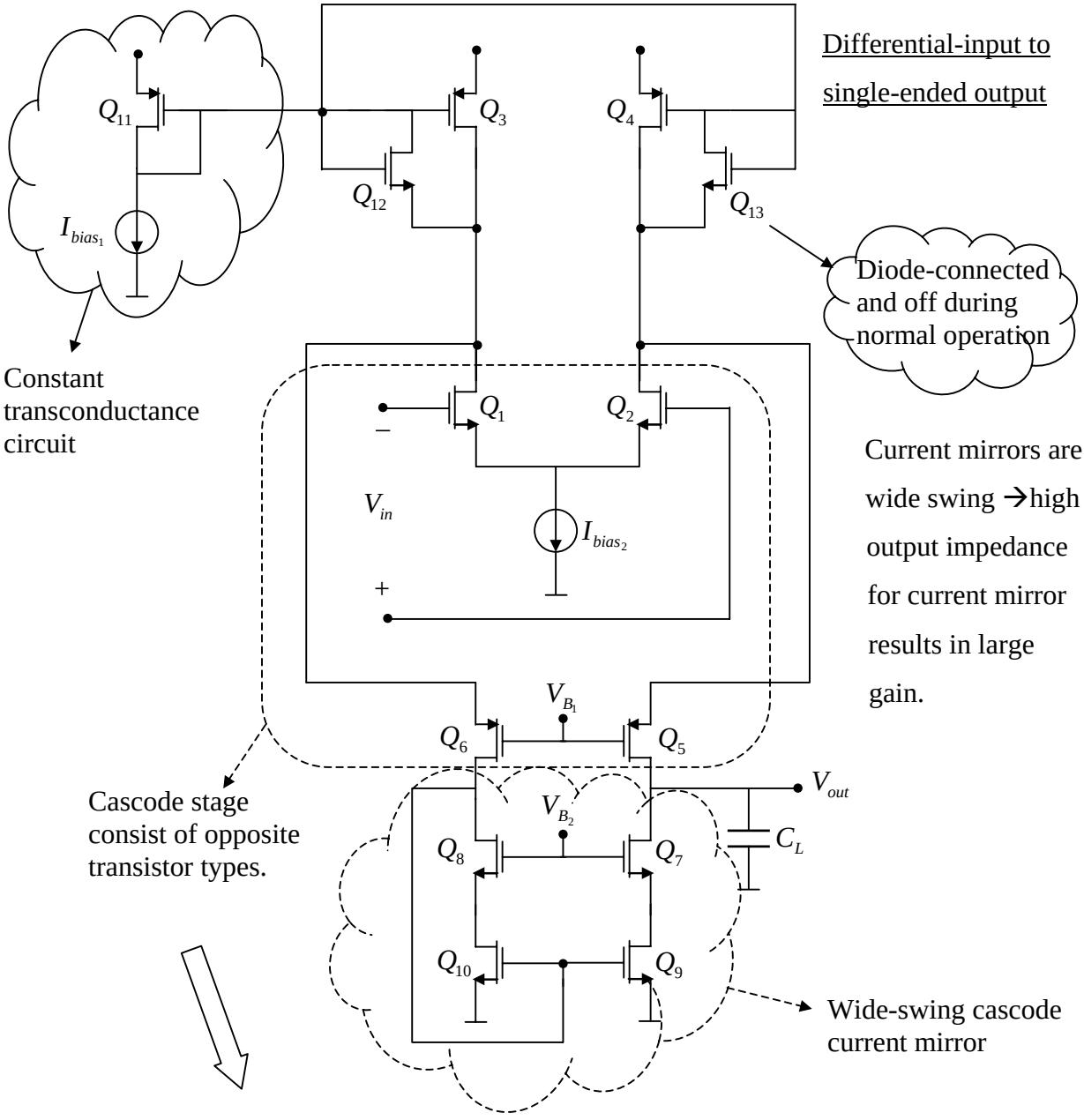
$$\text{more } C_L \Rightarrow \text{ more stable } \Rightarrow \text{ slower}$$

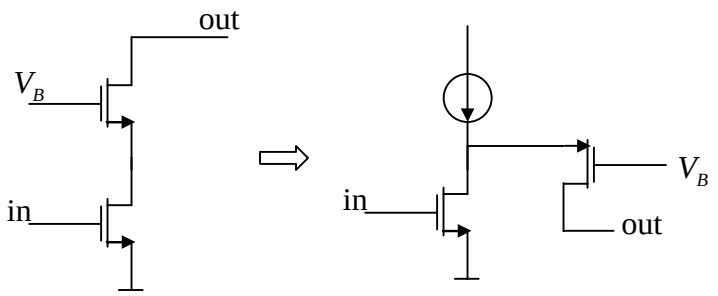
Instead of voltage gain, transconductance gain becomes important:

$$\left(\frac{i_{out}}{V_{in}}\right) \Rightarrow OTA \text{ (Operational Transconductance Amplifier)}$$

Folded cascade is an example of high output impedance OTAs.

Amplifier is actually just a single stage cascade Amp.





⇒ For differential output stage we need to use 2 of these wide swing current mirror stages.

I_{Bias_1} is a constant transconductance biasing circuit and V_{B_1} *and* V_{B_2} are connected to V_{casc-p} and V_{casc-n} respectively.

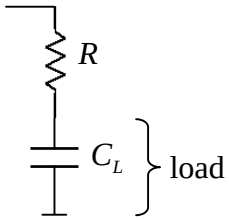
Q_{12} *and* Q_{13} serve two purposes:

1. Increase the slew-rate
2. During slew-rate limiting signal, these transistors prevent drain voltage of Q_1 and Q_2 to negative power supply.

- C_L will be the dominant pole

For small C_L one has to add capacitor to the load to achieve stability.

- For lead compensation



Current in Q_1 and $Q_2 \Rightarrow \frac{I_{Bias_2}}{2}$

Current in Q_5 *and* $Q_6 \Rightarrow I_{Bias_1} \times \frac{(W/L)_3}{(W/L)_{11}} - I_{Bias_2}/2$

For exact and accurate operation I_{Bias_1} *and* I_{Bias_e} are generated from the same source.

Small signal analysis

$$\left.\begin{aligned} A_v &= \frac{V_{out}(\omega)}{V_{in}(\omega)} = g_{m_1}.Z_L(\omega) \\ Z_L &= \frac{r_{out}}{1+ j\omega r_{out} C_L} \end{aligned}\right\} \Rightarrow \quad A_v = \frac{g_{m_1} r_{out}}{1+ j\omega r_{out} C_L}$$

$$r_{out} = r_{ds_{7,\ 9}} \parallel r_{ds_{5,\ 2,\ 4}}$$

Cascode current source

Cascode amplifiers

Current source

$$r_{out} \approx \frac{g_m r_{ds}^2}{2} \Rightarrow \boxed{A_v = \frac{g_{m_1}^2 \, r_{ds}^2/2}{1+ \frac{j\omega g_m r_{ds}^2 C_L}{2}}}$$

When load is only a capacitor

Mid band frequencies → ignore 1 in the denominator:

$$\Rightarrow A_v = \frac{g_{m_1}}{j\omega C_L} \quad \Rightarrow \quad \boxed{w_{ta} = \frac{g_{m_1}}{C_L}}$$

Unity gain frequency

$g_{m_1} \uparrow \Rightarrow$ BW $\uparrow$

→ use NMOS with W$\uparrow$

$\Rightarrow$ Large input current $I_{Bias}/2$

Current in cascode transistors $(P-MOS)$ and current mirror $(Q_7 - Q_{10})$ needs to be small to increase r_{out}.

$\Rightarrow$ gain will be maximized

The practical current ratio limit $\frac{I_{D_2}}{I_{D_5}} = 4$

Since the current is derived by subtraction

→ Having high input current I_{D_2} also helps reducing thermal noise → Since most of the bias current flows in the input differential pair, for the same power consumption, folded cascode has lower noise figure.

<u>Gain calculation with lead compensation</u>

$$Z_L = r_{out} \parallel \left(R_c + \frac{1}{j\omega c_L} \right)$$

Load Capacitor

Load Compensation Resistor

Assuming $r_{out} >> Z_L$

$$\boxed{A_v = \frac{g_{m_1}}{\frac{1}{r_{out}} + \frac{1}{R_C + \frac{1}{j\omega C_L}}} \cong \frac{g_{m_1}}{\frac{1}{R_C + j\omega c_L}} = \frac{g_{m_1}(1 + j\omega R_C C_L)}{j\omega C_L}}$$

If R_C is chosen to get a zero at 1.2 times the unity gain frequency, optimum speed and stability is achieved:

$$\text{w}\,\omega_Z = \frac{1}{R_C C_L} = 1.2 \times \omega_{ta} = 1.2 \times \frac{g_{m_1}}{C_L}$$

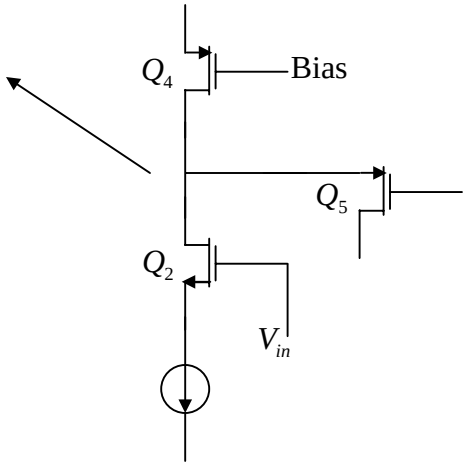
$$\Rightarrow \boxed{R_C = \frac{1}{1.2\ g_{m_1}}}$$

Location of second pole

The second pole is usually due to *RC* time constant at the source of P-channel transistors.

$$R_o = r_{ds_4} \| \sim r_{ds_2} \| \ 1/g_{m_5}$$

$$\Rightarrow R_o = \frac{1}{g_{m_5}}$$



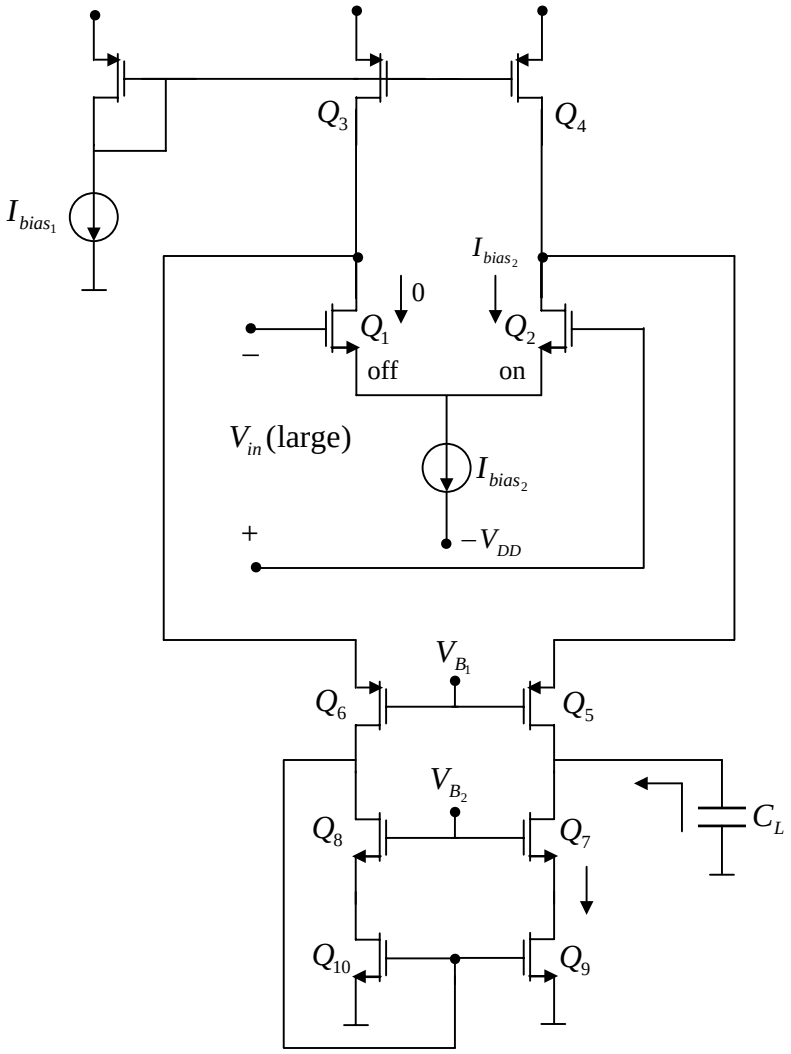
$$C_{2nd\ \ pole} = C_{gs_5} \| C_{ds_2} \| C_{ds_4} \approx C_{gs_5}$$

$$\omega_{2nd\ \ pole} = \omega_{p_2} \approx \frac{g_{m_5}}{C_{gs_5}}$$

To improve the high frequency performance one can increase g_{m_5} (current through PMOS transistors) at the cost of extra power consumption.

Slew Rate

What happens if Q_{12} and Q_{13} are not present during slew-rate limiting operation?



$$\Rightarrow \begin{cases} Q_1 : Off \\ Q_2 : On \end{cases}$$

$$\Rightarrow I_{D_3} = I_{D_6} = I_{D_8} = I_{C_{L_{disch\ arg\ e}}}$$

$$\text{SR} = \frac{I_{D_3}}{C_L}$$

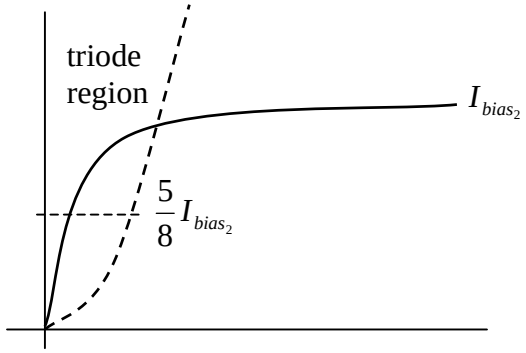
Usually the design is:

$$I_{D_1} = 4 \;\; I_{D_6} = \frac{I_{Bias_2}}{2}$$

$$\Rightarrow \;\; I_{D_3} = I_{D_1} + I_{D_6}$$

$$\Rightarrow I_{D_3} = \frac{I_{Bias_2}}{2} + \frac{I_{Bias_2}}{8} = \frac{5}{8} I_{Bias_2} \qquad \Rightarrow \quad I_{Bias_2} > I_{D_3} = I_{D_4}$$

So when Q_2 is On and need to sink I_{Bias_2} but I_{D_4} cannot give that much current, that pushes both Q_2 and I_{Bias_2} to triode regions → So their current decreases and become $\frac{5}{8} I_{Bias_2}$.



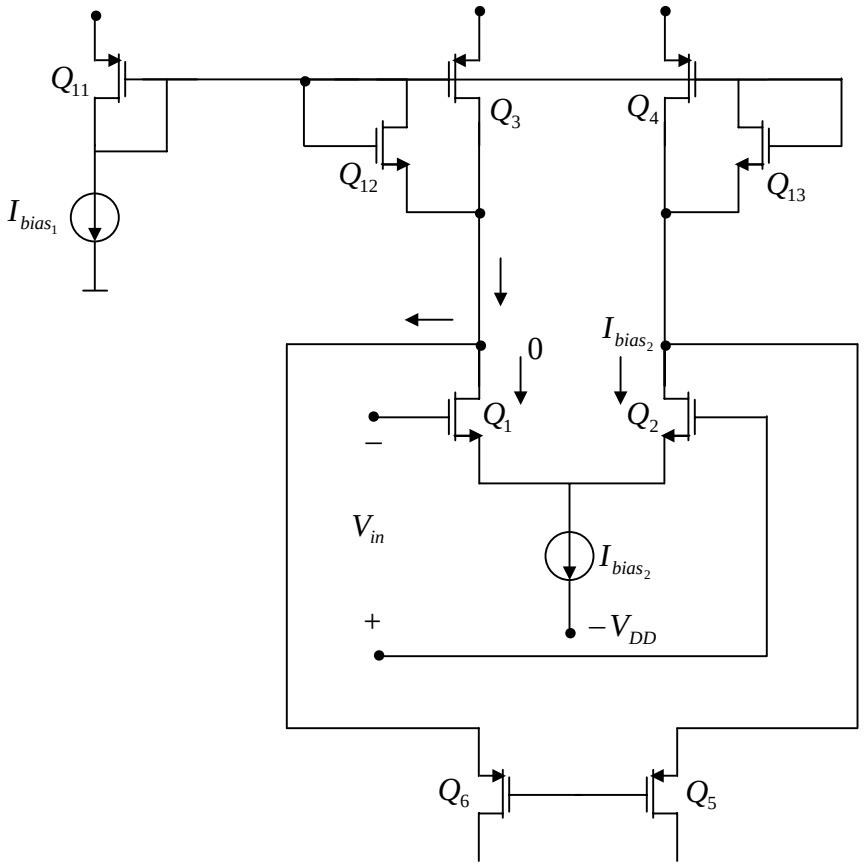
→ Drain of Q_2 approaches $-V_{DD}$

In $+ve$, V_{in} cycle drain of Q_2 needs to come back to $+V_{DD}$ → We have transition from $\sim -V_{DD}$ to $\sim +V_{DD}$

→ Additional time that adds to slew-rate + non-linear operation

→ as you go to triode region.

To solve this problem we add diode-connected transistors Q_{12} and Q_{13}.



Q_{12} and Q_{13} are normally off:

$V_{GS_{12}}$, $V_{GS_{13}} < V_{t_n}$

During slew-rate limiting operation the branch that has $I_{Bias_2}(I_{D_2}) \Rightarrow Q_{13}$ turns ON since the drain voltage of $Q_2 \downarrow$.

The first thing it does is to clamp drain of Q_2 to a $+ve$ voltage → Does not allow it to go $-ve$.

This is done by providing the current difference:

$$I_{Bias_2} - \frac{5}{8} I_{Bias_2} = \frac{3}{8} I_{Bias_2}$$

Partially by Q_{13} and partially by increasing Q_4.

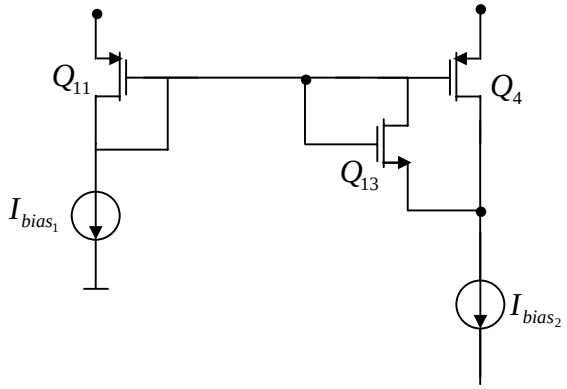
→ No additional slew-rate time is needed

Non-linearity due to transistors entering triode region will not occur.

During slew-rate:

$$\mathrm{I}_{D_2} = I_{Bias_2} = I_{D_{13}} + I_{D_4} \ (1) \Rightarrow \ \ I_{D_{13}} = I_{Bias_2} - I_{D_4}$$

The circuit looks like the following:



$$\left.\begin{aligned} &\frac{I_{D_{11}}}{I_{D_4}} = \frac{\left(W/L\right)_{11}}{\left(W/L\right)_4} \Rightarrow I_{D_{11}} = I_{D_4} \times \frac{\left(W/L\right)_{11}}{\left(W/L\right)_4} \\ &I_{D_{11}} = I_{Bias_1} + I_{D_{13}} \end{aligned}\right\} \quad \Rightarrow \quad I_{D_4} \times \frac{\left(W/L\right)_{11}}{\left(W/L\right)_4} = I_{D_{13}} + I_{Bias_1}$$

$$I_{D_4} \times \frac{\left(W/L\right)_{11}}{\left(W/L\right)_4} = I_{Bias_2} - I_{D_4} + I_{Bias_1}$$

$$\Rightarrow I_{D_4} = \frac{\left(I_{Bias_1} + I_{Bias_2}\right)\left(W/L\right)_4}{\left(W/L\right)_{11} + \left(W/L\right)_4}$$

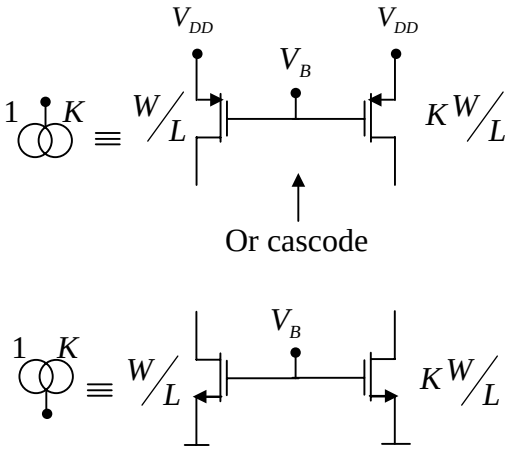
With Q_{12}/Q_{13} : S.R. $= \dfrac{I_{D_4} + I_{D_{13}}}{C_L} = \dfrac{I_{Bias_2}}{C_L}$

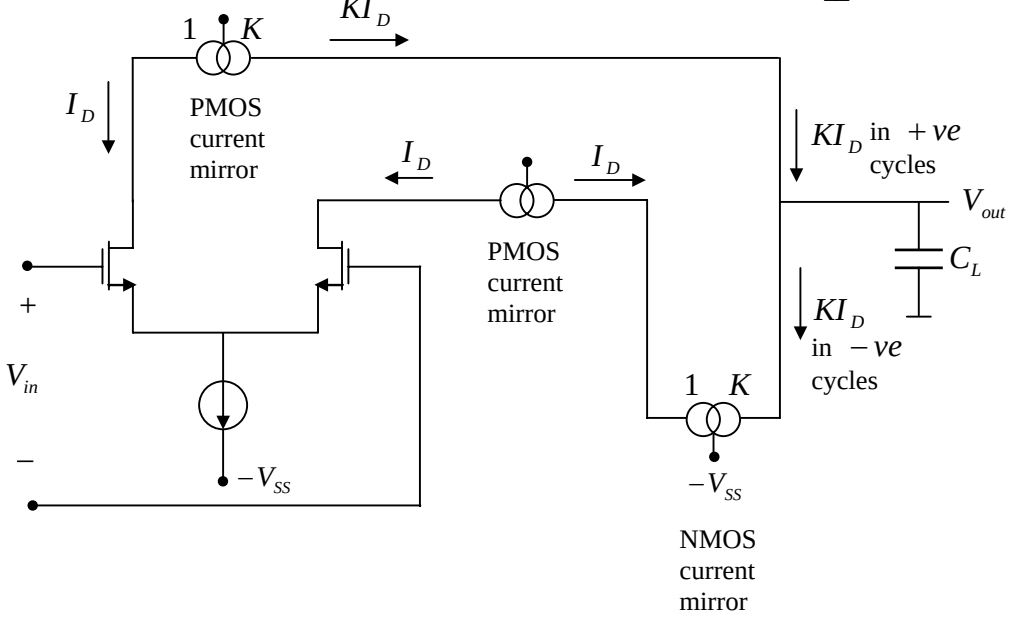
Without Q_{12}/Q_{13} : S.R. $= \dfrac{I_{D_4}}{C_L} = \dfrac{I_{Bias_1}\left(W/L\right)_4}{\left(W/L\right)_{11}}$

<u>Current Mirror OPAMP</u>

- Is used to drive capacitive loads.
- All nodes are low impedance except the output node → Therefore stability can be achieved by putting load capacitor C_L at the output node.

The idea is as following:





$$A_v = \frac{V_{out}}{V_{in}} = Kg_{m_1} Z_L(S) = \frac{Kg_{m_1} r_{out}}{1 + j\omega r_{out} C_L} \approx \frac{Kg_{m_1}}{j\omega C_L}$$

K is transistor W/L ratio of current mirrors

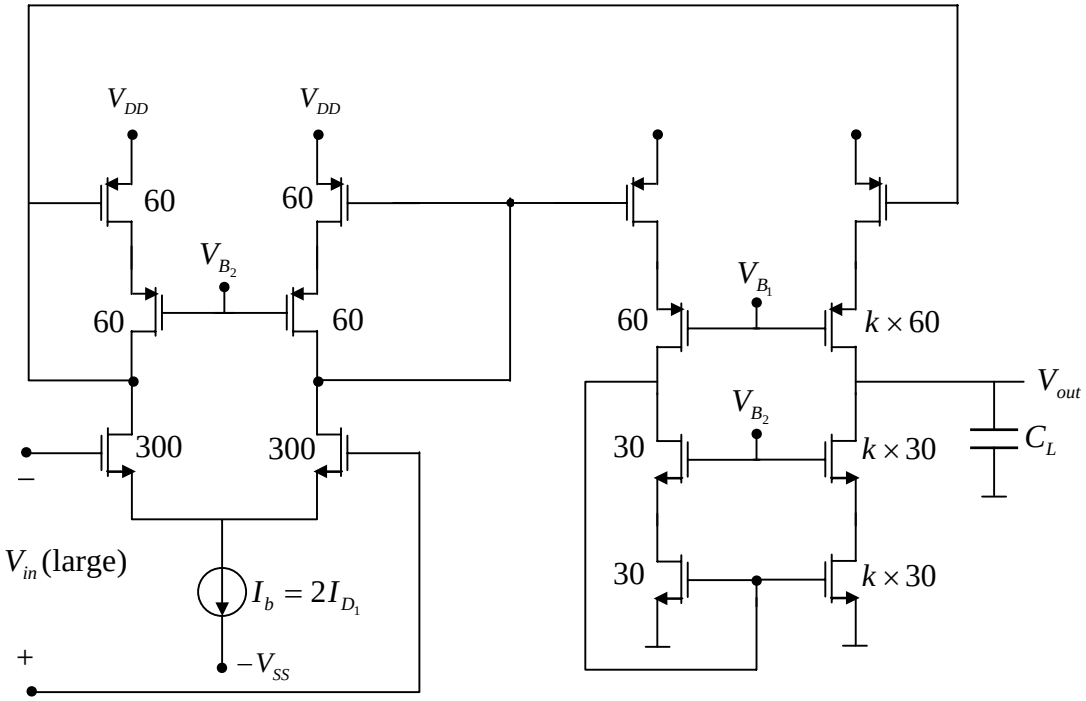
$$\omega_t \Big|_{A_V \to 1} = \frac{Kg_{m_1}}{C_L} = \frac{K\sqrt{2I_{D_1}\mu_n C_{0x}(W/L)_1}}{C_L}$$

Power dissipation:

$$P_{diss} = [V_{DD} - (-V_{SS})]\ I_{total}$$

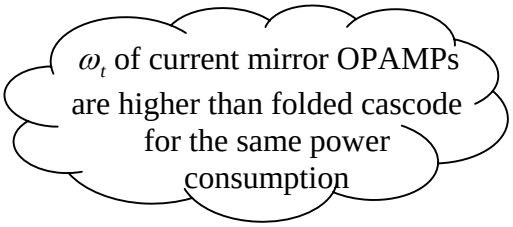
$$I_{total} = (3 + K)\ I_{D_1}$$

Practical implementation



As you increase K

- I_{total} increases so power dissipation increases
- Gain increases
- Unity gain frequency increases →



→ However there is a practical limit as the second pole of the OPAMP becomes problematic if the unity gain frequency increases too much.

→ K Max is typically around 5

$K \sim 2$: Good for general purpose OPAMP

$K = 1$: High speed OPAMP as you can use small C_L and your ω_t is still lower than the second pole.

Slow-Rate

$$SR = \frac{KI_b}{C_L} = \frac{2KI_{D_1}}{C_L}$$

$\Rightarrow$ In terms of S.R. current mirror OPAMPs are better that folded cascodes.