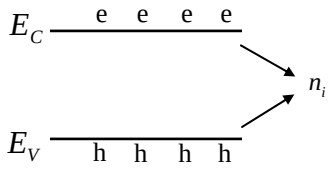
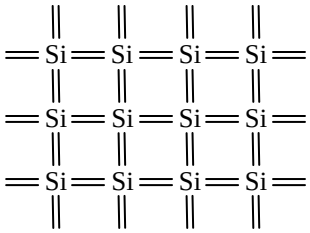
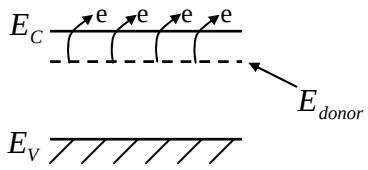
Semiconductors

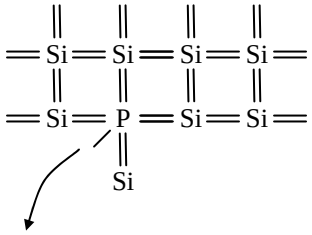
Intrinsic





N-material



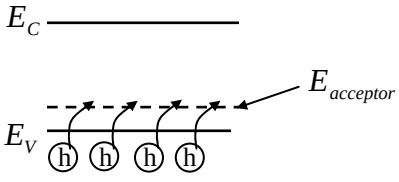


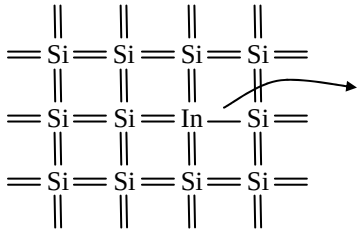
N_D → density of Donor atoms like **P**.

with minimum thermal energy this becomes a free electron

Available free electron (N → negative) → material is still neutral since –ve charged electron cancels positively charged **P** ion.

P-material





with minimum thermal energy an electron can be absorbed to this bond (p → positive) material is still neutral.

N_A → density of acceptor atoms like **In**.

$n = N_D$ ← in an N-material

$p = N_A$ ← in an P-material

Turns out that the density of the other carries goes down i.e. in N-material:

$$\begin{cases} n = N_D \\ p = \dfrac{{n_i}^2}{N_D} \end{cases}$$

n_i → Density of free electrons or holes of an intrinsic semiconductor

In P-material:

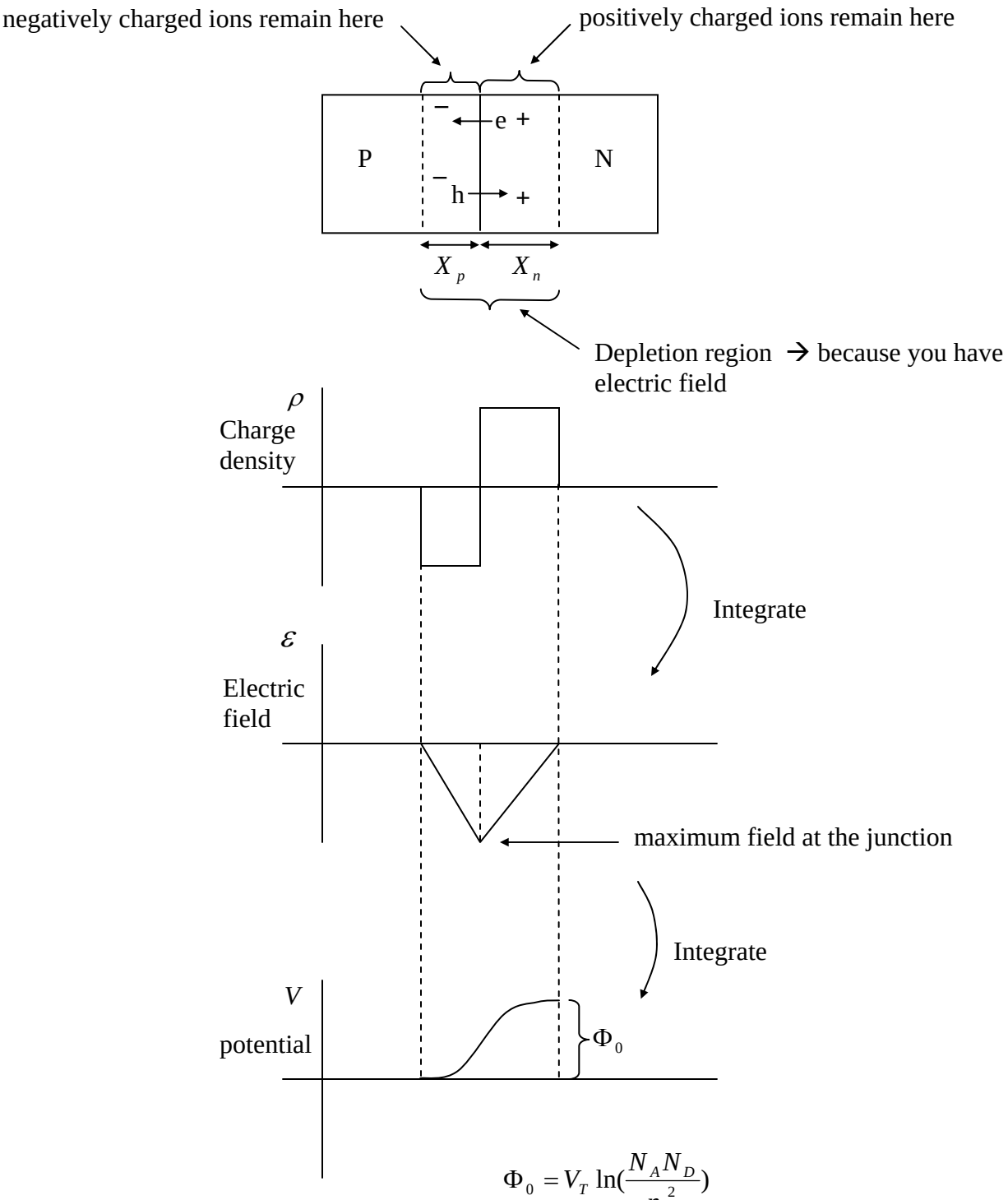
$$\begin{cases} p = N_A \\ n = \dfrac{{n_i}^2}{N_A} \end{cases}$$

n_i = depends on how much thermal energy is available (Temperature dependent)

at 27°C (300K) $n_i\big|_{Si} = 1.5 \times 10^{10} / cm^3$

Diodes

When you bring a P-material and N-material together what happens?



$$\Phi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$V_T = \frac{KT}{q} = 26mV$ at room temperature T =300

$\left.\frac{X_n}{X_p} = \frac{N_A}{N_D}\right\}$ → charge neutralization principle

you can calculate X_n and X_p:

$X_n + X_p$ = depletion region thickness = d

$$C_j = \varepsilon \frac{A}{d} = \varepsilon \frac{A}{X_n + X_p}$$

$$C_j = \sqrt{\frac{q\varepsilon}{2(\Phi_0 - V_{Bias})} \cdot \frac{N_A N_D}{N_A + N_D}}$$

$$\varepsilon = \varepsilon_r \varepsilon_0 = 11.8\varepsilon_0$$

↑ relative permitivity of silicon

V_{Bias} = voltage applied across the diode

Reverse bias $V_{Bias} = -V_R$

Forward bias $V_{Bias} = V_F$

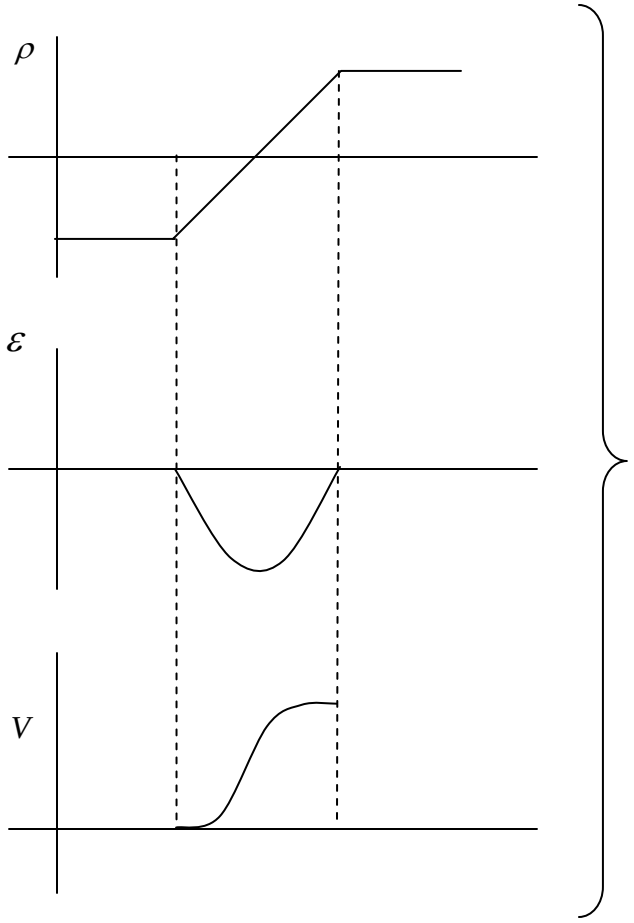
$$\rightarrow C_j = \frac{C_{j0}}{\sqrt{1 - \frac{V_{Bias}}{\Phi_0}}} \quad , \quad C_{j0} = \sqrt{\frac{q\varepsilon}{2\Phi_0} \cdot \frac{N_A N_D}{N_A + N_D}}$$

if one of the N_A or N_D is very high → one sided diode:

$$N_A >> N_D \rightarrow \quad \frac{N_A N_D}{N_A + N_D} = N_D$$

$$C_{j0} = \sqrt{\frac{q\varepsilon}{2\Phi_0} N_D}$$

in case of graded junction electric filed is not triangular. We have to modify equations.



$$\rightarrow \quad C_j = \frac{C_{j0}}{(1-\frac{V_{Bias}}{\Phi_0})^m}$$

$m = \frac{1}{2} \quad \rightarrow$ abrupt junction

$m = \frac{1}{3} \quad \rightarrow$ graded junction

when diode is subjected to large voltages → find average capacitance $C_{j-av} = \frac{\Delta Q}{\Delta V} = \frac{Q(V_2) - Q(V_1)}{V_2 - V_1}$

$$C_{j-av} = 2C_{j0}\Phi_0 \frac{\left(\sqrt{1-\frac{V_{Bias2}}{\Phi_0}} - \sqrt{1-\frac{V_{Bias1}}{\Phi_0}}\right)}{V_{Bias2} - V_{Bias1}}$$

$$\text{if} \quad \left.\begin{array}{l} V_{Bias1} = 0 \\ V_{Bias2} = -5V \\ \Phi_0 = 0.9V \end{array}\right\} \rightarrow \quad C_{j-av} = 0.56C_{j0}$$

In reverse bias: there is no current.

In forward bias: diode has a current:

$$I_D = I_S e^{V_D / V_T}$$

$$I_S \propto A \frac{N_A N_D}{N_A + N_D} \quad , \quad A = area$$

In forward bias there is another capacitor component. Different capacitance due to reaction of moving charges to the applied field (those who contribute to the current)

$$C_d = \tau_T \frac{I_D}{V_T}$$

$\frac{I_D}{V_T}$ → Diode current

$\frac{I_D}{V_T}$ → Thermal voltage

τ_T → Forward transit time

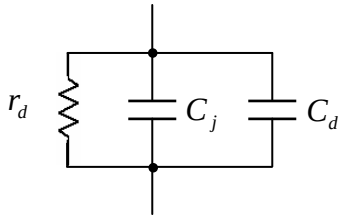
$$C_T = C_d + C_j$$ ← in parallel

Diode model

Forward bias:

$$I_D = I_S e^{V_D / V_T}$$

$$\frac{\partial I_D}{\partial V_D} = \frac{I_S}{V_T} I_S e^{V_D / V_T} = \frac{I_D}{V_T} = \frac{1}{r_d}$$

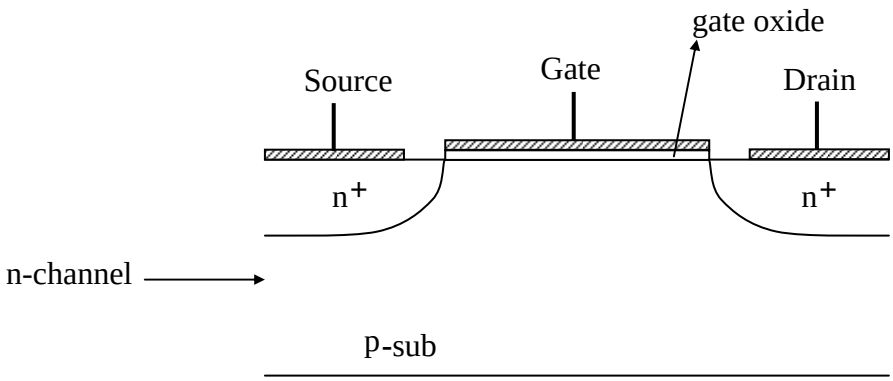


$r_d = \frac{V_T}{I_D}$: diode incremental resistance → this is not a real resistance.

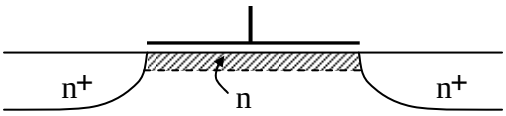
MOS transistors

N-channel → electrons are the conducting charges → faster

P-channel → holes are the conducting charges → slower



Weak inversion → behaves like a resistor



$$I_D = \mu_n C_{ox} \frac{W}{L} \underbrace{(V_{GS} - V_{th})}_{V_{eff}} V_{DS}$$

As you know increase V_{DS} → $$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^{\,2}}{2}\right] \qquad \text{(I)}$$