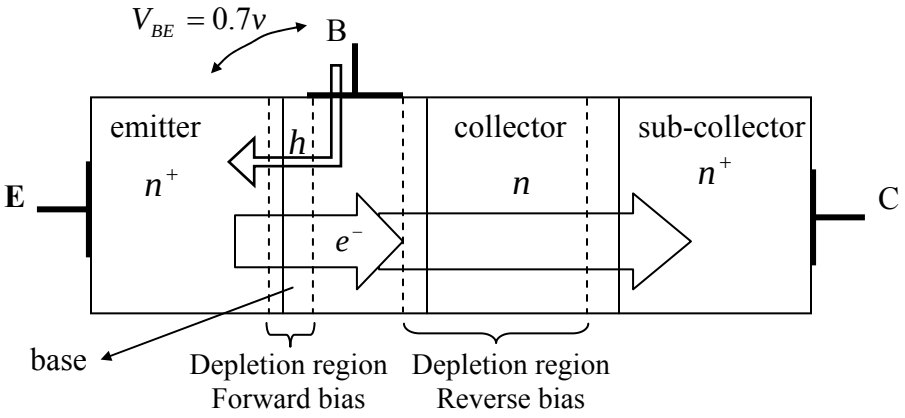
EB junction is forward-biased → e^- are injected to the base.

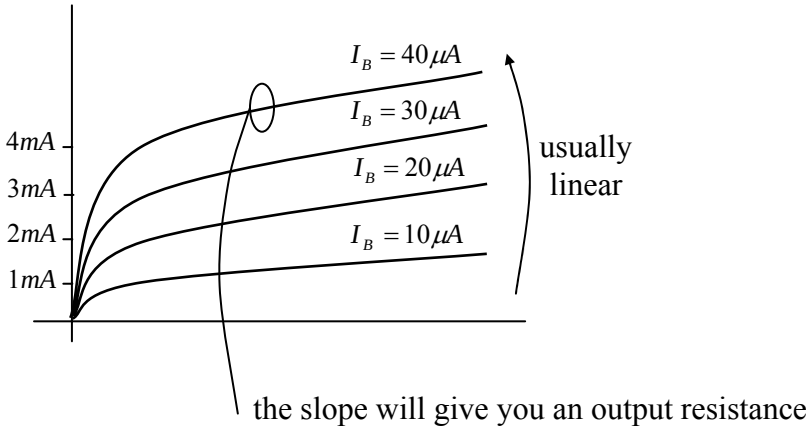
Base is short → so before they recombine with holes in the base they will be swept by electric field of reversed biased BC junction.

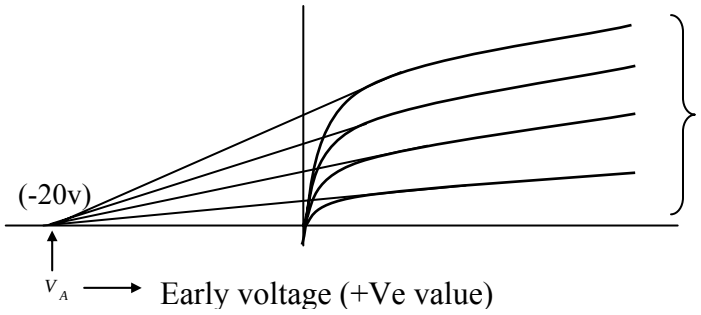


$I_C = \beta I_B$, β : current gain (common emitter)

$I_B = I_{sat}\, e^{V_{BE}/V_T}$, V_T :thermal voltage

$\longrightarrow \quad I_C = I_{CS} e^{V_{BE}/V_T}$





$$I_C = \beta I_B \left(1 + \frac{V_{CE}}{V_A}\right)$$

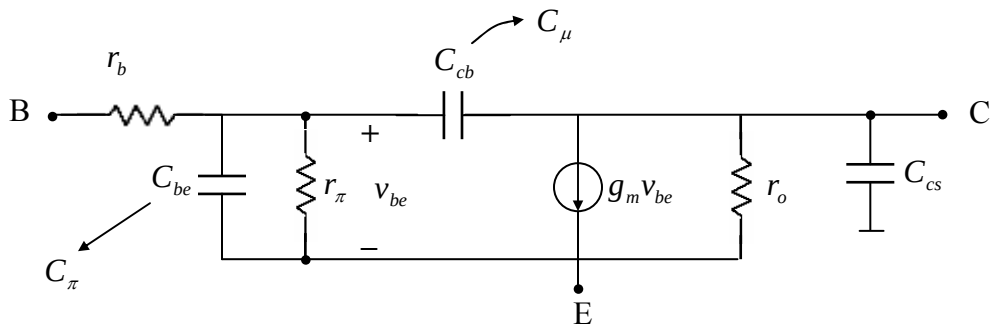
Early effect → similar to channel length modulation, here you base region thickness is modulated by V_{CB} .

$I_C + I_B = I_E \quad \rightarrow \quad I_E = (1+\beta) I_B$

$I_C = \alpha I_E$, α : common base current gain.

$\alpha = \dfrac{\beta}{1+\beta} < 1$

Small-signal model (hybrid-π model)



$$g_m = \frac{\Delta i_c}{\Delta v_{be}} = \frac{\partial (I_{CS} e^{v_{be}/V_T})}{\partial v_{be}} = \frac{I_C}{V_T}$$

$$r_\pi = \frac{\partial V_{BE}}{\partial I_B} = \frac{\beta}{g_m}$$

$$\frac{1}{r_o} = \frac{\partial I_C}{\partial V_{CE}} = \frac{I_C}{V_A} \quad \rightarrow \quad r_o = \frac{V_A}{I_C}$$

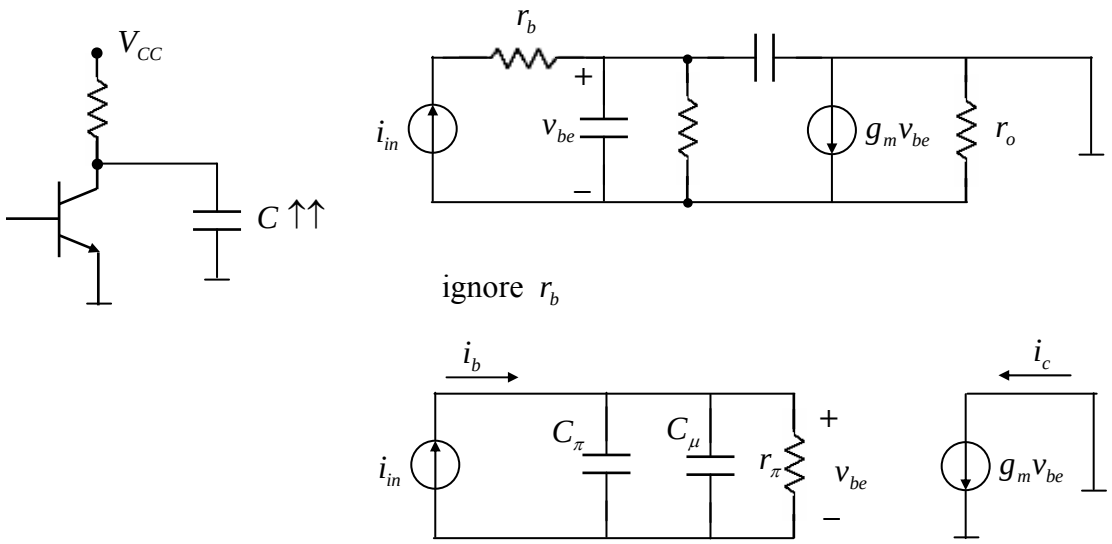
$C_{be} = C_\pi = C_j + C_d$

junction capacitance

diffusion capacitance

$C_{cb} = C_\mu = C_{j_{CB}}$ = reversed bias capacitance → usually graded junction (but not in SiGe transistors)

Calculate short circuit collector current



$$h_{21} = \frac{i_c}{i_b} = \frac{g_m r_\pi}{1 + j\omega(C_\pi + C_\mu) r_D}$$

unity gain frequency is the frequency when $h_{21} \to 1$.

$h_{21} = 1 \rightarrow f_T = \dfrac{g_m}{2\pi(C_\pi + C_\mu)}$ → this is the highest frequency of operation of the transistor.

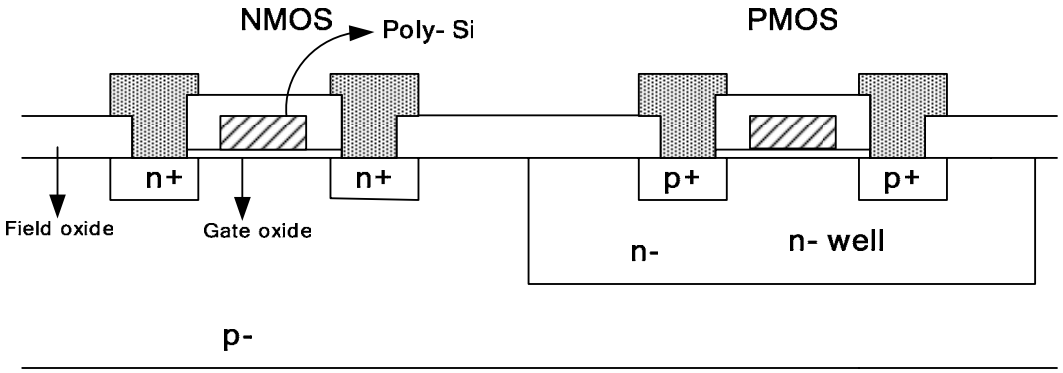
Goal $\begin{cases} g_m \uparrow\uparrow \\ C_\pi,\ C_\mu \downarrow\downarrow \end{cases}$

Read the chapter + Appendix

CMOS Technology

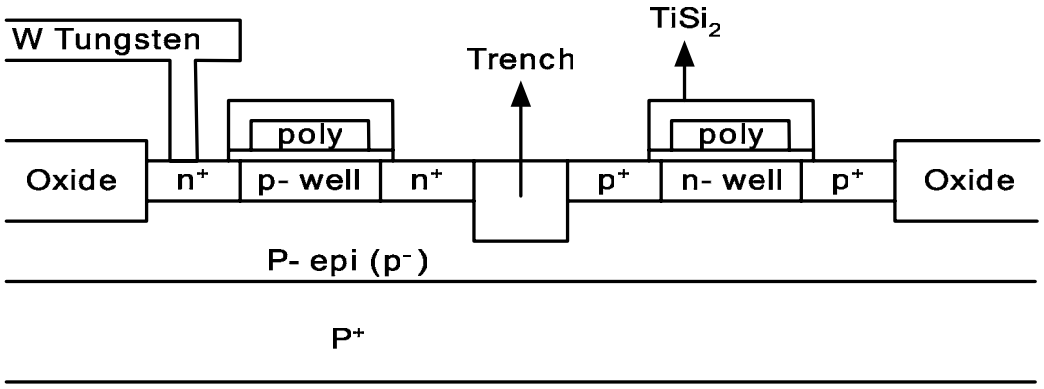
Smaller feature size : density ↑
switching speed ↑ → for the same of dynamic power ↓
V_{DD} ↓ → power decrease
leakage ↑ → static power ↑
cost/cm2 ↓ (cost of mask) 0.13μ $1M/step
cost/transistor ↑
complexity ↑

CMOS Process



n- well CMOS Process

New Processes use epi-layer

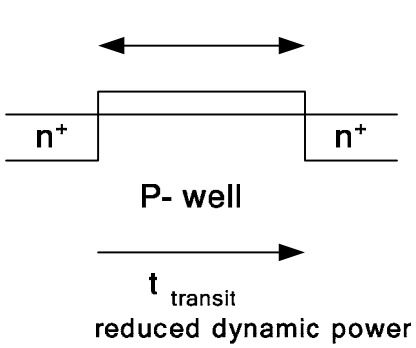


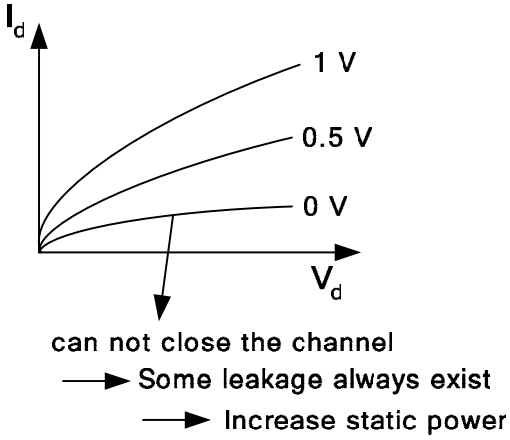
Dual- well epi process

IBM → 90nm trans. SOI substrate → f_T, f_{max} > 200GHz
Silk layer (Dow chemical)
8-level of metallization → 2 of them are Cu (Copper interconnect)
0.6V supply (digital)

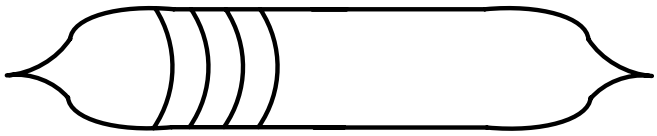
0.9V supply (analog)

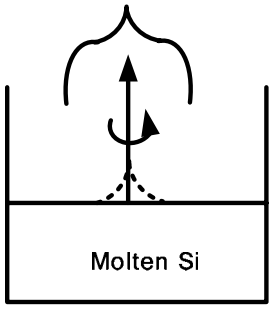
Short channel effects





Si-wafer

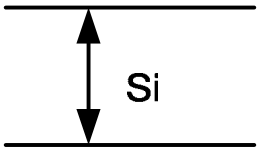




Thickness	Resistivity	Size
2mm(MEMS App.)	P- lightly doped sub. (30-100Ωcm)	4”
1mm	P+ highly doped (1-10 Ωcm)	↓
400μ	high resistivity (10k Ωcm)	12”
	after processing 1kΩcm	

200μ, 100μ, 50μ difficult to handle

Bulk → Bulk CMOS

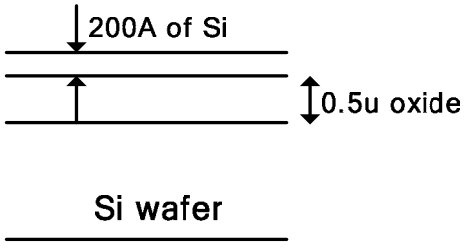


SOI → partially depleted, fully depleted

reduced parasitics → better performance 20% ↑

better on-off characteristics Simox wafers

→ implanting Oxygen in Si wafer

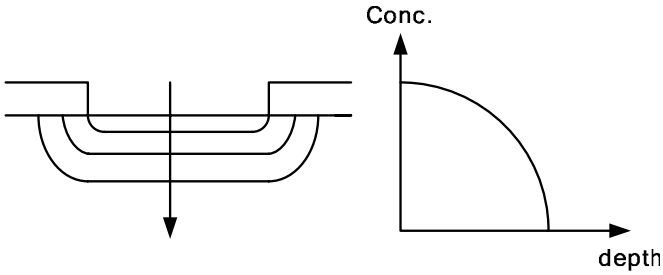


Photolithography

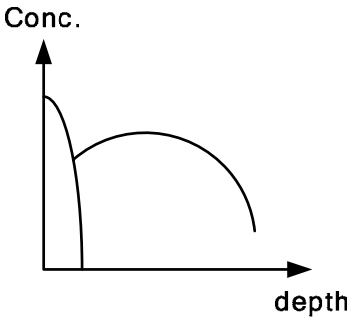
used for selective masking

Diffusion and Ion Implantation

Diffusion



Ion Implantation : Dose, Energy



Deposition

Field oxide, Si_3N_4 sacrificial (mask for ion implantation)

Etching

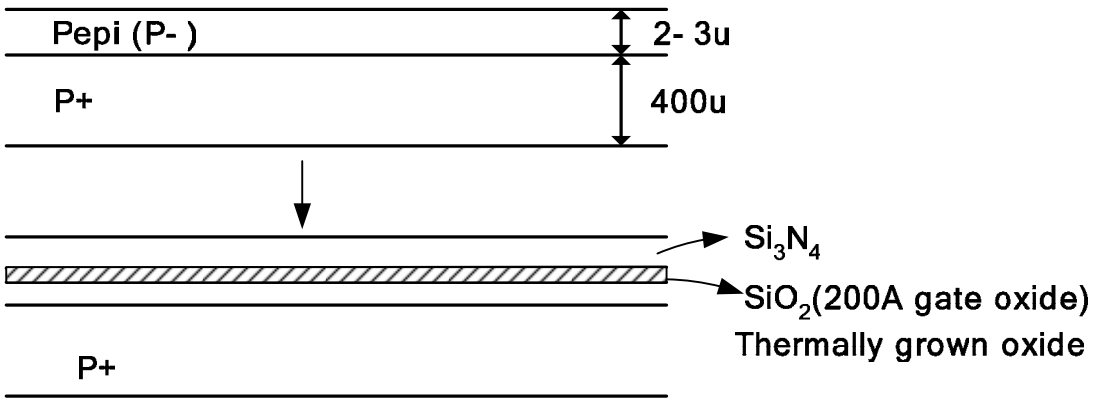
Wet & Dry etching (RIE-Reactive Ion Etching)

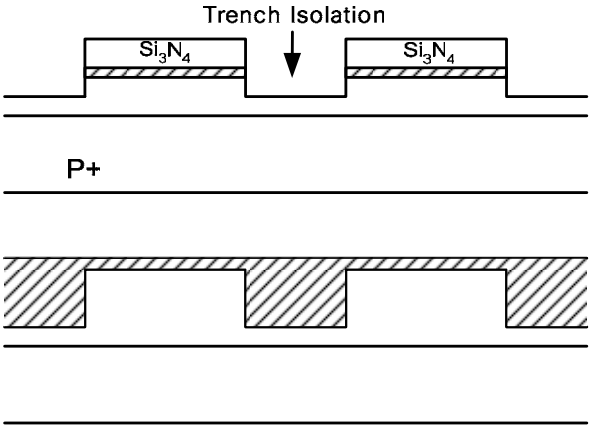
Planarization

For easy masking process

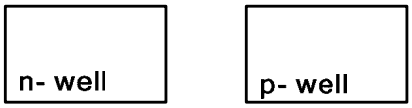
CMOS Process

Design rule (0.25μ) → set of minimum dimensions and spacing to get ~100% yield

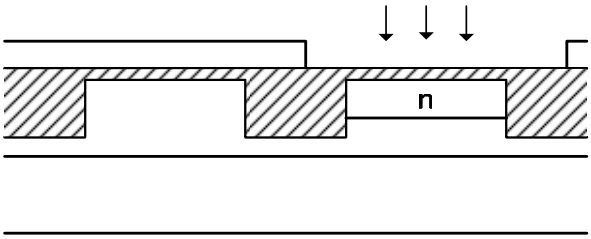




Use active mask

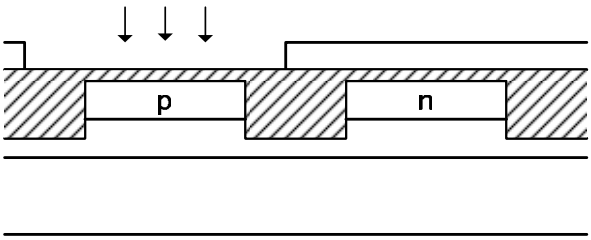


fill trenchs with field oxide(deposited)
+ Planarize

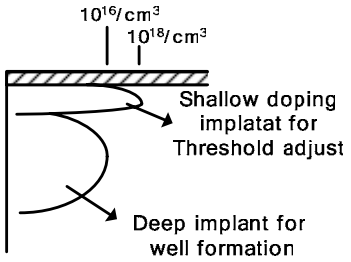


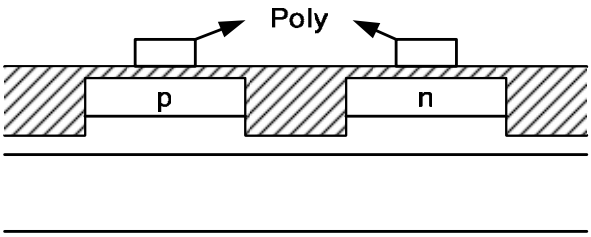
Use same active mask for
n- well and p- well formation

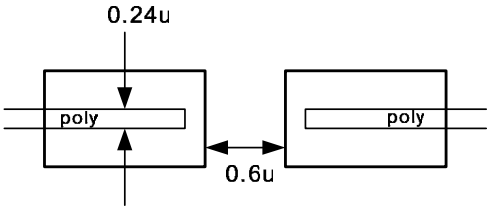
n- well
V_{TP} adjust

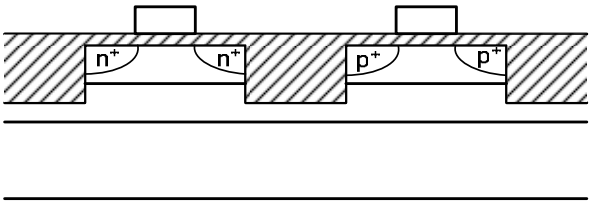


p- well
V_{TN} adjust



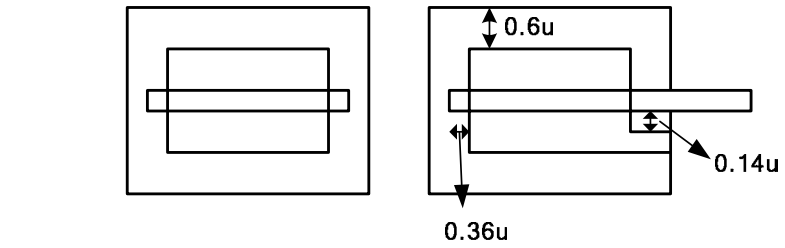


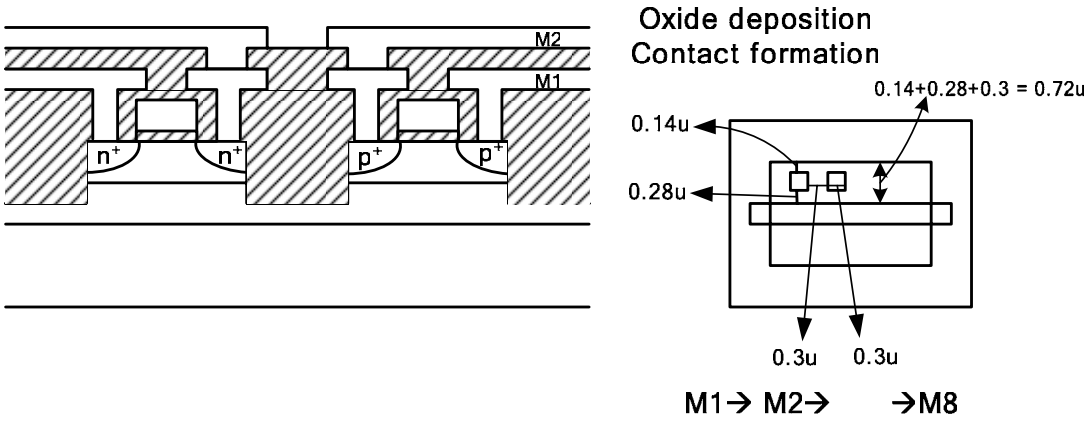




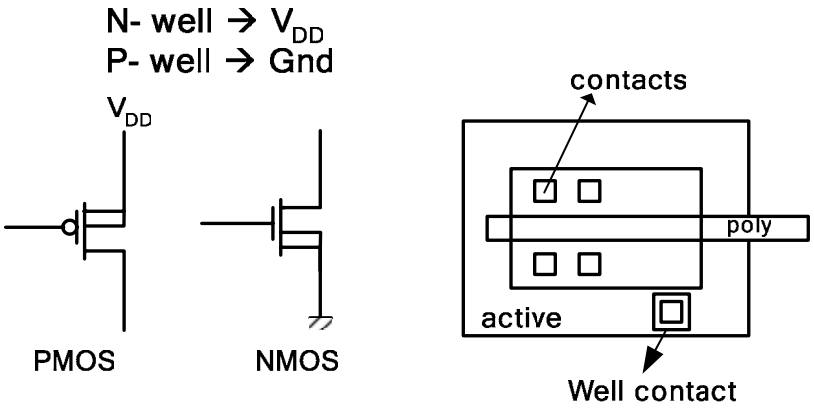
Source/drain implantation
(self- aligned process)

Select layers





⇒ to form a transistor



DRC (Design Rule Check)

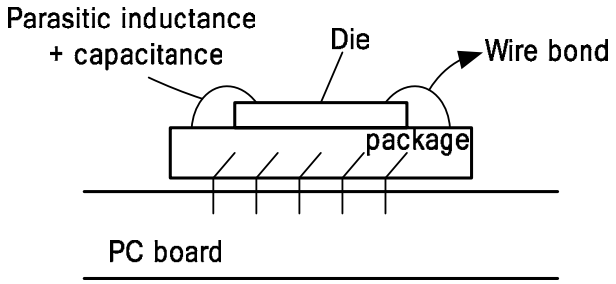
uses a technology file

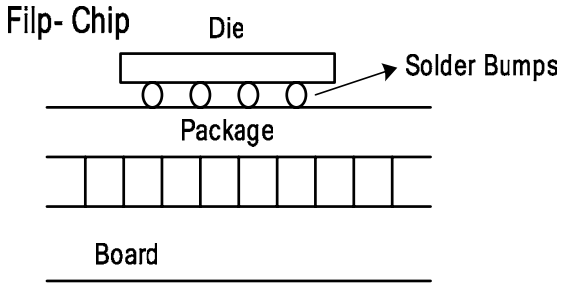
LVS (Layout vs. Schematic)

Extract circuit from layout → calculates parasitics

IC Packaging

Package account for 50% of delay





Different Packages : DIP → Dual-In-Line pakage

PGA → Pin-Grid-Array

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Surface mount → remove package

→ testing is difficult