Parameter Symbol	Parameter Name	Parameter Definition
Timing		
t_{APR}	Asynchronous Preset Recovery Time	The minimum time after the asynchronous preset becomes inactive to the next input clock triggering edge.
t_{APW}	Asynchronous Preset Width	The minimum pulse width required for the asynchronous preset signal.
t_{H}	Hold Time	The minimum time a valid data level is held after clock triggering edge.
t_{HP}	Hold Time for Preload	The minimum delay time for data to remain stable after the preload signal becomes inactive. This only applies to TTL-level preload.
t_{SRR}	Synchronous Reset Recovery Time	The minimum time between the synchronous reset going inactive and the next input clock triggering edge.
t_{S}	Setup Time, Input or Feedback to Clock	The minimum time a valid data level of input or feedback is stable before the next clock triggering edge.
t_{SP}	Data Setup Time for Preload	The minimum time for input data to be stable prior to the preload signal becoming inactive. This only applies to TTL-level preload.
t_{WH}	Clock Width High	The minimum width of the clock high from rising edge to the next falling edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WL}	Clock Width Low	The minimum width of the clock low from falling edge to the next rising edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WP}	Preload Pulse Width	The minimum pulse width required to preload the registers. This only applies to TTL-level preload.
t_{AP}	Asynchronous Preset to Output	The maximum time required to preset the register output after the preset signal is asserted.
t_{AR}	Asynchronous Reset to Output	The maximum time required to reset the register output after the reset signal is asserted.

Parameter Symbol	Parameter Name	Parameter Definition
Timing		
t_{CO}	Clock to Register Output	The maximum time it takes to obtain a valid data level on the output pin after an input clock triggering edge is applied.
t_{CR}	Input or Feedback to Registered Output from Combinatorial Configuration; Output Mux Select 1 to 0	The minimum time from input or feedback to registered output as output mux selection changes from combinatorial to registered output 1 to 0).
t_{EA}	Output Enable Time, Clock to Output	The minimum delay between when an input is asserted and the output switches from a high-impedance state to HIGH or LOW logic state.
t_{ER}	Output Disable Time, Input to Output	The minimum delay between when an input is asserted and the output switches from a HIGH or LOW logic state to a high-impedance state.
t_F	Fall Time	The minimum time for a signal to fall from 80% to 20% of its stabilized high value.
t_{PD}	Propagation Delay, Input or Feedback to Combinatorial Output	The time for a signal to propagate from input or feedback to output.
t_{PR}	Power-up Reset Time	The minimum time for a registered output signal to be reset after the power is applied.
t_{PXZ}	Output Disable Time, $\overline{OE}$ to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a HIGH or LOW logic state to be a high-impedance state.
t_{PZX}	Output Enable Time, $\overline{OE}$ to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a high-impedance state to a HIGH or LOW logic state.
t_R	Rise Time	The minimum time for a signal to rise from 20% to 80% of its stabilized high value.
t_{RC}	Input or Feedback to Combinatorial Output from Registered Configuration; Output Mux Select 0 to 1	The minimum time from input or feedback to combinatorial output mux selection changes from registered to combinatorial output (0 to 1).
Voltage		
V_{CC}	Supply Voltage, Positive Potential	The voltage required across supply and ground terminals of a TTL or CMOS integrated circuit.
V_I	Input Clamp Voltage	The maximum input clamp voltage limit on every input pin.
V_{IH}	High-Level Input Voltage	The minimum high-level input voltage that is guaranteed to represent a high logic level.
V_{IL}	Low-Level Input Voltage	The maximum low-level input voltage that is guaranteed to represent a low logic level.
V_{OH}	High-Level Output Voltage	The minimum high logic level guaranteed for all outputs.
V_{OL}	Low-Level Output Voltage	The minimum low logic level guaranteed for all outputs.

Parameter Symbol	Parameter Name	Parameter Definition
Current		
I_{CC}	Supply Current, Corresponding to V_{CC}	The maximum current into the V_{CC} terminal of a TTL or CMOS integrated circuit.
I_I	Input Current with Maximum Input Voltage	The maximum current into an input pin when the input voltage is applied to the input pin.
I_{IH}	High-Level Input Current	The maximum current into an input pin when a logic-high level is applied to the input pin.
I_{IL}	Low-Level Input Current	The maximum current into an input pin when a logic-low level is applied to the input pin.
I_{OH}	High-Level Output Current	The maximum current into an output pin to guarantee an output logic-high level.
I_{OL}	Low-Level Output Current	The maximum current into an output pin to guarantee an output logic-low level.
I_{SC}	Output Short-Circuit Current	The current into an output when that output is short-circuited to ground (0.5 V).
I_{OZH}	High-Level Leakage Current	The maximum current into a high-impedance state output pin when a high logic level is applied to the output pin.
I_{OZL}	Low-Level Leakage Current	The maximum current into a high-impedance state output pin when a low logic level is applied to the output pin.
Miscellaneous		
C_{IN}	Input Capacitance	The input pin capacitance at a specified voltage and frequency.
C_{OUT}	Output Capacitance	The output or I/O pin capacitance at a specified voltage and frequency.
T_A	Operating Free Air Temperature	The ambient homogeneous temperature of the environment during operation.
T_C	Operating Case Temperature	The maximum chassis temperature during operation.
f_{MAX}	Maximum External Frequency	The $f_{MAX,\ External}$ is the maximum clocking frequency with external feedback. It is the reciprocal of the clock period ($t_S + t_{CO}$).
f_{MAX}	Maximum Internal Frequency	The $f_{MAX,\ Internal}$ is the maximum clocking frequency with internal feedback. An internal counter is used to determine "f_{CNT}."
f_{MAX}	Maximum Frequency without Feedback	The $f_{MAX,\ No\ Feedback}$ is the maximum clocking frequency with no feedback. It is the reciprocal of the sum of the data setup time (t_S) and the data hold time (t_h).