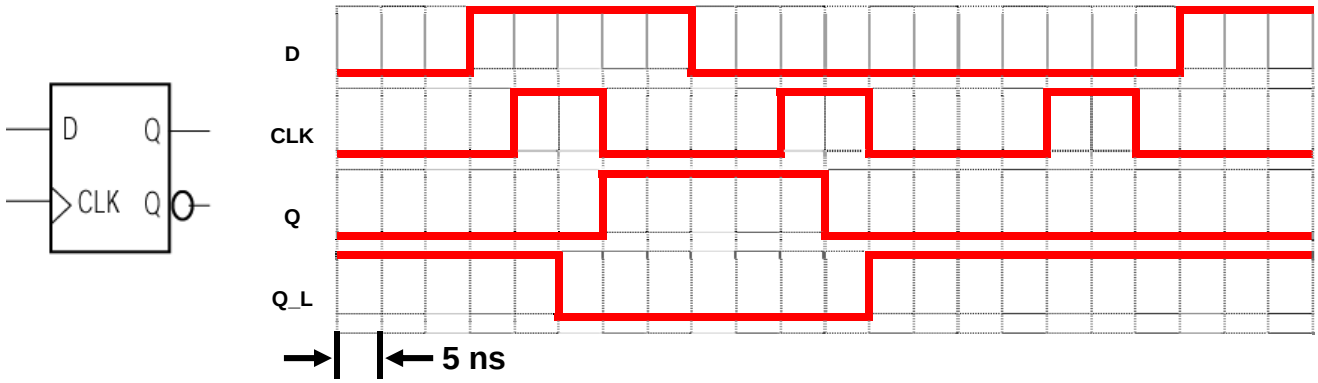
Practice Quiz 9

The following figure applies to questions 1–3:



1. The **nominal setup time** provided for the D flip-flop, based on the excitation signals (D and CLK) depicted in the timing chart, is:

   (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

2. The **nominal hold time** provided for the D flip-flop, based on the excitation signals (D and CLK) depicted in the timing chart, is:

   (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

3. The $t_{PLH(C \rightarrow Q)}$ of the D flip-flop is:

   (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

4. As a contestant on the TV series* ***Digital Dynasty***, you have been asked to "digitally dual" with your BECEFE (*best ECE friend evah*) over the phenomenon of metastability. You confidently explain to the host that the **next state** of an edge-triggered D flip-flop will most likely be **random** if:
   (A) its minimum setup time requirement is not met
   (B) its minimum hold time requirement is not met
   (C) its minimum clock pulse width requirement is not met
   (D) all of the above
   (E) none of the above

5. As a contestant on the hit TV series* ***Are You Smarter than Your BEFFAP?*** (*best engineering friend from another planet*) you have been asked to explain why a **"D" latch** is called **transparent.** Hoping to forgo an admission before a national television audience to the contrary, you calmly answer that a **"D" latch** is called **transparent** because its output:
   (A) is equal to its input when the latch enable is high-impedance
   (B) is equal to its input when the latch enable is asserted
   (C) is equal to its input when the latch enable is negated
   (D) changes state as soon as the latch is clocked
   (E) none of the above

* Yes, the course staff understands that hard-working ECE students do not have time to watch TV