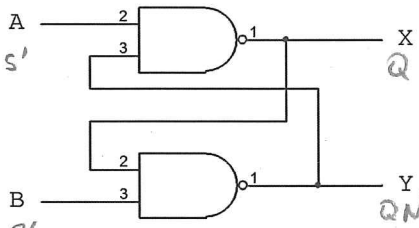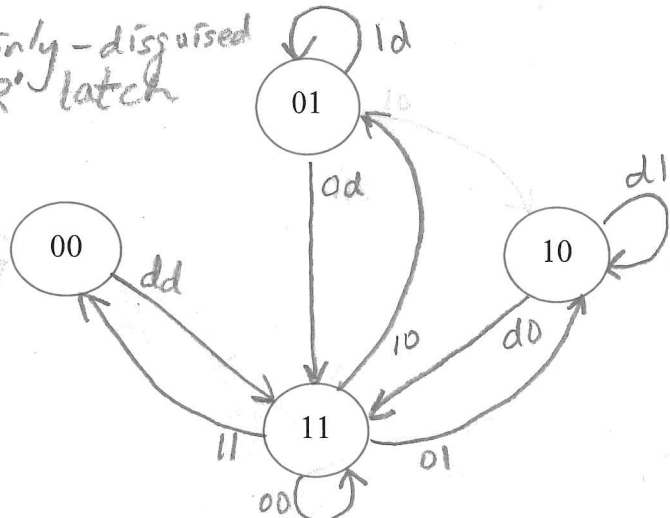# Practice Quiz 8

The following circuit applies to the questions on this quiz. Complete the next state equations, present state – next state table, and state transition diagram to determine the answers.

$$X(t+\tau) = \underline{A'(t) + Y'(t)}$$

$$Y(t+\tau) = \underline{B'(t) + X'(t)}$$

a thinly-disguised s'R' latch

X(t)	Y(t)	A(t)	B(t)	X(t+τ)	Y(t+τ)
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	0	0

1. If the **propagation delay** of each gate is **5 ns,** the **minimum length of time** that (valid) input combinations need to be asserted **in order to prevent metastable behavior** is:

    (A) 0 ns   (B) 5 ns   (C) 10 ns   (D) 20 ns   (E) none of these

2. If the **input** combination A=0, B=0 is applied to this circuit, the (steady state) output will be:

    (A) X=0, Y=0   (B) X=0, Y=1   (C) X=1, Y=0   (D) X=1, Y=1   (E) unpredictable

3. If the **input** combination A=0, B=1 is applied to this circuit, the (steady state) output will be:

    (A) X=0, Y=0   (B) X=0, Y=1   (C) X=1, Y=0   (D) X=1, Y=1   (E) unpredictable

4. If the **input** combination A=0, B=0 is applied to this circuit, **followed immediately** by the **input** combination A=1, B=0, the (steady state) output will be:

    (A) X=0, Y=0   (B) X=0, Y=1   (C) X=1, Y=0   (D) X=1, Y=1   (E) unpredictable

5. If the **input** combination A=0, B=0 is applied to this circuit, **followed immediately** by the **input** combination A=1, B=1, the (steady state) output will be:

    (A) X=0, Y=0   (B) X=0, Y=1   (C) X=1, Y=0   (D) X=1, Y=1   (E) unpredictable