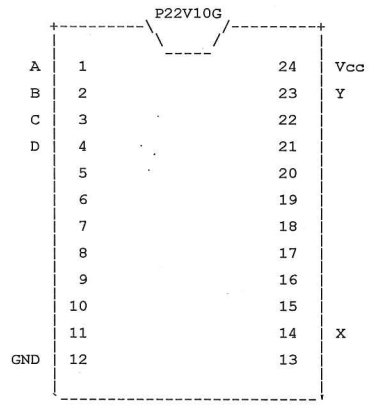
Practice Quiz 7

The **ispLever-Generated Reports** below apply to the questions on this quiz:

CHIP REPORT:

```
X = B&D&!A&C # !B&!D&!A&C
    # B&D&A&!C # !B&!D&A&!C;
Y = B&D # A&C # !A&!C;
```



REDUCED EQUATION REPORT:

P-Terms	Fan-in	Fan-out	Type	Name (attributes)
4/4	4	1	Pin	X
3/4	4	1	Pin	Y
7/8				

```
                Best P-Term Total: 7
                        Total Pins: 6
                       Total Nodes: 0
              Average P-Term/Output: 3
```

best P-term total

ispLEVER operators:
AND - & OR - #
NOT - ! XOR - $

```
Positive-Polarity Equations:
X = !B&!D&A&!C # B&D&A&!C # !B&!D&!A&C  # B&D&!A&C;
Y = B&D # !A&!C # A&C;

Reverse-Polarity Equations:
!X = B&!D # !B&D # !A&!C # A&C;
!Y = !D&A&!C # !B&A&!C # !D&!A&C # !B&!A&C;
```

1. The **fitter program** chose the **following form(s)** of the reduced equations to burn into the PLD:
   (A) the positive polarity forms of both X and Y
   (B) the reverse polarity forms of both X and Y
   (C) the positive polarity form of X and the reverse polarity form of Y
   (D) the reverse polarity form of X and the positive polarity form of Y
   (E) none of the above

   match chip report to reduced equation report

2. The **total number of P terms** used by this Verilog program is:
   (A) 3 (B) 4 (C) 7 (D) 8 (E) none of these

3. A possible **Verilog source form** of the equation for **X** is:
   (A) `X = (B ^ D) & (A ~^ C);`
   (B) `X = (B ^ D) | (A ~^ C);`
   (C) `X = (B ~^ D) & (A ^ C);`
   (D) `X = (B ~^ D) | (A ^ C);`
   (E) none of the above

4. A possible **Verilog source form** of the equation for **Y** is:
   (A) `Y = (A ^ C) | (B & D);`
   (B) `Y = (A ~^ C) | (B & D);`
   (C) `Y = (~A ^ ~C) | (B & D);`
   (D) `Y = (A ~^ C) & (B | D);`
   (E) none of the above

5. The **order** in which dataflow equations appear in Verilog program **does <u>not</u> matter.**
   (A) true (B) false