Practice Quiz 2

Closed Book and Notes

1. The **direction that current flows** between the drain (D) and source (S) of N-channel and P-channel MOSFETS is as follows:
   (A) N-channel: D→S; P-channel: S→D
   (B) N-channel: S→D; P-channel: D→S
   (C) N-channel: D→S; P-channel: D→S
   (D) N-channel: S→D; P-channel: S→D
   (E) none of the above

2. For most CMOS logic families, the **maximum acceptable V_{IL}** is:
   (A) 10% of the power supply voltage
   (B) 30% of the power supply voltage
   (C) 50% of the power supply voltage
   (D) 70% of the power supply voltage
   (E) 90% of the power supply voltage

3. For most CMOS logic families, the **switching threshold** is:
   (A) 10% of the power supply voltage
   (B) 30% of the power supply voltage
   (C) 50% of the power supply voltage
   (D) 70% of the power supply voltage
   (E) 90% of the power supply voltage

4. When **A = 0 V** and **B = 5 V,** the potential at **Vout** will be:
   (A) 0.00 V
   (B) 1.25 V
   (C) 2.50 V
   (D) 5.00 V
   (E) none of the above

5. When **A = 5 V** and **B = 0 V,** the amount of power dissipated by this circuit is:
   (A) 5 µW
   (B) 25 µW
   (C) 50 mW
   (D) 250 mW
   (E) none of the above